V.V.I

Mobility (μ) :- Mobility denotes the current carrying capacity or how fast the charge carrier is moving from one place to another place.

Mobility is defined as drift velocity of electric field Intensity.

$$\boxed{\mu = \frac{v_d}{E}} = v_d = \text{drift velocity.}$$

unit of mobility (μ) $= \frac{v_d}{E} = \frac{m/sec}{volt/m} = \boxed{\frac{m^2}{volt\,sec}}$

μ_n = mobility of electrons.

μ_p = mobility of holes.

$$\boxed{v_d = \mu E}$$

Drift current :- when applying potential through electrical circuits, if current is flowing from higher concentration to lower concentration.

Diffusion current :- It is defined as current carrier is flow from higher concentration to lower concentration through electrical circuits.

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ϵ = Permittivity

$\epsilon = \epsilon_0 \epsilon_r$; $\epsilon_0 = 8.85 \times 10^{-12}$ F/m

ϵ_r = Relative permittivity.

Einstein Relation (D_p) :-

D = Diffusion constant = Diffusivity.

$$\boxed{\frac{D_p}{\mu_p} = \frac{D_n}{\mu_n} = V_T}$$

(V_T = thermal voltage)

$$V_T = \frac{KT}{q} = \frac{T}{11600} \text{ volt}$$

properties of silicon & Germanium

	Property	Ge (2, 8, 18, 4)	Si
(1)	Atomic no	32	14
(2)	Atomic weight	72.6	28.1
(3)	Density (g/cm³)	5.32	2.33
(4)	Relative dielectric const.	16	12
(5)	Atoms/cm³	4.4×10^{22}	5×10^{22}
(6)	Energy Gap (E_g) at 0K (ev)	0.785 ev	1.21 ev
(7)	E_g at 300K (room temp)	0.72	1.1

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(8)	Intrinsic charge carrier conc^n (n_i) at 300 K (cm^{-3})	2.5×10^{13}	1.5×10^{10}
(9.)	Intrinsic resistivity at 300 K (Ωm)	45	230,000
(10.)	Mobility of e^- (μ_n) at 300K	3800	1200
(11.)	Mobility of holes (μ_p) $cm^2/volt \cdot sec$ at 300 K	1800	500
(12.)	D_n (cm^2/sec) $= \mu_n \times V_T$	99	34
(13.)	D_p (cm^2/sec) $= \mu_p \times V_T$	47	13

$\frac{D_p}{\mu_p} = V_T \Rightarrow D_p = V_T \times \mu_p = volt \times \frac{cm^2}{volt \cdot sec}$

$$\boxed{D_p = \frac{cm^2}{sec}}$$

For silicon (Si) :-

$$\boxed{E_G = 1.21 - 3.6 \times 10^{-4} \times T \ eV}$$

E_G of Si at 0K $= 1.21 - 3.6 \times 10^{-4} \times 0$

$= 1.21 \times 0$

$= 1.21 \ eV$

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E_G of Si at 300 K $= 1.21 - 3.6 \times 10^{-4} \times 300$
$= 1.1$ eV

For Germanium :-

$$\boxed{E_G = 0.785 - 2.23 \times 10^{-4} T}$$

E_G of Ge at 0K $= 0.785 - 2.23 \times 10^{-4} \times 0$
$= 0.785 - 0$
$= 0.785$

E_G at room temp $= 0.785 - 2.23 \times 10^{-4} \times 300$
$= 0.72$ eV

Two types of mobile charge carriers (+ve & -ve e^-) are available.

⇒ In an electric field the current conduction is due to the drift current of the carriers due to the application of applied potential.

⇒ Carrier diffuse if a concentration gradient exist.

Continuity equation of charge :-

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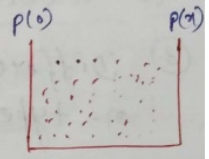
→ Law of conservation of charge.

Considering that charge can neither be created not be destroyed if generation recombination, drift & diffusion all taken into account.

constant Gradient (Derivative w.r.to t)

$$\boxed{\frac{\partial p}{\partial t} = \frac{p_0 - p}{\tau_p} - \frac{1}{q} \cdot \frac{\partial J_p}{\partial x}}$$

p = charge conc^n



Assignment :-

(i) Define mobility. write the unit of mobility.

Ans :- Mobility (μ) :- It is defined as the ratio of drift velocity (v_d) and Electric field intensity (E).

$$\text{mobility} = \frac{\text{drift velocity } (v_d)}{\text{electric field intensity } (E)}$$

* unit of mobility $= \frac{v_d}{E} = \frac{m/sec}{volt/m} = \frac{m^2}{volt \cdot sec}$.

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(2.) Difference between drift current & diffusion current.

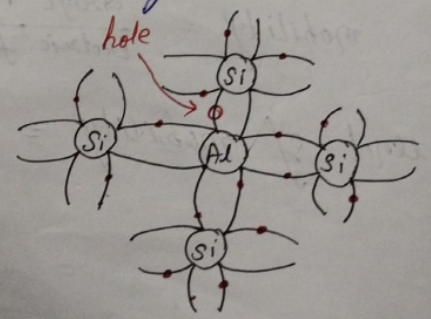
Ans :- Drift current :- It is the current flowing through circuit from higher level to lower level when potential is applied.

Diffusion current :- It is defined as when current carrier is flow from higher concⁿ to lower concⁿ through Electrical circuits

(3.) Different between p-type semiconductor & n-type semiconductor ?

Ans :- p-type semiconductor :- when suitable trivalent impurity is added to pure silicon or Germanium crystal we get extrinsic semiconductor called p-type semiconductor. Each trivalent impurity atom accepts one e^- from the neighbouring silicon atom so it is known as acceptor impurity.

$n_h > n_e$



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② Difference between drift current & diffusion current.

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③ Different between p-type semiconductor & n-type semiconductor?

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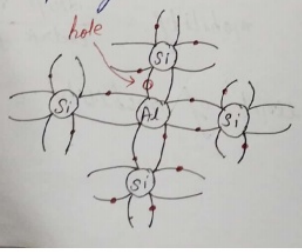
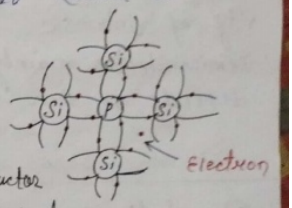


n-type semiconductor :- when suitable pentavalent impurity is added to pure silicon or Germanium crystal. we get an extrinsic semiconductor known as n-type semiconductor. Each pentavalent impurity atom donates one electron to the crystal so it is also known as Donar impurity.

$n_e > n_h$



(4) What is Instrinsic semiconductor and what is Extrinsic semiconductor?

Ans:-

Intrinsic	Extrinsic
(i) Intrinsic semiconductor are the crystals of pure elements like germanium and silicon	(i) when some impurity is added in the intrinsic semiconductor we get an extrinsic sem.
(ii) In intrinsic semiconductor the no. of density of electrons is equal to the no. of density of holes. i.e $n_e = n_h$	(ii) In extrinsic semiconductor the no. of density of e^- is not equal to no of density of holes. i.e $n_e \neq n_h$

(iii) The electrical conductivity of Intrinsic Semiconductor is low.	(iii) The electrical conductivity of extrinsic semiconductor is high.
(iv) Resistivity is higher	(iv) Resistivity is lower.
(v) The electrical conductivity of Intrinsic semiconductor mainly depends on their temp.	(v) The electrical conductivity of extrinsic semiconductor depends on the temp. as well as the amount of Impurity added in them

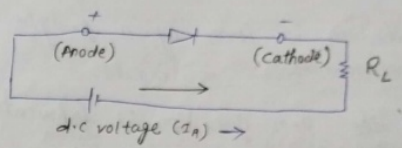
⑤ What is dopping ?

Ans :- It is the process of adding some Impurities to the Extrinsic semiconductor to Inc. the conductivity of the material.

⑥ What is diffusivity? Write the unit of diffusivity.

Ans :- Diffusivity defined as the rate of diffusion, a measure of the rate at which particle or heat or fluids can spread. Diffusivity $= \frac{cm^2}{sec}$

Semiconductor diode.



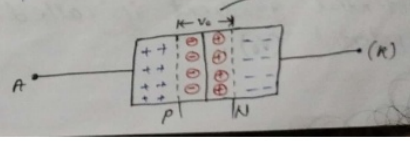
A diode is a two terminal device which conductos current effectively in only one direction.

It has two terminals anode (A) & cathode (K)

I_A is the direction of current flow. I_A is the function of d.c voltage applied accross its two terminals.

A p-n Junction diode is obtained when p-type conductivity & n-type conductivity of silicon crystal is closed to each other. p-type semiconductor has +ve charge carriers called holes and n-type semiconductor has -ve charge carrier called electrons.

The holes same electron are free to take parts in conduction. → Depletion layer



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on Baised p-n Junction (d.c voltage).

UNBIASED P-N JUNCTION

→ A p-n Junction is form by a p-type & n-type semiconductor materials.

As soon as the p-n Junction is fabricated some e^- across over the Junction from n-type to p-type because of conc^n gradient. The e^- entering into the p-region recombine with holes before moving deeper into it. these cause the decrease in concentration of holes in the p-region near p-n Junction. the holes deffusing from p-region to n-region cause a dec. in conc^n of e^- in n-regions near the p-n Junction.

⇒ This region is called depletion region.

→ The depletion region contains immobile charge i.e donors in the p-side & the acceptor in the n-side. The presence of two group of converted immobile oppositely charged ions give rise to an electric field and hence to a potential gradient is called contact potential (V_0).

three charge carriers exist only outside the depletion region because of contact potential electrons cannot diffuse from n-side to p-side.

i.e, holes cannot diffuse from p-type to n-type.

However there is a small drift current from n to p region by the thermally generated holes in the n-regions and e^- in the p-region.

The net current in the unbaised Junction is 0.

Hence, under equilibrium condition the value of V_0 is such that the forward diffusion current equals to the revers drift current

The contact potential of Ge = 0.3 V (0.2 to 0.4 V)

The contact potential of Si = 0.7 V (0.6 to 0.9 V)

This contact potential depends upon the doping concentration is acceptor (n_A) donar (n_D)

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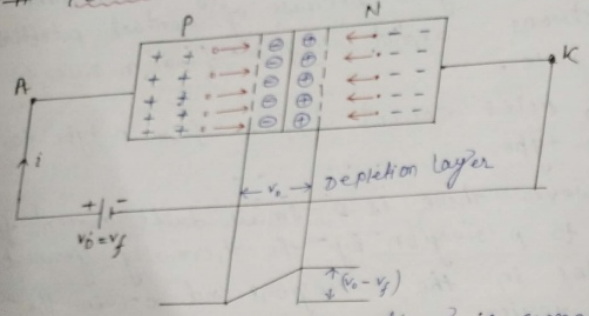
Forward Biased



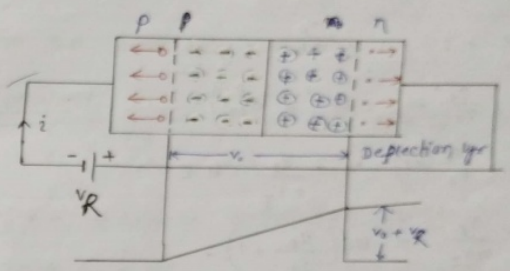
When the +ve terminal of battery is connected to p-region and -ve terminal of battery is connected to n-region of the junction diode, then the p-n junction diode is said to be forward baised.

In forward baising the Effective barrier potential reduces to $(V_0 - V_f)$ and the knees of depletion layer also dec.

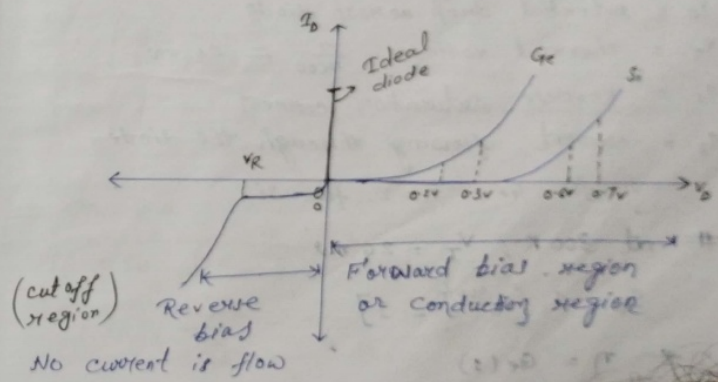
Reverse biased p-N junction.

When the +ve terminal of battery is connected to n-region and -ve terminal of battery is connected to p-region of the junction diode is said to be Reverse biased.

In reverse baising the effective barrier potential increase to $(V_0 + V_R)$ and also thickness of the depletion layer inc. the junction resistance inc. in reverse bias.



V-I characteristics of p-N junction diode



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Diode current equation:

$$\boxed{I_D = I_R\left(e^{\frac{-V_R}{\eta V_T}} - 1\right)}$$ (η = ita)

$$\Rightarrow \frac{I_D}{I_S} = e^{\frac{-V_D}{\eta V_T}} - 1$$

$$\Rightarrow \frac{I_D}{I_S} + 1 = e^{\frac{-V_D}{\eta V_T}}$$

$$\Rightarrow \ln\left(\frac{I_D}{I_S} + 1\right) = \ln\left(e^{\frac{-V_D}{\eta V_T}}\right)$$

$$\Rightarrow \ln\left(\frac{I_D}{I_S} + 1\right) = -\frac{V_D}{\eta V_T} \cdot \ln e$$

$$\Rightarrow -\frac{V_D}{\eta V_T} = \ln\left(\frac{I_D}{I_S} + 1\right)$$

V_R = Reverse voltage

V_D = potential drop across diode

V_T = Thermal voltage $= \frac{T}{11600} \simeq 26$ mV

I_S = Reverse saturation current.

I_D = current flowing through the diode.

$\eta = 1$ for Ge, $\eta = 2$ for Si

at 300 K, $V_T = 26$ mV

$$I_D = I_S\left[e^{40V/\eta} - 1\right]$$

* η = Ge (1)

$$I_D = I_S\left[e^{40V} - 1\right] \longrightarrow (1)$$

* η = Si (2)

$$I_D = I_S\left[e^{20V} - 1\right] \longrightarrow (2)$$

(a) Ge ~~p-n~~ ~~Diode~~, ~~I_S = 0.3 μA~~, V

Forward Bias

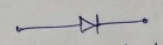
$$\boxed{I_D = I_R\left(e^{\frac{V_F}{\eta V_T}} - 1\right)}$$ [$I_S = I_R$ = Reverse saturat current]

$I_R = I_S$ = Reverse saturation current.

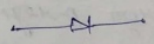
I_R = Ge = μA

I_R = Si = nA

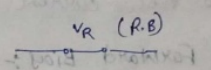
In F.B

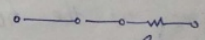


Ideal diode



practical diode





In R.B

$$I_D = I_R\left(e^{\frac{-V_R}{\eta V_T}} - 1\right)$$

$$= I_R\left(\frac{1}{e^{\frac{V_R}{\eta V_T}}} - 1\right)$$

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$V_T = 26\ mV$

$V_R \gg V_T$

$\Rightarrow e^{-\frac{V_R}{\eta V_T}} = \infty$

$\Rightarrow e^{-\frac{V_R}{\eta V_T}} = -\infty$

$e = 0$

when $V_R \ggg V_T$

$e^{V_R/\eta V_T} \simeq 0$

$I_D = I_R(0-1)$

$\Rightarrow I_D = -I_R$

So net current is zero

In Forward Bias :-

The Barrier potential across the p-N Junction decreases as the holes from p-region moves towards the junction and cross over the junction and injected into into the n-region.

→ The distribution of holes in the n-region are called majority charge carriers. They deffuse towards the cathode terminal and contribute whole current.

Ly, The e^- from the n-region injected into the p-region and diffuse towards the positive anode terminal and contribute the e^- component of the current.

The diffusion current across the junction is must larger than the reverse drift current.

Imp The diffusion current depends upon the concentration majority charge carriers.

In Reverse bias :-

→ The contact potential is increase from V_0 to $V_0 + V_R$

→ The holes in the p-region and the electron in the n-region move away from the junction. A large no. of ionised immobiles atoms around the junction are exposed. Hence the forward deffusion current is zero but a very small drift current flows from cathode to anode and is independ of bias suffly voltage V_R.

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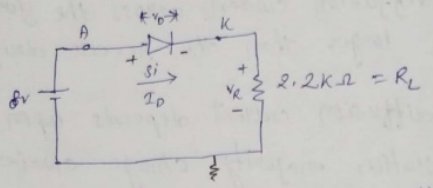
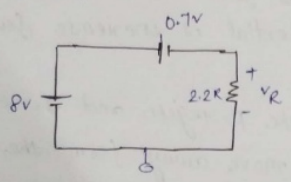
The reverse saturation current every 10°c rise in temperature.

$(I_R = I_S)$ doubles.

Q) ① Determine V_D, I_D, V_R



Solⁿ :- V_D = potential drop in silicon diode = 0.7v



~~Applied~~ Applying ~~Kirct~~ Kichorff voltage law (KVL) on the above ckt.

$\Rightarrow 8v - 0.7v - V_R = 0$

$\Rightarrow V_R = 8v - 0.7v$

$\Rightarrow V_R = 7.3v$

The I_D current is flowing through the resister 2.2 kΩ

So, the potential drop across the resister is V_R

$V_R = I_D \times R_L$

$\Rightarrow 7.3v = I_D \times 2.2K\Omega$

$\Rightarrow I_D = \frac{7.3}{2.2K}$

$\Rightarrow I_D = \frac{7.3 \times 10^{-3}}{2.2}$ A

$\Rightarrow I_D = \frac{7.3}{2.2}$ mA $= 3.32$ mA

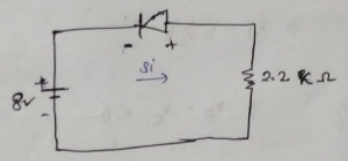
$\boxed{K = 10^3}$

$\boxed{10^{-3} A = 1 mA}$

KVL

Sum of all potentials ~~which~~ is equal to zero.

$\sum$ all potentials = 0

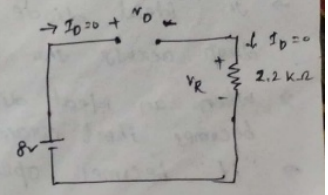
② 

Determine V_D, I_D, V_R

Solⁿ :- V_D = potential drop in silicon diode = 0.7v.

~~Applying Kichorff voltage law (KVL) on the above ckt~~

~~$\Rightarrow 8v + 0.7v - V_R = 0$~~



Here the diode is reversed Bias., so no current flow in the ckt.

i.e $I_D = 0$

If $I_D = 0$, then $V_R = I_D \times 2.2\,K\Omega$

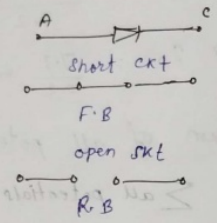
$= 0 \times 2.2\,K\Omega = 0.$

Applying KVL.,

$8V - V_D - V_R = 0$

$\Rightarrow 8V - V_D - 0 = 0$

$\Rightarrow V_D = 8V.$



F.B.

$V_A > V_C \Rightarrow V_A - V_C > 0$

R.B

$V_A < V_C \Rightarrow V_A - V_C < 0.$

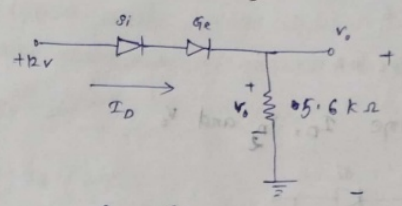
When diode is connected with reverse bias then it becomes off state that is open circuited no current flow through the circuit

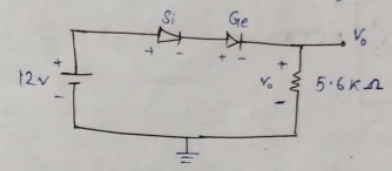
→ In ideal diode there is no potential drop across the diode

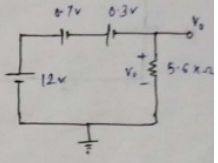
→ When an ideal diode is Forward biased it becomes short circuit and in Reverse biased

→ it becomes open circuit

Prob. ③ Determine V_o and I_D







Both Si & Ge diode are forward biad.

So the Si & Ge diode is replace by 0.7 & 0.3V

Calculation of V_o

Applying KVL in the circuit

$12V - 0.7V - 0.3V - V_o = 0$

$\Rightarrow V_o = 12 - 1V = 11V$, $\boxed{V_o = 11V}$

calculation of I_D.

$V_o = I_D \times 5.6\,K\Omega$

$\Rightarrow I_D = \frac{V_o}{5.6K\Omega} \Rightarrow I_D = \frac{11V}{5.6\,K\Omega} = \frac{11}{5.6} \times 10^{-3}\,A$

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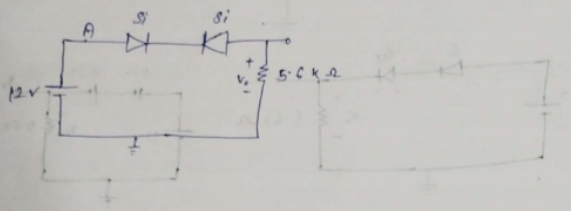
$\Rightarrow I_D = \frac{11}{5.6}$ mA

$\Rightarrow I_D = 1.96$ mA

(4) Determine I_D, V_{D_2} and V_o



b) What is the ratio of current for forward biased mode with voltage 0.05 V to the current with same magnitude of reverse bias.

Soln:- For forward bias current

300K = 26 mV
= 0.026 V

$$I_F = I_0 \left(e^{\frac{V_F}{\eta V_T}} - 1\right)$$

$$\Rightarrow I_F = I_0 \left(e^{0.05/\eta V_T} - 1\right) \rightarrow (1)$$

For reverse bias current

$$I_R = I_0 \left(e^{\frac{-V_R}{\eta V_T}} - 1\right)$$

$$\Rightarrow I_R = I_0 \left(e^{-0.05/\eta V_T} - 1\right) \rightarrow (2)$$

from eqn (1) & (2) we get

$$\Rightarrow \frac{I_F}{I_R} = \frac{\left(e^{0.05/\eta V_T} - 1\right)}{\left(e^{0.05/\eta V_T} - 1\right)}$$

$$\Rightarrow \frac{I_F}{I_R} = \frac{\left(e^{0.05/0.026} - 1\right)}{\left(e^{-0.05/0.026} - 1\right)}$$

$$\Rightarrow \frac{I_F}{I_R}$$

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Q.) ~~Write~~ A Germanium diode ~~th~~ carries a current of 1 mA at room temp when a forward Bias of 0.15 v is applied. Estimate the reverse saturation current at room temp.

Soln:- $I_D = 1\,mA$,

at room temp, Thermal voltage $= V_T = 26\,mv$

$V_f = 0.15\,v$

We know the diode eqn.

$$I_D = I_R\left(e^{\frac{V_f}{\eta V_T}} - 1\right)$$

for Germanium diode, $\eta = 1$,

$$I_R = \frac{I_D}{\left(e^{\frac{V_f}{\eta V_T}} - 1\right)}$$

$$I_R = \frac{1mA}{\left(e^{\frac{0.15\,A}{1\times 26mV}} - 1\right)}$$

$$I_R = \frac{1}{\left(e^{\frac{0.15}{0.026}} - 1\right)}\,mA$$

$$I_R = \frac{1}{320.29126 - 1}\,mA$$

$$\Rightarrow I_R = \frac{1}{319.29126} \quad \Rightarrow I_R = 3.1319\times 10^{-3}\,mA$$

$$\Rightarrow I_R = 3.13\,\mu A.$$

(2.) ~~A~~ The current flowing through a silicon diode at room temp is $9\times 10^{-7}A$ when a large reverse voltage is applied. Calculate the current following through the diode when 0.4v forward bias is applied.

Soln:- $I_R = 9\times 10^{-7}A$, at room temp

Thermal Voltage $T_V = 26\,mv = 26\times 10^{-3}\,v$

$V_f = 0.4\,v$, I_D

We know that,

$$I_D = I_R\left(e^{\frac{V_f}{\eta V_T}} - 1\right) \longrightarrow (1)$$

for silicon diode, $\eta = 2$

from eqn (1).

$$I_D = 9\times 10^{-7}\left(e^{\frac{0.4}{2\times 0.026}} - 1\right)$$

$$\Rightarrow I_D = 0.00197\,A$$

$$\Rightarrow I_D = 1.97\,mA$$

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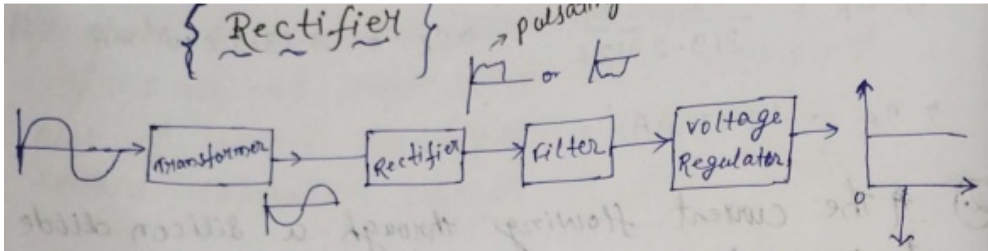
{ Rectifier }



Regulated pure dc. output voltage

Rectifier is a device which converts A.C. or Sinusoidal AC voltage into either positive or negative pulsating D.C.

There are three types of rectifier circuit.

(i.) Half Wave Rectifier

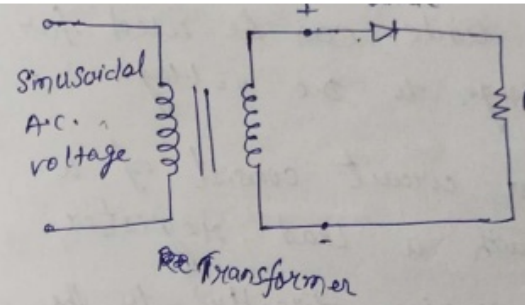
(ii.) Full Wave Rectifier

(a.) centre-tapped voltage Full wave Rectifier

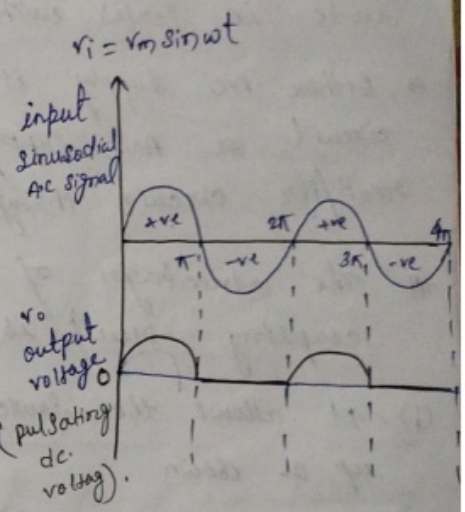
(b.) Bridge-type Full Wave Rectifier

(iii.) Peak Rectifier.

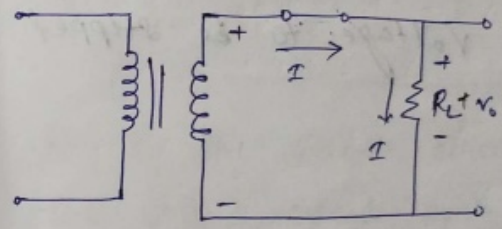
i.) **Half Wave Rectifier** :- A half wave rectifier converts an AC signal to DC by passing either the negative or positive half cycle of the waveform and blocking the other



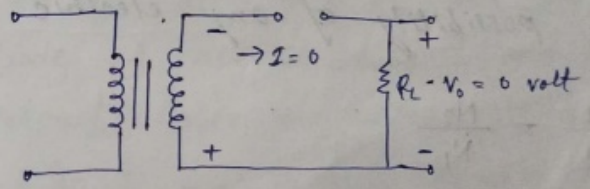
$v_i = V_m \sin \omega t$



During +ve half cycle of input voltage



During -ve half cycle of input voltage



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The semiconductor diode can be used for converting A.C. voltage to D.C voltage

→ Half wave rectifier circuit consist of a diode in series with a load register

→ Either AC supply is given directly to the circuit or A.C supply is given to the rectifier circuit through a transformer.

The advantages of using transformer coupling circuit is :-

(i) It allows the source voltage to be stepped up or down

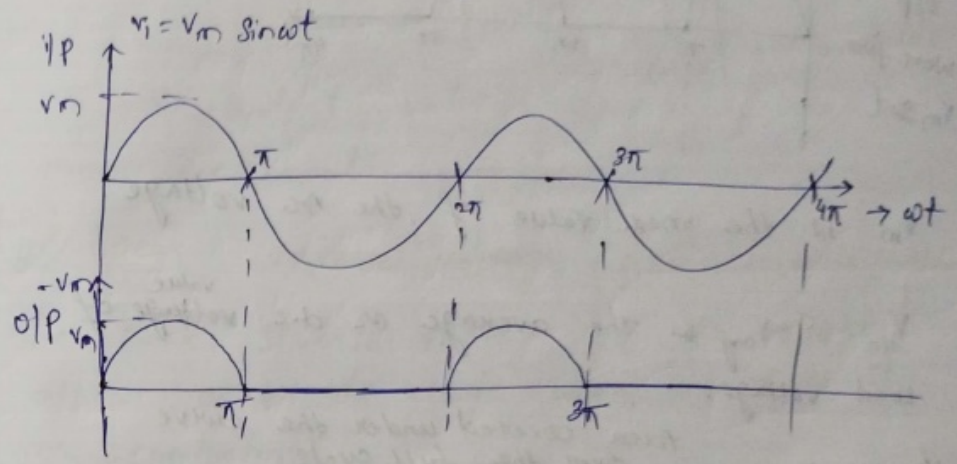
$$\frac{V_2}{V_1} = \frac{N_2}{N_1}$$

(ii) The AC power supply source is electrically Isolated from the rectifier circuit. it reduces the possibility of any electric shock.

$$\frac{V_2}{V_1} = \frac{N_2}{N_1}$$

where V_1 is the r.m.s value of primary voltage then V_2 r.m.s value of secondary voltage.

N_1 is the no. of turns in the primary winding then N_2 is the no. of turns in the secondary winding



In the diode circuit during +ve half of the Input ~~cycle~~ cycle (0-π) the diode is forward biased

→ During -ve half of the Input cycle, the diode is reverse biased and behaves as open circuit hence no current will flow.

assuming the voltage across the diode is negligible, if +ve half of the input the cycle the ~~Input~~ output voltage is equal to output voltage

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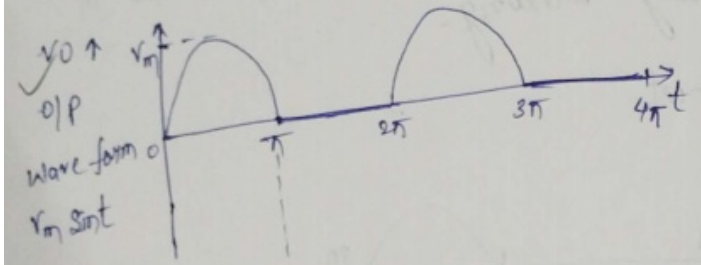
So, we have the output



V_m is the max. value of the A.C voltage.

V_{dc} or V_{avg} is the average or d.c ~~voltage~~ value of load voltage.

$$V_{dc} \text{ or } V_{avg} = \frac{\text{Area covered under the curve over the full cycle}}{\text{time period}}$$

$$= \frac{\int_0^{\pi} V_m(t) \cdot dt}{2\pi} = \frac{\int_0^{\pi} V_m \sin t \cdot dt}{2\pi}$$

$$\Rightarrow V_{dc} = \frac{V_m}{2\pi} \left[-\cos t\right]_0^{\pi}$$

$$\Rightarrow V_{dc} = \frac{V_m}{2\pi} \left[\cos t\right]_{\pi}^{0}$$

$$\Rightarrow V_{dc} = \frac{V_m}{2\pi} \left[\cos 0 - \cos \pi\right]$$

$$\Rightarrow V_{dc} = \frac{V_m}{2\pi} \left[1 - (-1)\right]$$

$$\Rightarrow V_{dc} = \frac{V_m}{2\pi} \cdot 2$$

$$\Rightarrow V_{dc} = \frac{V_m}{\pi} = 0.318\, V_m.$$

$\left[\cos \pi = -1, \ \cos 0 = 1\right]$

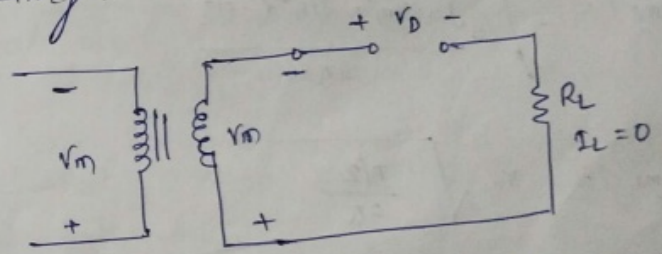
It is seen that the avg. or d.c. value of the output voltage 31.8 % of the max. A.c input voltage.

(V_{rms})

Peak Inverse Voltage (PIV) :- (Diode is off)

The peak Inverse voltage is the voltage appear across the diode when the diode is non-conducting.

~~Let~~ as



Let us Apply KVL to the secondary side.

$$-V_m - V_D = 0$$

$$\Rightarrow \boxed{V_D = -V_m}$$

Hence the max. peak Inverse voltage in half wave rectifier circuit in V_m

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the r.m.s value of the output wave form is equal to V_{rms}.

$$V_{rms} = \sqrt{\frac{\int_0^{2\pi} V_o(t)^2 \cdot dt}{2\pi}}$$

$$= \sqrt{\frac{\int_0^{\pi} (V_m \sin t)^2 \, dt + \int_{\pi}^{2\pi} 0 \cdot dt}{2\pi}}$$

$$\Rightarrow V_{rms} = \sqrt{\frac{\int_0^{\pi} V_m^2 \cdot \sin^2 t \cdot dt}{2\pi}}$$

$$\Rightarrow V_{rms} = V_m \sqrt{\frac{\pi/2}{2\pi}}$$

$$\Rightarrow V_{rms} = V_m \times \sqrt{\frac{\pi}{2} \times \frac{1}{2\pi}}$$

$$\Rightarrow \boxed{V_{rms} = \frac{V_m}{2}}$$

$$\int_0^{2\pi} \sin\theta \cdot d\theta = 0$$

$$\int_0^{2\pi} \cos\theta \cdot d\theta = 0$$

Derive V_{rms}, V_{dc} or V_{avg} of half wave

$$I_{dc} \text{ or } I_{avg} = \frac{I_m}{\pi}$$

$$I_{rms} = \frac{I_m}{2}$$

$$PIV = V_m$$

Average value of d.c current

$$I_{dc} = I_{avg} = \frac{V_{dc}}{R_L} = \frac{V_m/\pi}{R_L}$$

$$= \frac{V_m}{R_L} \times \frac{1}{\pi} = \frac{I_m}{\pi} \quad \left[\because \frac{V_m}{R_L} = I_m\right]$$

In deriving the average value of D.c current and D.C voltage, we have assume the diode is ideal and the forward restiance is zero.

If the diode is not ideal then V_{dc} is equal to then $V_{dc} = \frac{V_m}{\pi} - I_{dc} \cdot R_f$

$$I_{dc} = \frac{V_m}{\pi(R_f + R_L)}$$

When directly we are giving the A.c input signal to the input of half wave rectifier circuit

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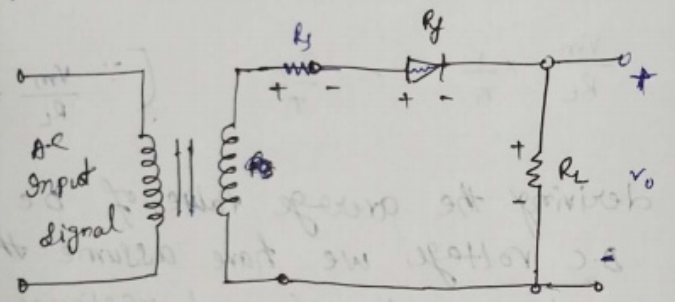
R_f is the forward resistance of the diode.

R_L is the load resistance

Case - II

When a.c input signal is giving input through ~~to the~~ ~~transformer~~ ~~when~~ the half wave rectifier circuit.



→ R_s is the winding Resistance of the transformer. Secondary winding

$$V_{dc} = \frac{V_m}{\pi} - I_{dc}(R_s + R_f)$$

$$I_{dc} = \frac{V_m}{\pi(R_s + R_f + R_L)}$$

Ripple factor :- The output current wave form of a half wave rectifier circuit is shown as a figure. It is seen that the output wave form is periodic in nature with the fundamental period 2π. hence the output wave form contains average value and A.c value. The a.c component present in the output is called ripple. This ripples are on-desirable for electronic circuit operation

$$\boxed{\gamma = \frac{I_{rms}}{I_{dc}}}$$

The ripple factor is defined as the ratio of the ~~rms~~ rms value of current (ac). Component of the output current to the d.c current of the output.

$$\boxed{I_{rms} = \sqrt{I_{dc}^2 + I_{(rms)}^2}}$$

$$\Rightarrow \frac{I_{rms}}{I_{dc}} = \frac{\sqrt{I_{dc}^2 + I_{(rms)}^2}}{I_{dc}}$$

$$\frac{I_{rms}}{I_{dc}} = \sqrt{\frac{I_{dc}^2 + I_{rms}^2}{I_{dc}}}$$

$$\frac{I_{rms}}{I_{dc}} = \sqrt{1 + \frac{I_{(rms)}^2}{I_{dc}^2}}$$

$$\Rightarrow \left(\frac{I_{rms}}{I_{dc}}\right)^2 = 1 + \frac{I_{(rms)}^2}{I_{dc}^2}$$

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$$\Rightarrow \left(\frac{I_{(rms)}}{I_{dc}}\right)^2 = \left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1$$

$$\Rightarrow \frac{I_{rms}}{I_{dc}} = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

$$\Rightarrow r = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

$$\Rightarrow r = \sqrt{\left(\frac{\frac{I_m}{2}}{\frac{I_m}{\pi}}\right)^2 - 1}$$

$$\Rightarrow r = \sqrt{\left(\frac{\pi}{2}\right)^2 - 1}$$

$$\Rightarrow r = \gamma = 1.21.$$

Ripple factor $= \sqrt{\left(\frac{I_{(rms)}}{I_{dc}}\right)^2 - 1}$

// Form factor :- $\frac{I_{rms}}{I_{dc}} = \frac{V_{rms}}{V_{dc}}$

$$= \sqrt{(\text{form factor})^2 - 1}$$

form factor is defined as the ratio of the rms value to the dc. value.

$$\text{form factor} = \frac{I_{rms}}{I_{dc}} = \frac{V_{rms}}{V_{dc}} = \frac{I_m/2}{I_m/\pi}$$

$$= \frac{\pi}{2} = \frac{3.14}{2} = 1.57$$

// Efficiency of half wave rectifier :- (η)

Ac means rms value.

$$\eta = \frac{P_o}{P_i} = \frac{P_{dc}}{P_{ac}}$$

$P = I^2 . R$ = power

$$\Rightarrow P = \frac{I_{dc}^2 \cdot R_L}{I_{rms}^2 (R_f + R_L)}$$

$$\Rightarrow P = \frac{\left(\frac{I_m}{\pi}\right)^2 \cdot R_L}{\left(\frac{I_m}{2}\right)^2 \cdot (R_f + R_L)}$$

$$\Rightarrow P = \frac{4}{\pi^2} \times \frac{R_L}{R_f + R_L}$$

$$\Rightarrow P = \frac{4}{\pi^2} \times \frac{1}{\left(\frac{R_f}{R_L} + 1\right)}$$

$$\eta = \frac{0.406}{1 + \frac{R_f}{R_L}}$$

$$\boxed{\eta = \frac{40.6}{1 + \frac{R_f}{R_L}} \%}$$

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If $R_L \gg R_f$

$$\frac{R_f}{R_L} \simeq 0$$

$$\eta_{max} = 40.6\%$$

$$= 0.406$$

It is seen that the effiency of half wave rectifier circuit is 40.6% under the condition $R_L \gg R_f$. However in actual practice η is less than 40.6%.

Regulation :- The variation of d.c output voltage as a function of d.c load current

$$\% \text{ Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$

NL = No load, FL = Full Load.

Assignment :- (2)

A sinusoidal voltage of 40 V and frequency 50 Hz is applied to a half-wave rectifire. $R_L = 200\,\Omega$, $V_\gamma = 0$. $R_f = 20\,\Omega$, $R_r = \infty$.

Find V_{dc}, I_{dc}, I_{max}, I_{rms}, P_{dc}, η, ripple factor, % regulation.

Solⁿ :- $V_{rms} = 40\ V$

Frequency, $f = 50\ Hz$

$R_L = 200\,\Omega = 0.2\,k\Omega$

$R_F = 20\,\Omega = 0.02\,k\Omega$

$R_r = \infty$, $V_\gamma = 0$

$$I_{max} = \frac{V_{s\,max}}{R_L + R_F} = \frac{40\sqrt{2}}{200+20} = 0.257\,A \text{ or } 257\,mA \text{ Ans}$$

$$I_{rms} = \frac{I_{max}}{2} = \frac{257}{2} = 128.5\,mA \text{ Ans}$$

$$I_{dc} = \frac{I_{max}}{\pi} = \frac{257}{\pi} = 81.8\,mA \text{ Ans}$$

$$V_{dc} = I_{dc} R_L = 81.8 \times 10^{-3} \times 200 = 16.36\,V \text{ Ans}$$

$= 81.8\,mA \times 0.2\,k\Omega$ $= 81.8 \times .2\,V = 16.36\,V$

$$P_{dc} = I_{dc}^2 R_L = (81.8 \times 10^{-3})^2 \times 200 = 1.338\,W \text{ Ans}$$

$$P_{ac} = \frac{I_{max}^2}{4}(R_F + R_L)$$

$$= \frac{(257 \times 10^{-3})^2}{4} \times (20 + 200) = 3.63\,W$$

$$\eta = \frac{P_{dc}}{P_{ac}} \times 100 = \cancel{1.38}\ \frac{1.338}{3.63} \times 100 = 36.86\%$$

$$\text{Ripple factor, } \gamma = \left(\frac{I_{rms}^2}{I_{dc}^2} - 1\right)^{1/2}$$

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$$= \sqrt{\left(\frac{128.5}{81.8}\right)^2 - 1} = 1.21 \text{ Ans}$$

$$V_{dc} = \frac{V_{max}}{\pi} - I_{dc} R_f = \frac{40\sqrt{2}}{\pi} - 81.8 \times 10^{-3} \times 20$$

$$= 18 - 1.636 = 16.364\,V$$

$$\text{Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$

$$= \frac{\frac{V_{max}}{\pi} - I_{dc} \cdot R_f}{I_{dc} \cdot R_f} \times 100$$

$$= \frac{18 - 16.364}{16.364} \times 100 = 9.998\% \text{ Ans}$$

$V_{rms} = \frac{V_{max}}{\sqrt{2}} \Rightarrow V_{max} = V_{rms} \times \sqrt{2}$

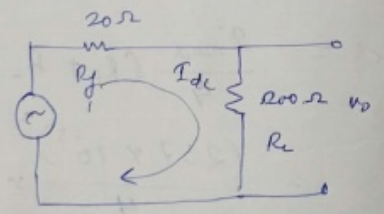
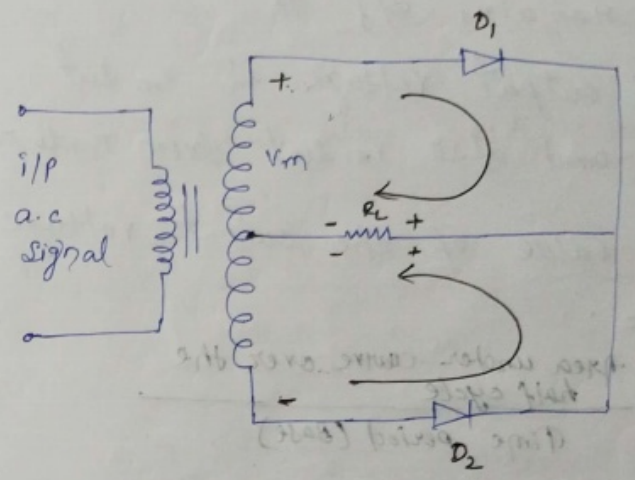
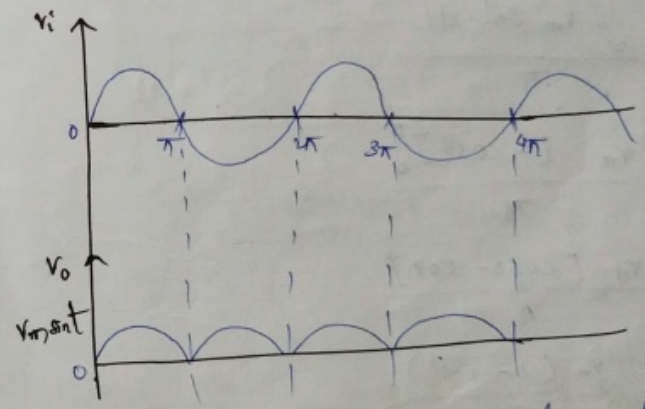


fig. of Assig. ②

Full wave Rectifier :- ① center tapped





① During +ve half of the input voltage $V_i = V_m$ is +ve. The diode D_1 conducts and D_2 ~~even~~ remains off

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During -ve input cycle diode D_2 conducts and diode D_1 remains off.

⇒ The resulting output voltage is $V_m \sin t$ from 0 to π and also $V_m \sin t$ from π to 2π

The average value of the output voltage is equal to V_{dc}.

$$V_{dc} \text{ or } V_{avg} = \frac{\text{Area under curve over the half cycle}}{\text{Time period (Base)}}$$

$$= \frac{\int_0^{\pi} V_m \sin t \cdot dt}{\pi}$$

$$= \frac{V_m \left[-\cos t\right]_0^{\pi}}{\pi}$$

$$= \frac{V_m \left[\cos 0 - \cos \pi\right]}{\pi}$$

$$= \frac{V_m (1 - (-1))}{\pi}$$

$$= \frac{2V_m}{\pi}$$

$$\boxed{V_{dc} \text{ or } V_{avg} = \frac{2V_m}{\pi}}$$

∴ Hence average value of D.C output current

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{2V_m}{\pi} \times \frac{1}{R_L} = \frac{2V_m}{\pi R_L}$$

V_{rms} of full wave rectifier circuit. (output wave form).

$$V_{rms} = \sqrt{\frac{\int_0^{\pi} (V_m \sin t)^2 \cdot dt}{\pi}}$$

$$= \sqrt{\frac{\int_0^{\pi} V_m^2 \cdot \sin^2 t \cdot dt}{\pi}}$$

$$= \sqrt{\frac{V_m^2 \int_0^{\pi} \sin^2 t \cdot dt}{\pi}}$$

$$= \sqrt{\frac{V_m^2 \times \pi/2}{\pi}}$$

$$= \sqrt{\frac{V_m^2}{2}} \Rightarrow \boxed{\frac{V_m}{\sqrt{2}} = V_{rms}}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$I_{dc} = \frac{2I_m}{\pi}$$

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ripple factor $= r = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$

$$= \sqrt{\left(\frac{\frac{I_m}{\sqrt{2}}}{\frac{2 I_m}{\pi}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1} = \boxed{0.482}$$

form factor $= \frac{I_{rms}}{I_{dc}} = \frac{\frac{I_m}{\sqrt{2}}}{\frac{2 I_m}{\pi}} = \frac{\pi}{2\sqrt{2}}$

$$= \frac{\pi}{2 \times 1.414} = \frac{\pi}{2.828} = 1.11$$

Efficiency of Full Wave Rectifier :-

$$\eta = \frac{P_{dc}}{P_{ac}} \times 100$$

$$= \frac{I_{dc}^2 \cdot R_L}{I_{rms}^2 \cdot (R_f + R_L)}$$

$$= \frac{\left(\frac{2 I_m}{\pi}\right)^2 \cdot R_L}{\left(\frac{I_m}{\sqrt{2}}\right)^2 (R_f + R_L)}$$

$$\eta = \frac{8}{\pi^2} \times \frac{R_L}{R_f + R_L}$$

$$\eta = .812 \times \frac{1}{\frac{R_f + R_L}{R_L}}$$

$$\eta = \frac{.812}{1 + \frac{R_f}{R_L}}$$

$$\boxed{\therefore \eta\% = \frac{81.2}{1 + \frac{R_f}{R_L}} \%}$$

$$\eta = 81.2\% = 0.816.$$

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S.No	Particulars	Half Wave Rectifier	Full Wave Rectifier	
			Centre-Tap	Bridge
1.	No. of diode required	1	2	4
2.	Transformer requirement	not essential	essential by centre tap	not essential
3.	Average value of current I_{dc}	I_{max}/π	$2I_{max}/\pi$	$2I_{max}/\pi$
4.	RMS value of current, I_{rms}	$I_{max}/2$	$I_{max}/\sqrt{2}$	$I_{max}/\sqrt{2}$
5.	Peak inverse voltage (PIV)	$V_s max$	$2V_s max$	$V_s max$
6.	Peak load current, I_{max}	$\frac{V_s max}{R_L + R_f}$	$\frac{V_s max}{R_L + R_f}$	$\frac{V_s max}{R_L + 2R_f}$
7.	DC output voltage V_{dc}	$(I_{max}/\pi) \times R_L$	$(2/\pi) I_{max} R_L$	$(2/\pi) I_{max} R_L$
8.	Rectificat^n efficiency	40.6 %	81.2 %	81.2 %
9.	Ripple factor	1.21	0.482	0.482
10.	Fundamental frequency of ripple	Supply frequency, f	2f	2f
11.	Voltage regulation	good	better	good
12.	Transformer utilisat^n factor	0.286.	0.692	0.812
13.	Form factor	1.57	1.11	0.812
14.	peak factor.	2	$\sqrt{2}$	$\sqrt{2}$

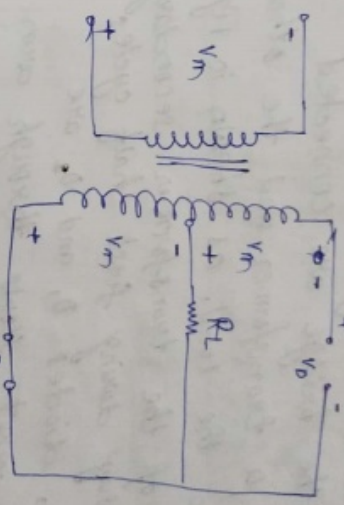
Advantages of center tapped F.W.R. ckt.

(i) The d.c output voltage and current values are twice then those of H.W.R. ckt

(ii) the ripple factor is much less than HWR ckt

(iii) the efficency is twice that of half wave rectifier circuit.

Peak Inverse voltage (PIV) of center tapped F.W.R.



Applying KVL to the outer loop,

$$-V_m - V_m - V_o = 0$$

$$\Rightarrow V_o = -2V_m$$

Hence, Max peak Inverse voltage across each diode is $2V_m$.

Disadvantage:- It is very difficult to construct.

(ii) Peak Inverse voltage is $2V_m$ of half wave Rectifier.

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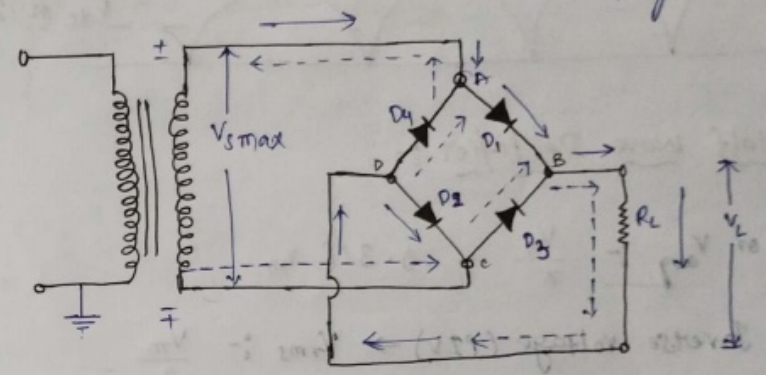
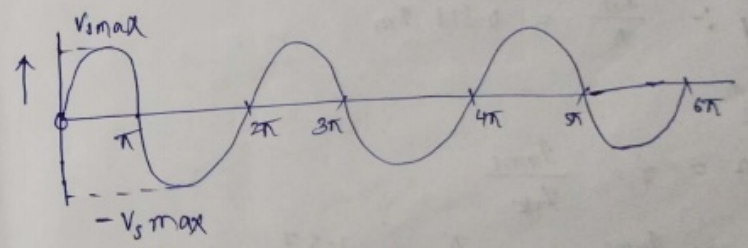
Bridge rectifier :-

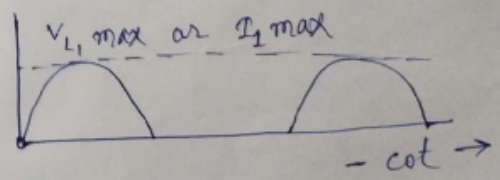
→ A type of full-wave rectifier that uses four or more diodes in a bridge circuit configuration to efficiently convert alternating current (AC) to direct current (DC).

construction :-

In the bridge circuit four diode are connected in the form of a wheatstone bridge. two diametrically opposite junctions of the bridge are connected to the secondary of a transformer and the other two are connected to the load, as shown in fig. when the upper end of the transformer secondary winding is positive, say during first half cycles of the input supply, diodes D_1 and D_2 are forward biased and current flows through arm AB, enters the load at positive terminal, leaves the load at -ve terminal, and returns back flowing through arm DC. During this half of each input cycle, the diodes D_4 and D_3 are reverse biased and so the current is not allowed to flow in Arms AD and BC. The flow of current is ~~not allowed to~~ indicated by solid arrows end of ac supply becomes positive, diodes D_2 and D_4 become forward biased and current flows through arm DA. Flow of current has been shown by dotted arrows in the figure. Thus the direction of flow of current ~~has been shown by~~ through the load resistance R_L remains the same during both half cycles of the input supply voltage.







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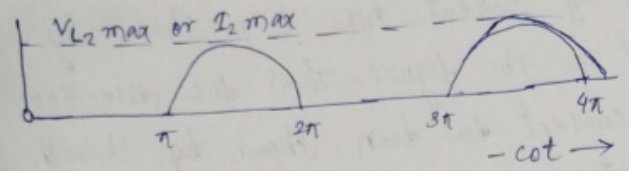
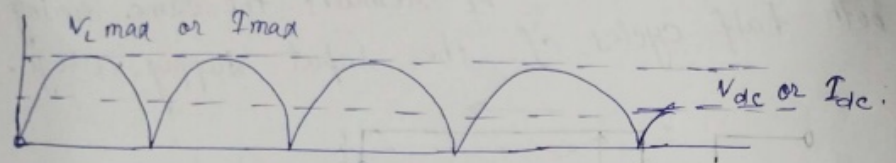




Extra

Half Wave Rectifier :-

V_{dc} or V_{avg} :- $\frac{V_m}{\pi} = 0.318\ V_m$

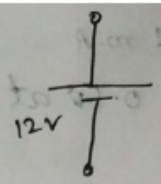
Peak Inverse voltage (PIV) → V_{rms} :- $\frac{V_m}{2}$

I_{dc} or I_{avg} :- $\frac{I_m}{\pi} = 0.318\ I_m$

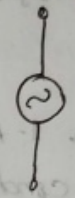
I_{rms} :- $\frac{I_m}{2}$

ripple factor = $\gamma = \frac{I_{rms}}{I_{dc}}$

Form factor = $\frac{I_{rms}}{I_{dc}} = \frac{\pi}{2} = 1.57$



d.c power supply $V_{cc} = 12\ V$



A.C power supply.
$V_i = V_m \sin t$

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Q.) A silicon diode is said to be a 1 mA device displays a forward voltage of 0.7 V at a current of 1 mA.
Evaluate the junction scaling constant I_s in the event that n is either 1 or 2.
What scaling constant would apply for 1-A diode for the same manufacture that conducts 1A at 0.7 V

Soln :- Given,

$I_D = 1\,mA$

$V_f = 0.7\,V$

$\left[\because e^{\frac{V_f}{nV_T}} >>> 1\right]$.

We know

$$I_D = I_s\left(e^{\frac{V_f}{nV_T}} - 1\right) \simeq I_s\left(e^{\frac{V_f}{nV_T}}\right)$$

$$\Rightarrow I_s = I_D \times e^{\frac{-V_f}{nV_T}}$$

$$\Rightarrow I_s = 10^{-3} \times e^{\frac{-0.7}{n \times 0.026}}$$

$I_D = 1\,mA$

$n = 1$

$$I_s = 10^{-3} \times e^{\frac{-0.7}{0.026}} = 6.9 \times 10^{-16}\,A \simeq 10^{-15}\,A$$

$n = 2$

$$I_s = 10^{-3} \times e^{\frac{-0.7}{2 \times 0.026}} = 8.3 \times 10^{-10}\,A \simeq 10^{-9}\,A$$

We need the diode ~~containing~~ conducting 1 A at 0.7 volt which correspond to ~~1000~~ 1001 mA diode. So we have to connect 1001 mA diode in parallel with total junction area 1000 times greater.

So, the I_s is also 1000 times greater.

For $I_D = 1\,A$

$n = 1$, $I_s = 6.9 \times 10^{-16}\,A \times 1000 = 6.9 \times 10^{-16}\,A = 6.9 \times 10^{-12}\,A$

$n = 2$, $I_s = 8.3 \times 10^{-10}\,A \times 1000 = 8.3 \times 10^{-10} \times 10^{3} = 8.3 \times 10^{-7}\,A$

Bridge Rectifier

The bridge type Rectifier circuit is also full wave Rectifier circuit but it uses four diodes two diode conducts during +ve half and another two diodes conducts -ve half of the Input cycle.

During +ve half D_1 & D_2 conducts & during -ve half D_3 & D_4 conducts.

output dc. voltage

$$V_{dc} = \frac{2V_m}{\pi} \text{ volt.}$$

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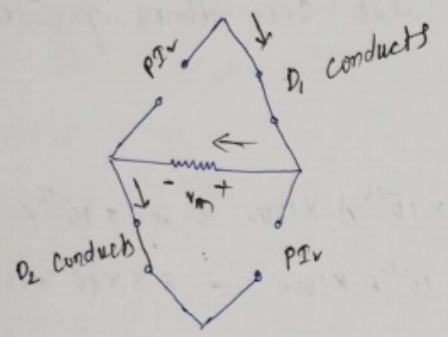
output dc. current :-

$$I_{dc} = \frac{2I_m}{\pi} = \frac{2V_m}{\pi R_L}$$

peak Inverse voltage :-



The max. PIV is required for each diode in bridge circuit rectifier is V_{max}.

Ripple factor is same as center tapped full wave rectifier i.e 0.48

Advantage of Bridge Rectifier circuit

→ The peak Inverse voltage (PIV) of each diode is only V_m as compared to the ~~center~~ PIV of center tapped rectifier circuit where it is $2V_m$

→ No center tapped is required on the tranformer.

→ It can work with output floating terminal.

Q.) Differences of Half wave Rectifier & full wave Rectifier.

	H.W.R	center tapped	Bridge Rectifier
① Diode	one	Two	Four
② Transformer	Simple	center tapped transformer	Simple.
③ PIV	V_m	$2V_m$	V_m
④ Ripple factor	1.21	0.48	0.48
⑤ Efficiency (max)	40.6 %	81.2 %	81.2 %
⑥ dc. output voltage	$\frac{V_m}{\pi}$	$\frac{2V_m}{\pi}$	$\frac{2V_m}{\pi}$

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Q What is a p-n Junction?

Ans:- The contact surface between the layers of p-type & n-type semiconductor pieces, placed together to form a p-n junction is called p-n junction.

Q Why is silicon preferred over germanium in the manufacture of semiconductor devices?

Ans:- The silicon semiconductor devices have in general, higher p.i.v and current ratings and wider temperature range than germanium semiconductor devices and therefore, silicon is preferred over germanium in the manufacture of silicon semiconductor devices.

Q What does the arrowhead represent in a schematic symbol of a p-n Junction?

Ans:- The arrowhead in the schematic symbol of a p-n junction indicates the direction of conventional current flow when the diode is forward bias.

Q How diode act as Rectifier?

Ans:- Rectifier is a device which converts the sinusoidal ac voltage into unidirectional

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Questions :- Assignment

1) What is a P-N Junction ?

Ans :- The contact surface between the layers of p-type & N-type semiconductor pieces placed together to form a P-N junction is called P-N junction.

2) Why is silicon prefered over germanium in the manufacture of semiconductor devices ?

Ans :- The silicon semiconductor devices have in general, higher PIV and current ratings and wider temperature range than germanium semiconductor devices and therefore, silicon is preferred over germanium in the manufacture of ~~silicon~~ semiconductor devices.

3) What does the arrowhead represent in a schematic symbol of a P-N Junction?

Ans :- The arrowhead in the schematic symbol of a P-N junction indicates the direction of convential current flow when the diode is forward bias.

4) How diode act as Rectifier ?

Ans :- Rectifier is a device which converts the sinusoidal ac voltage into unidirectional pulsating voltage. Diode is an electronic device consisting of two elements know as cathode and anode. since in a diode electrons can flow in only one direction i.e from cathode to anode, the diode provides the unilateral i.e from cathode to anode, the diode provides the unilateral conduction necessary for rectification. this is true for diodes of all types - vaccum, gas-filled, crystal or semiconductor diodes.

6) What is junction diode?

Ans :- Diode is a two terminal device which conducts exponentially in one direction and has a poor conduction in reverse direction. It will be an ideal case if its conduction in one direc is like a perfect insulator. ~~Ideal diode characteri~~ is

7) What is the main different betw the characteri of a simple and those of an Ideal diode ?

Ans :- the Important difference betw the characte stic of a simple switch and those of an ide diode is that an ideal diode acts like an automatic switch - the switch is closed when the diode is forward biased and is opened reverse biased.

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(8) Name the breakdown mechanism in a lightly doped p-N Junction under reverse biased condition.

Ans :- Avalanche breakdown.

(9) Name the breakdown mechanism in a heavily doped p-N junction under reverse biased condition.

Ans :- Zener breakdone.

(10) what is reverse saturation current?

Ans :- Reverse current of a diode is due to minority carriers and is caused when the diode is reverse biased. The reverse current is constant, independent of the applied reverse bias. consequently it is called the reverse saturation current.

(11) Is reverse saturation current of a junction diode independent of reverse bias voltage?

Ans :- Yes.

(12.) Germanium is more temperature dependent than silicon. why?

Ans :- Because the reverse saturation current in case of a germanium diode is approximately 1,000 times larger.

(14.) Explain the effect of temperature on the V-I characteristics of the diode.

Ans :- Reverse saturation current I_0 and volt equivalent of temperature V_T Inc. with the inc. in the temperature I_0 doubles of threshold or cut in voltages. with the increase in temp. Forward characteristic becomes more ideal. In reverse bias, the breakdown voltage increase with the increase in temperature.

(15.) what is static resistance of a diode?

Ans :- The static or dc. resistance of a diode is the resistance offered by it to the direct current. It is defined as the ratio of the diode voltage and current at the point of interest and is not sensitive to the shape of V-I Characteristic curve. It decreases with the increase in diode current voltage.

(16.) Define Dynamic resistance of a p-N junction diode in forward biased condition.

Ans :- The resistance offered by a p-N Junction diode to the changing forward current is defined as the dynamic resistance.

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It may be given as:

A.c or dynamic resistance.

$$r = \frac{\text{small change in forward voltage}}{\text{small change in forward current}}.$$

thus ac resistance of a diode is sensitive to the shape of v-I characteristic curve in the region of interest. It dec. for higher level of diode current or voltage.

(17) Explain what do you understand by the expression "linearization of a nonlinear device.

Ans:- A nonlinear device, such as a diode, has a nonlinear voltage current characteristics. In a diode v and I are related by equation.

$$I = I_0 \left(e^{v/\eta V_T} - 1\right)$$

Diode shows nonlinearity until the threshold or cutin voltage V_T is reached. voltage-current characteristics of the diode follow a linear relationship after it has attained the cutin voltage. just as for a resistance of very low magnitude. It means that diode exhibits nonlinearity for lower voltage ($v < V_T$) but linearity for voltages exceeding V_T

The equivalent circuit for the linear approximation is a constant-voltage source in series with a resistor.

(18) What is step graded junction?

Ans:- A junction is said to be step graded if there is an abrupt change from acceptor ion concentration on the p-side to donar ion concentration on the N-side such as alloyed or fused junctions.

(19) What is linear graded junction?

Ans:- A junction is said to be linearly graded if the charge concentration varies gradually with the distance in its transition region such as a growth junctions.

(20) What are two types of capacitances across P-N junction? Which of these is more important in case of forward bias?

Ans:- In a P-N junction, there are two capacitive effects which are two be considered. Thus, there are two types of capacitance namely transition or depletion region capacitance and diffusion

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capacitance. In the case of a forward bias diffusion or storage capacitance. In the case is much larger than transition capacitance.

(Q7) Define transition and diffusion capacitances.

Ans :- When p-n junction is reverse biased, the depletion ~~layer~~ region acts like an insulator or dielectric material while the p- and n-type regions on either side have a low resistance and act as the plates. Thus p-n junction may be considered a parallel plate capacitor. The junction capacitance is termed as space charge capacitance or transition capacitance or depletion region capacitance and is denoted by C_T.

When a p-n junction is forward biased, a ~~[illegible]~~ capacitance, which is much larger than the transition capacitance, comes into play. This type of capacitance is called the diffusion capacitance C_D.

(Q8) How does diffusion capacitance C_D vary with dc diode current?

Ans :- In a p-n junction diode, the diffusion capacitance is directly proportional to the

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capacitance. In the case of a forward bias diffusion or storage capacitance. In the case is much larger than transition capacitance.

(21.) Define transition and diffusion capacitances.

Ans :- When P-N Junction is reverse biased, the depletion ~~layer~~ region acts like an insulator or dielectric material while the P- and N-type regions on either side have a low resistance and act as the plates. thus P-N Junction may be considered a parallel plate capacitor. The junction capacitance is termed as space charge capacitance or transition capacitance or depletion region capacitance and is denoted by C_T.

When a P-N Junction is forward bias, a ~~capacitor~~ capacitance, which is much larger than the transition capacitance, comes into play. This type of capacitance is called the diffusion capacitance C_D.

(22.) How does diffusion capacitance C_D vary with dc diode current?

Ans :- In a P-N Junction diode, the diffusion capacitance is directly proportional to the diode forward current.

(23.) How does transition capacitance vary with junction voltage in a P-N Junction diode?

Ans :- Transition capacitance is inversely proportional to the square root of the junction voltage.

(24.) What is the relation betw the transition capacitance and reverse bias voltage in a PN diode?

Ans :- Transition capacitance $C_T = \frac{dQ}{dV}$, where dQ is the increase in charge due to increase in voltage dV.

Since, depletion region increase with the increase in

Assignment :- (2)

(1.) What is a dc power supply.

Soln :- The part of the equipment that converts ac into dc is called the dc power supply

(2.) What is meant by rectifier?

Ans :- A rectifier is a device which converts A.C into unidirectional current.

(3.) Enummerate the properties that the junction diodes designed for use as rectifier should posses.

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Ans:- Junction diodes designed for use in rectifiers should have the properties :-

① V-I characteristics as close as possible to that of an ideal.

(ii) Negligible forward resistance.

(iii) Negligible reverse current i.e large reverse resistance.

(iv) Large reverse breakdown voltage.

(v) Small offset voltage V_0 in the forward direction

(4) Define peak inverse voltage (PIV) is ~~the max~~. pos. of a diode. what is the difference betw PIV of a center tapped FWR and bridge rectifier?

Ans:- peak inverse voltage (PIV) is the ~~maximum~~ max. possible that occurs across a diode when it is reverse biased. PIV of a center-tapped FWR is double of that of bridge rectifier.

(5) What is the importance of peak inverse voltage?

Ans:- If the applied voltage in reverse biased condition exceeds peak inverse voltage (PIV) rating of the diode, then the diode may get damaged.

(6) why half-wave rectifiers are generally not used in dc power supply?

Ans:- The type of supply available from half-wave rectifier is not satisfactory for general power supply. That is why it is generally not used in dc power supply.

(7) Why diodes are not operated in the breakdown region in rectifiers?

Ans:- In breakdown region, a diode has a risk of getting damaged or burnt because the magnitude of current flowing through it increase in an uncontrollable manner. That is why diodes are not operated in the breakdown region in rectifiers.

(8) What is rectification efficiency of a full-wave rectifier?

Ans:- $\eta = \dfrac{0.812}{1 + \dfrac{2R_F}{R_L}}$, max value is 81.2%

(9) what is ripple factor?

Ans:- The ripple factor is defined as the ratio of the A.C component of the output current

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to the d.c component

$$\gamma = \frac{I_{rms}}{I_{dc}}$$

(10) What is transformer utilisation factor?

Ans:- Transformer utilisation factor is defined as the ratio of power delivered to the ~~head~~ load and a.c rating of secondary of supply power transformer.

(11) The output of 60 Hz full-wave bridge rectifier has 60 Hz ripple. Is the circuit working properly?

Ans:- A full-wave rectifier with 60 Hz input must have lowest ripple frequency equal to twice the input frequency i.e 120 Hz. If the ripple ~~factor~~ frequency is 60 Hz, it means some diodes in the circuit are not working.

(12) State the advantages of polyphase rectifiers over single phase rectifiers.

Ans:- Advantages of polyphase rectifiers over single phase rectifiers.

(i) Ripple factor dec. rapidly with an inc. in the number of phase

(ii) polyphase rectifiers give smooth direct current.

(iii) There is almost no difference in performance of a polyphase rectifier with or without filter inductance.

(13) What is meant by filter?

Ans:- Filter is a device that converts pulsating output of rectifier into a steady dc level.

Transistor

Transistor = Trans + istor

Trans signifyes the transfer property of the solid state device.

istor signifys the property of Resistor.

→ Transistor can be used as a amplifier or switch.

classification of Transistor :-

→ Transistor

- Bipolar (Both e^- & holes are responsible for current conduction)
- unipolar (either e^- or holes)

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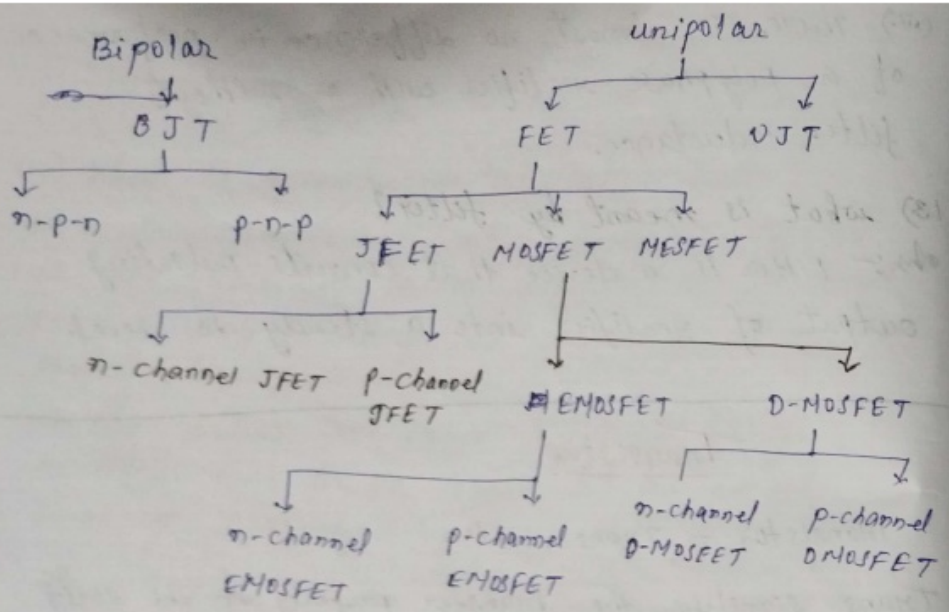


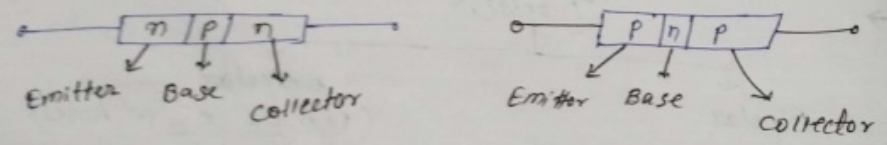
E = Enhancement type

D = Depletion type.

Transistor is a semiconductor triode.

BJT is a Bipolar Device.

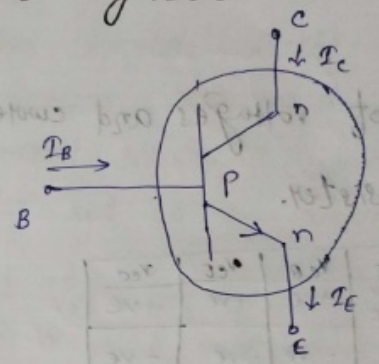
BJT are of two types.



BJT has 3 terminal.

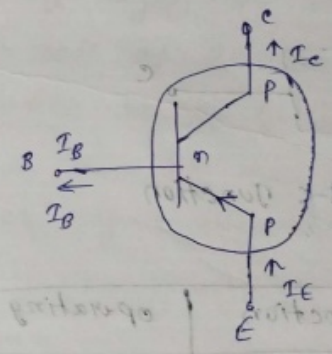
1. Emitter (E)
2. Base (B)
3. Collector (C)

circuit Symbol.



$I_E = I_B + I_C$

(npn Transistor)



(p-n-p) Transistor)

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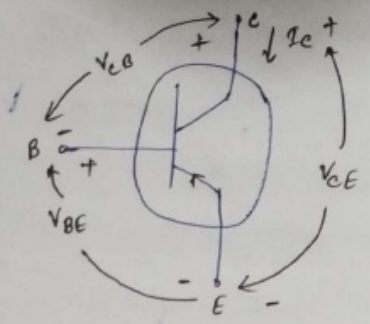


For npn transistor

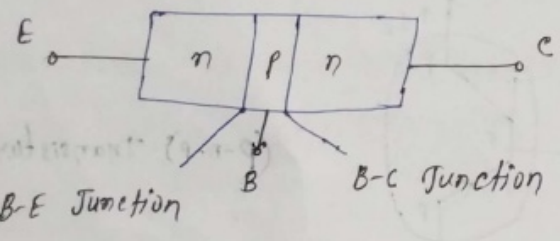
$V_{BE} = 0.7V$

p-n-p Transistor

Sign convent^n of voltages and current

→ Type of transister.

	I_E	I_B	I_C	V_{BE}	V_{CB}	V_{CE}	V_{CC}
n-p-n	-ve	+ve	+ve	0.7v +ve	+ve	+ve	+ve
p-n-p	+ve	-ve	-ve	-ve	-ve	-ve	-ve



B-E Junction	BC Junction	operating Region
F.B	R.B	Active region
R.B	R.B	cut off region
F.B	F.B	saturation region
R.B	F.B	Reverse active Inverted region

There are three operating regions in BJT.

① Active Region → The Base emitter Junction is forward Bias and base current Junction is Reverse bias. In active Region the transistor act as an amplifier.

② cut off region → In cut off region base ~~Ammeter~~ emitter Junction is R.B and base collector region is R.B. In cut off region the transistor is an off device. So its acts as an switch.

③ Saturation region :- In saturation region the Base ~~Ammeter~~ Junction is F.B and base Collector ~~region~~ Junction is F.B.

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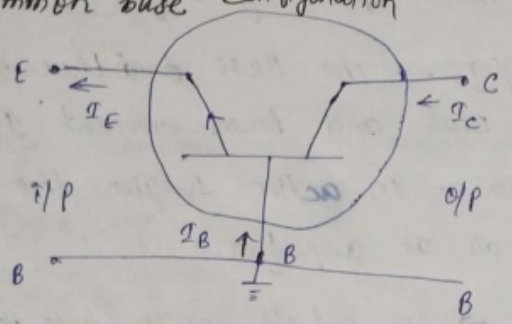
In BJT there are three configurat^n :-

(1.) Common Base (CB) configurat^n.

(2.) Common ~~Amplifier~~ Emitter (C.E) configurat^n

(3.) Common Collector (C.C) configurat^n.

(1.) Common base configuration



current gain Amplification factor $= \alpha_{dc} = \frac{I_C}{I_E}$

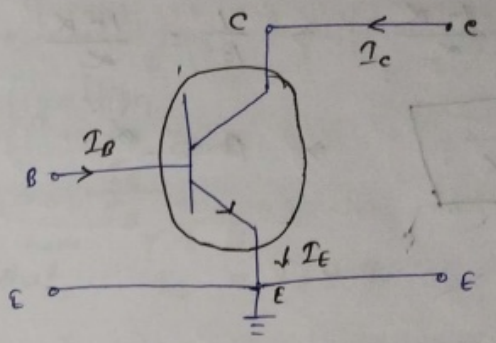
$\Rightarrow I_C = \alpha_{dc} I_E = \alpha I_E$

α value lies 0.9 to 0.99

$\boxed{I_C = \alpha I_E}$, α is the

(2.) Common Emitter configurat^n.

→ In Common Emitter Configurat^n Emitter terminal is directly grounded and emitter terminal is common to both input & output.



Current Amplificat^n factor $= \beta_{dc} = \beta = \frac{I_C}{I_B}$

$\Rightarrow I_C = \beta I_B$

β values lies bet^w 50 to 500

Relat^n bet^w α & β. $\Rightarrow \beta > \alpha$

We know,

$I_E = I_B + I_C$

and, $\alpha = \frac{I_C}{I_E}$

$\alpha = \frac{I_C}{I_B + I_C}$

$\Rightarrow I_C = \alpha (I_B + I_C)$

$\Rightarrow I_C = \alpha I_B + \alpha I_C$

$\Rightarrow I_C - \alpha I_C = \alpha I_B$

$\Rightarrow (1-\alpha) I_C = \alpha I_B$

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$\Rightarrow \frac{I_B}{I_\alpha} = \frac{1-\alpha}{\alpha} \Rightarrow \frac{1}{\beta} = \frac{1-\alpha}{\alpha}$

$\Rightarrow \boxed{\beta = \frac{\alpha}{1-\alpha}}$ $\Rightarrow \beta = \alpha$

Now,

$\beta = \frac{\alpha}{1-\alpha}$

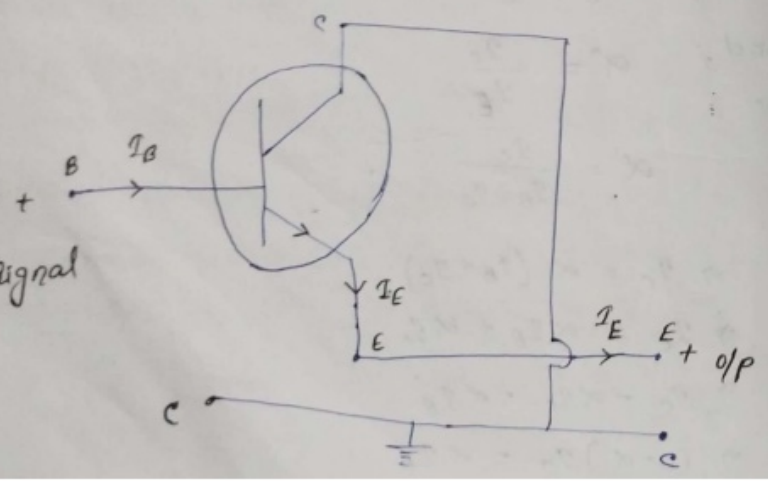
$\Rightarrow \beta(1-\alpha) = \alpha$

$\Rightarrow \beta - \beta\alpha = \alpha \Rightarrow \beta = \alpha + \beta\alpha$

$\Rightarrow \beta = \alpha(1+\beta)$

$\Rightarrow \boxed{\alpha = \frac{\beta}{\beta+1}}$

Common collector (CC) configuration :-



γ_{dc} = current gain amplificat^n factor in CC configuration.

$\gamma > \beta > \alpha$

$\gamma_{dc} = \frac{I_E}{I_B}$

Relation betw γ & β

We know that, $I_E = I_B + I_C$

$\gamma_{dc} = \gamma = \frac{I_B + I_C}{I_B} = 1 + \frac{I_C}{I_B}$

$\Rightarrow \gamma = 1 + \beta$

$\Rightarrow \frac{I_C}{I_B} = \beta$

$\Rightarrow \gamma = \gamma_{dc} = \beta_{dc} + 1 = \beta + 1$

$\gamma = \beta + 1 = \frac{\alpha}{1-\alpha} + 1 = \frac{\alpha + 1 - \alpha}{1-\alpha} = \frac{1}{1-\alpha}$

$\beta = \frac{\alpha}{1-\alpha}$

$\gamma = \frac{\beta}{\beta+1}$

In common collector (CC) configurat^n

The voltage gain is nearly equal to 1 or less than unity.

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when in common collector configurat^n the voltage gain is 1 the output follows the Input signal. That's why c.c configurat^n is also known as Emitter follower circuit.

$\gamma = 51$ to 501

Among the three configurat^n C_B, C_E & CC CE is preferable.

As both voltage gain & current gain are high in this configuration.

Biasing circuit.

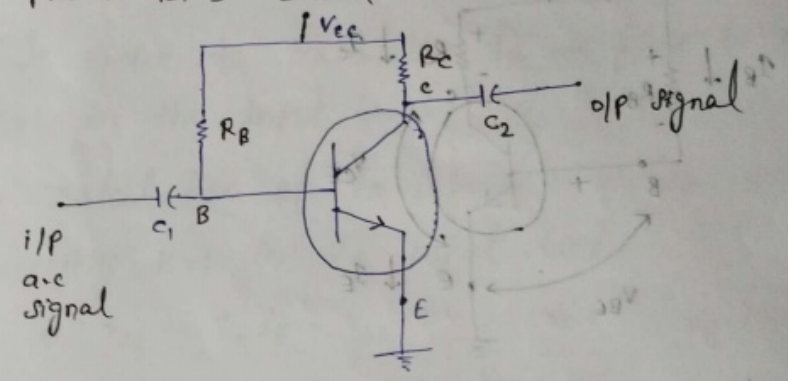
1. Fixed Bias circuit.
2. Emitter stablized (self) Bias circuit.
3. Voltage divider Bias circuit.
4. Voltage feedback Bias circuit.

Biasing is the process to apply d.c voltages to establish a fixed level of current & voltage. The biasing circuit can be design to set the device ~~locat^n~~ operat^n at the operating point with in the active region.

So, that the transister will do the faithful emplificat^n.

Biasing means D.C Analysis.

1. Fixed Bias circuit.



The capacitor will not allow d.c signal because dc signal frequency is zero.

→ Biasying is the process of appaging a fixed d.c voltage in order to make base emmiter junct^n forward bais and base collector junct^n reverse bias for getting the faithful ammplificat^n

→ Biasing is requared to set the operating point in betw the middle of the active region or load line.

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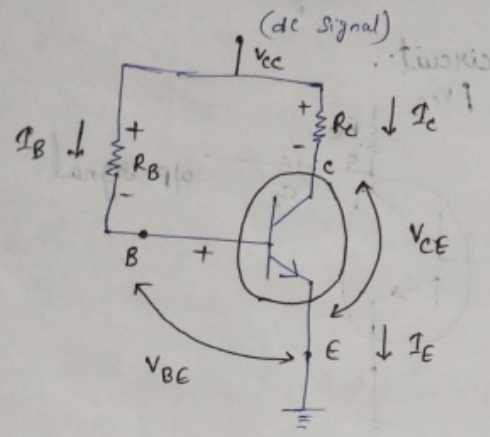
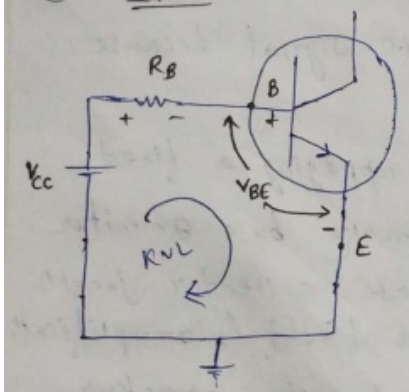
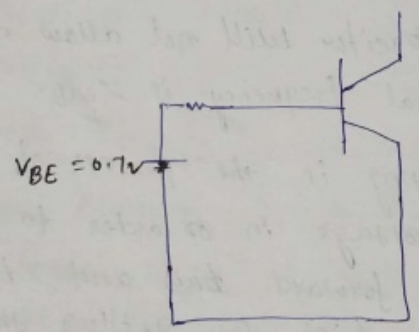
→ To stabilize the collector current against temp. variation.

→ The operating point is made independent of the transister parameter such as β.

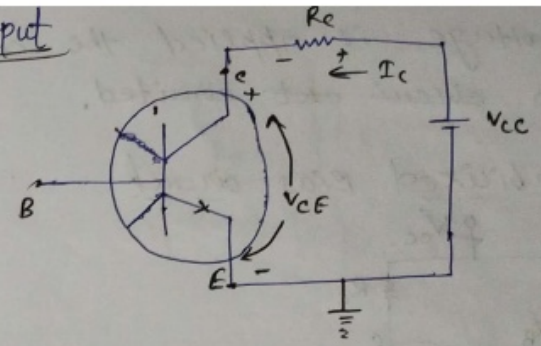


Input





output



→ In order to calculate I_B we have to apply KVL in the input loop.

calculation of I_B,

Applying KVL in the input loop.

$\Rightarrow V_{cc} - I_B R_B - V_{BE} = 0$

$\Rightarrow I_B R_B = V_{cc} - V_{BE}$

$\Rightarrow \boxed{I_B = \frac{V_{cc} - V_{BE}}{R_B}}$

where V_{cc} is fixed, V_{BE} is fixed, R_B is fixed so that I_B is fixed.

Applying KVL in output loop., for calculn of I_c

$\Rightarrow V_{cc} - I_c R_c - V_{CE} = 0$

$\Rightarrow I_c R_c = V_{cc} - V_{CE}$

$\Rightarrow \boxed{I_c = \frac{V_{cc} - V_{CE}}{R_c}}$

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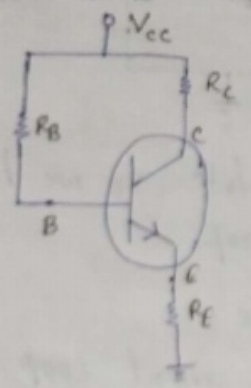
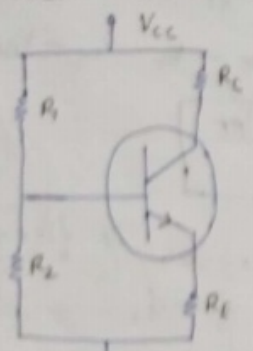
* When d.c voltage is applied the capacitor become open ~~circui~~ ~~cut~~ circuited.

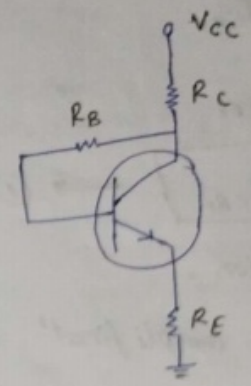
Emitter stabilized Bias circuit.



Voltage Divider Bias circuit.



Voltage Feedback biasing circuit.



c. gain & v. gain > 1
so c.e is preferable

BJT is a bipolar device. Bipolar means Both majority & minority charge carriers are responsible for current conduction.

In CB configuration.

α = current gain amplificatn factor

$$I_C = \alpha I_E + I_{CBO}$$

αI_E → majority charge carrier

I_{CBO} → Leakage current due to minority charge carriers.

CBO → Collector to Base with Emitter open.

I_{CBO} → collector to Base current with Emitter open (Leakage current)

$$I_C = \alpha I_E + I_{CBO}$$

$$\because I_C = \alpha (I_B + I_C) + I_{CBO}$$

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$$S = S_{I_{CO}} = \frac{\partial I_C}{\partial I_{CO}}\Big|_{\beta,\, V_{BE} = \text{const}}$$

$$S = S_\beta = \frac{\partial I_C}{\partial \beta}\Big|_{I_{CO},\, V_{BE} = \text{const}}$$

$$S = S_{V_{BE}} = \frac{\partial I_C}{\partial V_{BE}}\Big|_{I_{CO},\, \beta = \text{const}}$$

↳ Leakage current

Assignment.

① What is Biasing? Why it is required.

Ans:- Biasing :- Biasing is the process to apply d.c voltage to Establish fixed level of current or voltage.

→ It is required to active the transistor.

② What is stability factor?

Ans:- Stability factor (S) :- The rate of change of collector current w.r.t change in any one of the factors (I_{CO}, β, V_{BE}) while others two remaining const.

The rate of change of collector current w.r.t rate of change of reverse saturation current is called stability factor.

$$S = S_{I_{CO}} = \frac{\partial I_C}{\partial I_{CO}}\Big|_{\beta,\, V_{BE} = \text{const}}$$

$$S = S_\beta = \frac{\partial I_C}{\partial \beta}\Big|_{I_{CO},\, V_{BE} = \text{const}}$$

$$S = S_{V_{BE}} = \frac{\partial I_C}{\partial V_{BE}}\Big|_{\beta,\, I_{CO} = \text{const}}$$

BJT (Bipolar Junction Transistor) characteristics

→ ① Bipolar Junction transistor was invented by William Schokley. Bartain and Bardeen.

② current flows both due majority and minority caries that's why called bipolar device.

③ It is a current controlled device (CCD)

④ Noisy device due to presence of minority carriers.

⑤ Thermal stability is lesser because of leakage current or reverse saturation current.

⑥ Doping is emitter is highest and in base it is lowest.

⑦ Area of collector is highest and in base it is lowest.

⑧ Transistor action take place in base region.

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Mode of operation

Mode	J_E	J_c	property	Application
Saturation	F.B	R.B	very low resistance	'ON' switch
Cut-off	R.B	R.B	very high resistance	'OFF' switch
Active	F.B	R.B	Excellent transistor action	Amplifier
Reverse Active	R.B	F.B	poor transistor action	Attenuator

current in BJT

- Collector current in transistor is given by

$$\boxed{I_c = \beta I_B + (\beta+1) I_{co}}$$

This eqn is valid in active region.

$\beta \rightarrow$ current gain of common emitter.

- power dissipation in a transistor is given by

$$\boxed{P_T = |I_c| \times |V_{CE}|}$$

where, $I_c \rightarrow$ collector current

$V_{CE} \rightarrow$ collector to emitter voltage.

- Emitter cut off current I_{CBO} is given by

$\boxed{I_{CBO} = I_{co}}$ but actually it is slightly greater than I_{co}

- Base cut off current I_{CEO} is given by

$$\boxed{I_{CEO} = (\beta+1) I_{co}}$$

$I_{co} \rightarrow$ Reverse saturation current across Reverse.

current gain :-

- current gain of common base α is given by

$$\boxed{\alpha = \left|\frac{I_c}{I_E}\right| = \frac{\beta}{\beta+1}}$$

$\beta \rightarrow$ current gain of common emitter.

- β in terms of α is given by $\boxed{\beta = \frac{\alpha}{1-\alpha}}$

- current gain of common collector γ is given by

$$\boxed{\gamma = \beta+1 = \frac{1}{1-\alpha}}$$

Note :- β for d.c ~~voltage~~ analysis is greater than β for a.c analysis i.e $\boxed{\beta_{dc} > \beta_{ac}}$ or $\boxed{h_{FE} > h_{fe}}$

- Emitter injection efficiency γ_E is given by

$$\boxed{\gamma_E = \frac{i_{Ep}}{i_{Ep} + i_{En}}}$$

for p-n-p transistor

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$$\boxed{\gamma_E = \frac{i_{En}}{i_{Ep} + i_{En}}}$$ for n-p-n transistor

i_{Ep} → Emitter current due to holes.

i_{En} → Emitter current due to electrons.

- Base transport factor B is given by.

$$\boxed{B = \frac{i_c}{i_{Ep}}}$$ for p-n-p transistor

$$\boxed{B = \frac{i_c}{i_{En}}}$$ for n-p-n transistor.

- current gain α in terms of γ_E and B is given by $\boxed{\alpha = B\gamma_E}$

Value of γ_E and B is very close to 1 and in ideal conditions it is 1.

- In a diffusion transistor base current is only due to diffusion.
- In a drift transistor base current is due to both diffusion and drift phenomenon.
- Recombination agent used to trap charge carriers is Gold.

Early Effect.

- ✓ Increase in depletion region width due to increase in reverse biased across collector base junction is called Early effect.
- ✓ Due to early effect effective base width decreases.
- ✓ Due to early effect α increases by little amount but β increase by a large amount.
- ✓ The effective base width offers a ~~special~~ spread resistance at high frequencies.
- ✓ Emitter junction breakdown voltage is smaller than the collector junction breakdown voltage

$$V_{BE} < V_{CE}$$

- ✓ Emitter junction breakdown is due to zener effect while collector junction breakdown is due to Avalanche effect.

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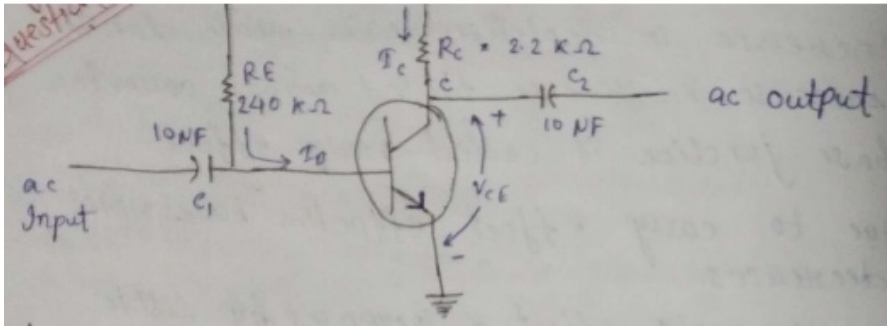


Determine saturation level for the network.

Sol^n:-

$$I_{C_{max}} = \frac{V_{CC}}{R_C} = \frac{12\,V}{2.2\,k\Omega} = 5.45\ mA$$

(a) $I_{B_0} = \dfrac{V_{CC} - V_{BE}}{R_B} = \dfrac{12V - 0.7V}{240\,k\Omega} = 47.08\ \mu A$

(Base operation)

$I_{C_0} = \beta I_{B_0} = (50)(47.08\,\mu A) = 2.35\ mA$

(Collector operation)

(b) $V_{CE_0} = V_{CC} - I_C R_C$

$= 12V - (2.35)(2.2\,k\Omega)$

$= 6.83\ V$

(c) $V_B = V_{BE} = 0.7V$

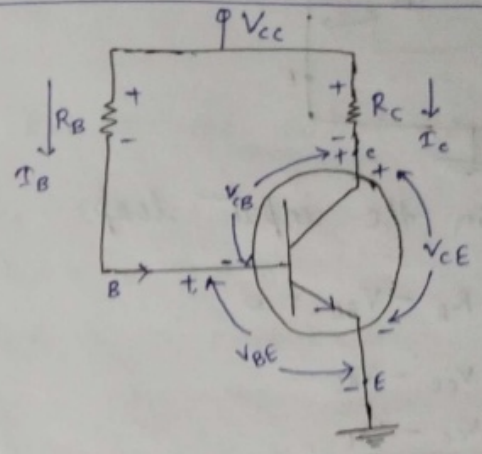
$V_C = V_{CE} = 6.83\ V$

(d) using double subscript notation yields

$V_{BE} = V_B - V_C$

$= -6.13\ V$

with the -ve sign revealing that the junction is reverse for linear amplification.



$T\uparrow,\ I_{CO}\uparrow$

$T\uparrow,\ \beta\uparrow$

$T\uparrow,\ V_{BE}\downarrow$

$V_{AB} = V_A - V_B$

$V_{BE} = V_B - V_E$

$V_{CE} = V_C - V_E$

$V_{CB} = V_C - V_B$

$I_E = I_B + I_C$

V_C = Collector to grounded potential

V_E = Emitter to grounded potential

V_B = Base to grounded potential.

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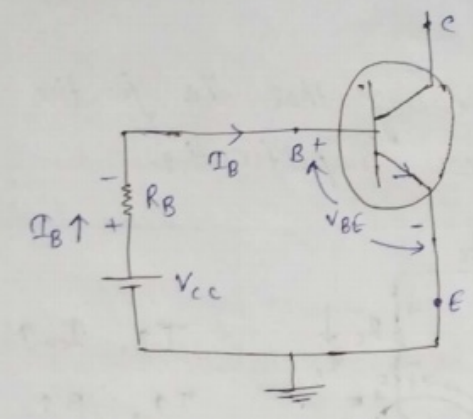
Input loop.



Applying KVL in the input loop.

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$\Rightarrow I_B R_B = V_{CC} - V_{BE}$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

V_{CC} is fixed d.c voltage

$V_{BE} = 0.7V$; also fixed.

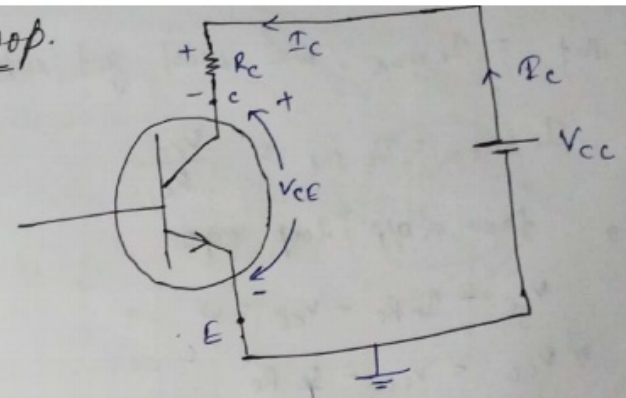
R_B = fixed Resister value so it is known as fixed bias ckt

calculat^n of I_C,

$$I_C = \beta I_B$$

calculat^n of I_E, $I_E = I_B + I_C$

Output loop.



Applying KVL in the output loop.

$$V_{CC} - I_C R_C - V_{CE} = 0$$

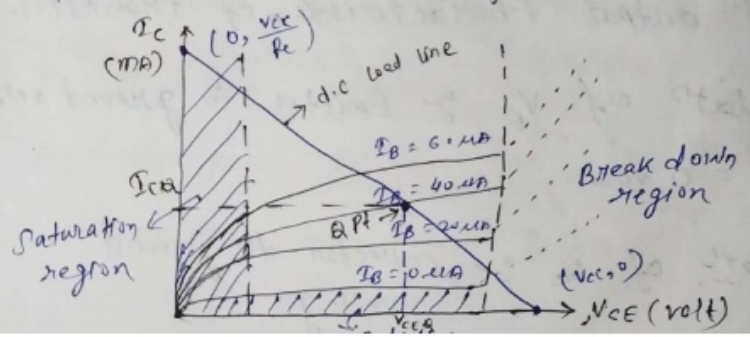
$$\Rightarrow V_{CE} = V_{CC} - I_C R_C$$

$$\Rightarrow I_C R_C = V_{CC} - V_{CE}$$

$$\Rightarrow I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

From the output loop eq^n.

$V_{CC} - I_C R_C - V_{CE} = 0$ we can draw the output characteristics of the transistor.



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$I_{C\,sat} = I_{C\,max}$, we will get when $V_{CE} = 0$ volt

$I_{C\,sat} = I_{C\,(sat)} = \frac{V_{CC}}{R_C}$

Also, from o/p loop eqn

$V_{CC} - I_C R_C - V_{CE} = 0$

$\Rightarrow V_{CE} = V_{CC} - I_C R_C$

$\Rightarrow V_{CE\,max} = V_{CE\,(cut)} = V_{CC}$

To draw a DC load line we need two point

$(V_{CE\,max}, 0)$ and $(0, I_{C\,max})$

i.e. $(V_{CC}, 0)$ & $\left(0, \frac{V_{CC}}{R_C}\right)$

Operating point or ~~quiet~~ Quiescent point :- It is defined as the intersection point of d.c load line and output characteristic curve of transistor.

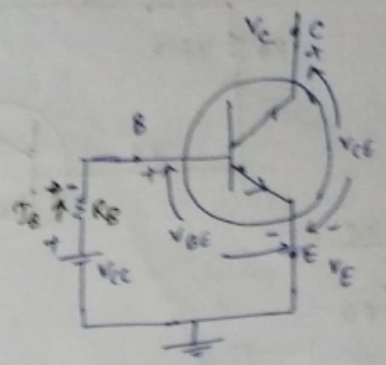
Calculat^n of V_E :- Emitter to ground volt.

$V_E = 0$ volt.

calculat^n of V_C :- collector to ground voltage

$V_C - V_{CE} = 0$

$\Rightarrow \boxed{V_C = V_{CE}}$



calculat^n of V_B :-

$V_B - V_{BE} = 0$

$\Rightarrow \boxed{V_B = V_{BE} = 0.7V}$

other method

$V_B + I_B R_B - V_{CC} = 0$

$\Rightarrow \boxed{V_B = V_{CC} - I_B R_B}$

In the output loop eqn

$V_{CC} - I_C R_C - V_{CE} = 0$

In V_{CE} axis, $I_C = 0$

In V_{CE} axis, the point is $(V_{CE} = V_{CC}, 0)$

In I_C - axis, $V_{CE} = 0$

So, the point on I_C - axis $\left(0, \frac{V_{CC}}{R_C}\right)$

as on I_C - axis, $V_{CC} - I_C R_C = 0$

$\Rightarrow I_C = \frac{V_{CC}}{R_C}$

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$I_{C\,sat} = I_{C\,max}$; we will get when $V_{CE} = 0$ volt

$I_{C\,sat} = I_{C\,sat} = \frac{V_{CC}}{R_C}$

Now, from o/p loop eqn

$V_{CC} - I_C R_C - V_{CE} = 0$

$\Rightarrow V_{CE} = V_{CC} - I_C R_C$

$\Rightarrow V_{CE\,max} = V_{CE(sat)} = V_{CC}$

To draw a d.c load line we need two point.

$(V_{CE\,max}, 0)$ and $(0, I_{C\,max})$.

i.e. $(V_{CC}, 0)$ & $(0, \frac{V_{CC}}{R_C})$

operating point or ~~quiec~~ Quiescent point :- It is defined as the intersection point of d.c load line and output characteristic curve of transistor.

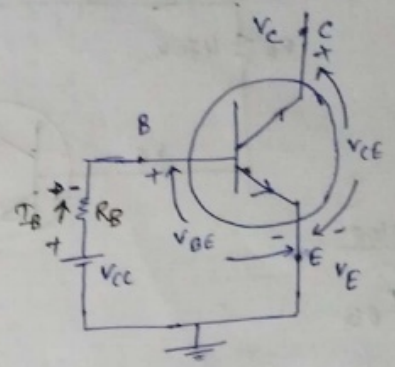
Calculat^n of V_E :- Emitter to ground volt.

$V_E = 0$ volt.

calculat^n of V_C :- collector to ground voltage

$V_C - V_{CE} = 0$

$\Rightarrow \boxed{V_C = V_{CE}}$



calculat^n of V_B :-

$V_B - V_{BE} = 0$

$\Rightarrow \boxed{V_B = V_{BE} = 0.7V}$

other method

$V_B + I_B R_B - V_{CC} = 0$

$\Rightarrow \boxed{V_B = V_{CC} - I_B R_B}$

In the output loop eqn

$V_{CC} - I_C R_C - V_{CE} = 0$

In V_{CE} axis, $I_C = 0$

In V_{CE} axis, the point is $(V_{CE} = V_{CC}, 0)$

In I_C - axis, $V_{CE} = 0$

So, the point on I_C - axis $(0, \frac{V_{CC}}{R_C})$

as on I_C - axis, $V_{CC} - I_C R_C = 0$

$\Rightarrow I_C = \frac{V_{CC}}{R_C}$

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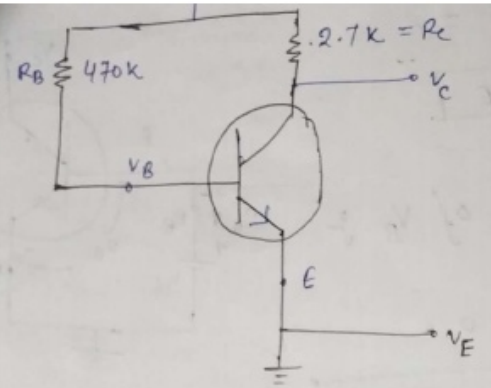
Problem



Determine

(a) I_{BQ}

(b) I_{CQ}

(c) V_{CCQ}

(d) V_C

(e) $V_B = 0.7V$

(f) V_E

$I_B \rightarrow \mu A$

$I_C \rightarrow mA$

Soln :- (a) $I_{BQ} = \dfrac{V_{CC} - V_{BE}}{R_B}$

$= \dfrac{16 - 0.7}{470k\Omega} = \dfrac{15.3V}{470k\Omega} = 32.55\mu A$

(b) $I_{CQ} = \beta I_{BQ} = (90)(32.55)\mu A = 2.93\ mA$

(c) $V_{CEQ} = V_{CC} - I_{CQ} R_C = 16V - (2.93\ mA)(2.7k\Omega)$

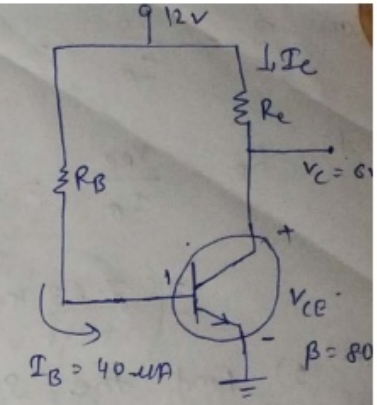
$= 8.09\ V$

(d) $V_C = V_{CEQ} = 8.09\ V$

(e) $V_B = V_{BE} = 0.7V$

(f) $V_E = 0V$

② Soln :- $I_C = ?$, $R_C = ?$, $R_B = ?$, $V_{CE} = ?$



(a) $I_C = \beta I_B = 80(40\mu A) = 3.2\ mA$

(b) $R_C = \dfrac{V_{R_C}}{I_C} = \dfrac{V_{CC} - V_C}{I_C}$

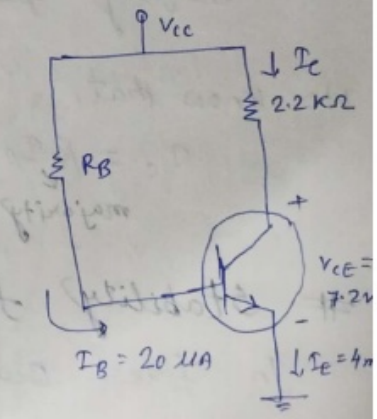
$= \dfrac{12V - 6V}{3.2\ mA} = \dfrac{6V}{3.2mA}$

$= 1.875\ k\Omega$

(c) $R_B = \dfrac{V_{R_B}}{I_B} = \dfrac{12V - 0.7V}{40\mu A} = \dfrac{11.3V}{40\mu A} = 282.5k$

(d) $V_{CE} = V_C = 6V$

③ $I_C = ?$, $V_{CC} = ?$, $\beta = ?$, $R_B = ?$



Soln; (a) $I_C = I_E - I_B$

$= 4mA - 20\mu A$

$= 3.98mA \cong 4\ mA$

(b) $V_{CC} = V_{CE} + I_C R_C$

$= 7.2V + (3.98\ mA)(2.2k\Omega)$

$= 15.96V \cong 16V$

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(c.) $\beta = \frac{I_C}{I_B} = \frac{3.98\ mA}{20\ \mu A} = 199 \cong 200$

(d.) $R_B = \frac{V_{RB}}{I_B} = \frac{V_{CC} - V_{BE}}{I_B} = \frac{15.96V - 0.7V}{20\ \mu A}$

$= 7.63\ k\Omega$

(5.) Find the saturation current (I_{Csat}) for the fixed-bias configuration

Sol^n: $I_{Csat} = \frac{V_{CC}}{R_C} = \frac{16V}{2.7k\Omega} = 5.93\ mA$.

Biasing means d.c analysis.

Stability factor - $S = \left.\frac{\partial I_C}{\partial I_{CO}}\right|_{\beta,\ V_{BE} = const.}$

We know that,

$I_C = \beta I_B + (\beta+1) I_{CO} \longrightarrow (1)$

β → majority, $(\beta+1)$ → minority charge

Stability factor of fixed Bias circuit.

In fixed Bias ckt, $I_B = \frac{V_{CC} - V_{BE}}{R_B}$ = fixed value.

Differentiating eq^n (1) w.r.t I_{CO}

$$\frac{\partial I_C}{\partial I_{CO}} = \frac{\partial}{\partial I_{CO}}\left(\beta I_B + (\beta+1) I_{CO}\right)$$

$$= \frac{\partial(\beta I_B)}{\partial I_{CO}} + \frac{\partial((\beta+1) I_{CO})}{\partial I_{CO}}$$

$$= 0 + (\beta+1)\times 1 = \boxed{\beta+1}$$

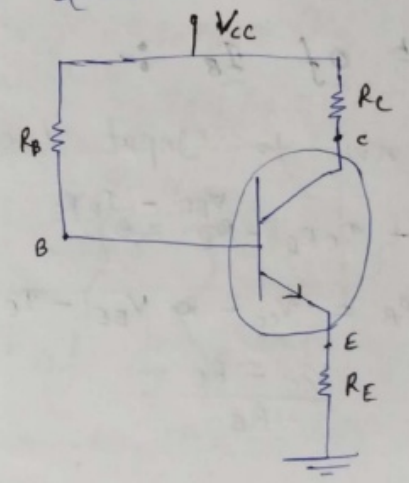
Here, β & I_B is const.

Ideal value of stability factor is 1.

The practical value of stability factor is always less than 20.

Emitter stabilized Bias circuit.

→ Here R_E Resistor is present.



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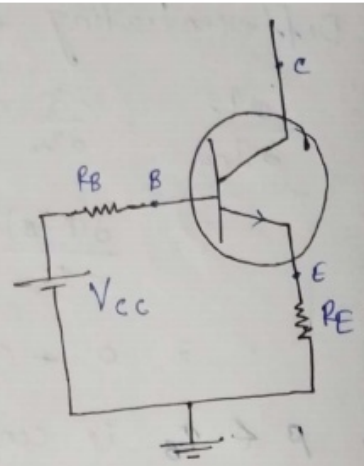
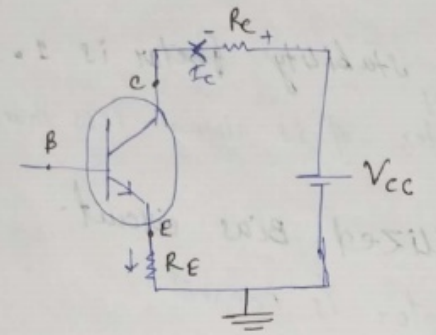
Input loop :-



output loop :-



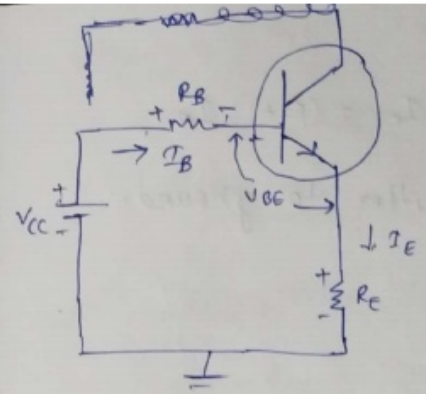
calculat^n of I_B :-

Applying KVL to Input loop

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$\Rightarrow I_B R_B = V_{CC} - V_{BE} - I_E R_E$$

$$\Rightarrow I_B = \frac{V_{CC} - R_E}{R_B}$$



$$\Rightarrow V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

we know that, $I_E = I_B + I_C$

$$= I_B + \beta I_B$$

$$I_E = (\beta+1) I_B$$

Now,

$$\Rightarrow V_{CC} - I_B R_B - V_{BE} - (\beta+1) I_B R_E = 0$$

$$\Rightarrow V_{CC} - V_{BE} = I_B R_B + (\beta+1) I_B R_E$$

$$= I_B (R_B + (\beta+1) R_E)$$

$$\Rightarrow \boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1) R_E}}$$

calculat^n of I_C :-

~~Applying KVL to output loop.~~

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$I_C = \beta I_B$

calculat^n of $I_E = I_B + I_C = (\beta+1) I_B$

calculat^n of V_E :- Emitter to ground.

$V_E - I_E R_E = 0$

$\Rightarrow V_E = I_E R_E$ volt

calculat^n of V_B :-

$V_{BE} = 0.7\,V$

$\Rightarrow V_{BE} = V_B - V_E$

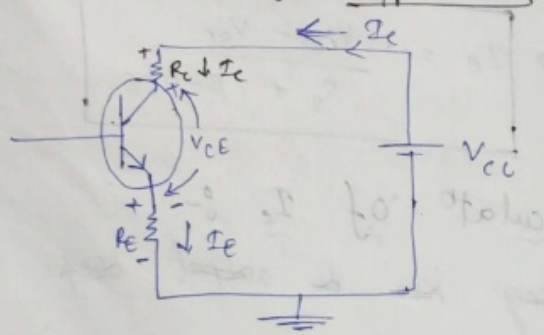
$\Rightarrow V_B = V_E + V_{BE} = V_E + 0.7V$

other method :-

$V_B - V_{BE} - I_E R_E = 0$

$\Rightarrow V_B = V_{BE} + I_E R_E = V_{BE} + V_E$

calculat^n of V_{CE} :- output loop



Applying KVL into output loop.

$\Rightarrow V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$

$\Rightarrow \boxed{V_{CE} = V_{CC} - I_C R_C - I_E R_E}$

calculat^n of V_C :- collector to ground.

$V_C - V_{CE} - I_E R_E = 0$

$\Rightarrow V_C = V_{CE} + I_E R_E$

other method :-

$\boxed{V_C = V_{CC} - I_C R_C}$

Transistor Load Lines :- the concept of load line is very important in understanding the working of a transistor. It is defined as the locus of operating point on the output characteristic of the transistor. It is the line on which the operating point moves when a.c signal is applied to the transistor.

DC Load Line :- The DC load line is the load line of the DC equivalent circuit defined by reducing the reactive components to zero.

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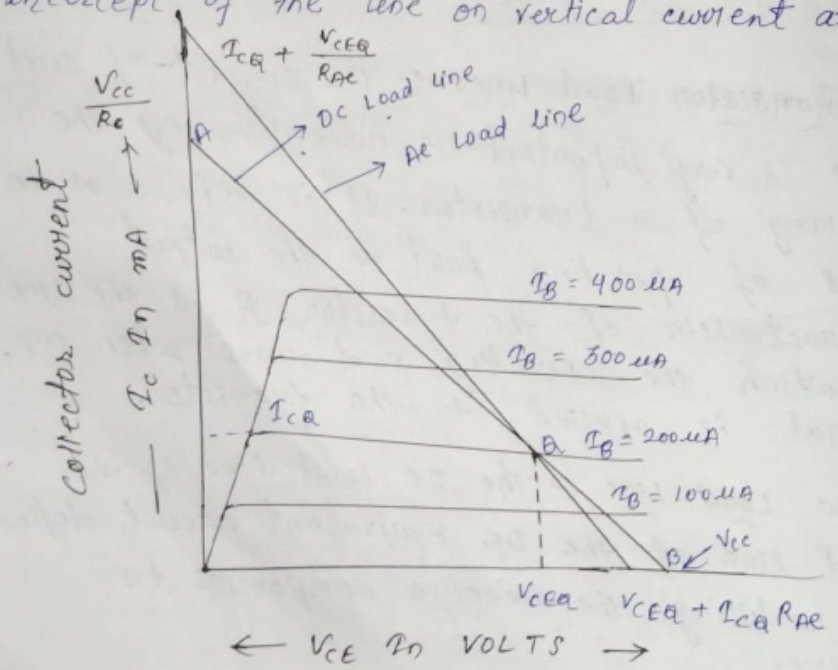
$$V_{CC} = V_{CE} + I_C R_C$$

$$\Rightarrow I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$\Rightarrow I_C = \frac{-V_{CE}}{R_C} + \frac{V_{CC}}{R_C}$$

the eqn is to be plotted on the output characteristic of the transistor, V_{CE} and I_C are variables.

Identify this eqn as $y = mx + c$ where $m = -\frac{1}{R_C}$ as the slope of the line and $I_C = \frac{V_{CC}}{R_C}$ as intercept of the line on vertical current axis



consider the following two particular situations :-

(i) when $V_{CE} = 0$, $I_C = \frac{V_{CC}}{R_C}$ ... saturatn point A

(ii) when $I_C = 0$, $V_{CE} = V_{CC}$ .... cutoff point B

By joining two points A and B, dc load line is obtained. The dc load line represents the dynamic characteristic of the device. The dc load line gives the values of collector current I_C and collector-emitter voltage V_{CE} corresponding to zero signal conditions.

Quiescent point :- It is defined as the intersection point of d.c load line & A.c load line.

AC Load Line :- When an a.c signal is applied, the transistor voltage V_{CE} and collector current I_C vary above and below the quiescent point Q. So Q is common to both dc and ac load lines. The ac load line gives the value of V_{CE} and I_C when an ac signal is applied. Collector-emitter voltage change ΔI_C and compute the corresponding collector-emitter voltage change $\Delta V_{CE} = -\Delta I_C$ to obtain another point lying on the ac load line.

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eg:- ① In CE configuration collector supply voltage $V_{cc} = 10\,V$, load resistance R_c is $8\,K\Omega$. Draw dc load line. Determine the operating point Q for zero signal if base current is $15\,\mu A$ and β is 40.

Soln:-

Collector supply voltage,

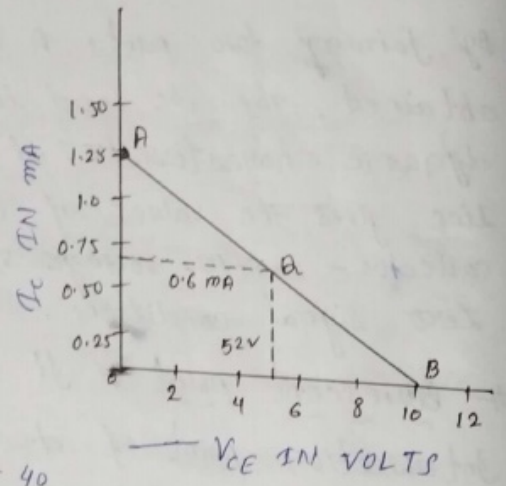
$V_{cc} = 10\,V$

Load Resistance,

$R_c = 8\,K\Omega$

Zero signal base current $I_B = 15\,\mu A$

current gain factor $\beta = 40$



collector - Emitter voltage V_{CE} is given as

$$V_{CE} = V_{cc} - I_c R_c$$

For $V_{CE} = 0$

$$I_c = \frac{V_{cc}}{R_c} = \frac{10\,V}{8\,K\Omega} = 1.25\,mA$$

this gives point A on the load line

For $I_c = 0$, $V_{CE} = V_{cc} = 10\,V$

This gives point B on the load line. AB is the required dc load line.

Zero signal collector current.

$$I_c = \beta I_B = 40 \times 15 \times 10^{-6} = 0.6\,mA$$

Zero signal collector - emitter voltage

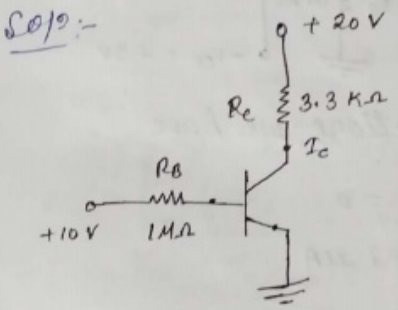
$$V_{CE} = V_{cc} - I_c R_c$$

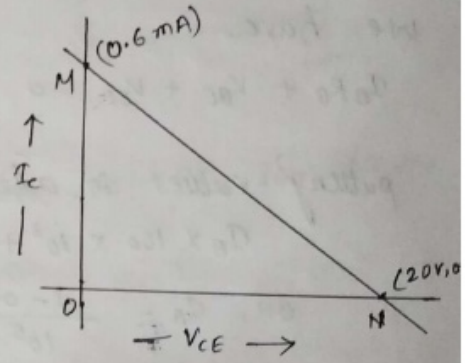
$$= 10 - 0.6\,mA \times 8\,K\Omega = 5.2\,V$$

∴ operating point Q is $(5.2\,V, 0.6\,mA)$.

eg:- ② Draw the load line for the following figure. What is I_c at saturation point? Find V_{CE} at cutoff point.

Soln:-





Soln:- Applying Kirchhoff's voltage law to be the output loop we have,

$$V_{cc} = I_c R_c + V_{CE}$$

For cutoff point, $I_c = 0$

and therefor, $V_{CE} = V_{cc} = 20\,V$ Ans

∴ For saturation point $V_{CE} = 0$

$$I_c = \frac{V_{cc}}{R_c} = \frac{20}{3.3 \times 10^{3}} = 6\,mA \text{ Ans}$$

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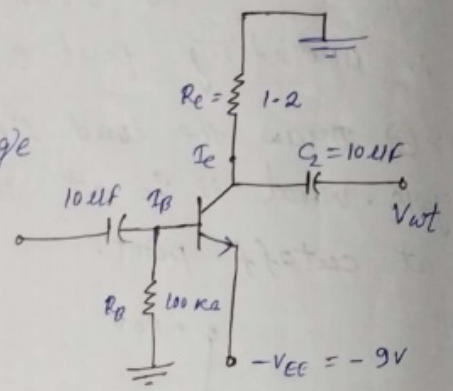
Therefor, load line ...

(20V, 0 mA) and (0V, 6mA).

eg:- ③ Determine V_c and V_B for the network given below with $\beta = 45$ and $V_{BE} = 0.7$ volt.

Sol^n:-

$\beta = 45$ and $V_{BE} = 0.7$ volt



Applying Kirchhoff's voltage law in input loop we have..

$$I_B R_B + V_{BE} + V_{EE} = 0$$

putting values in above equations we have

$$I_B \times 100 \times 10^3 + 0.7 - 9 = 0$$

$$\text{or, } I_B = \frac{9 - 0.7}{10^5} = 83\ \mu A$$

$$I_C = \beta \times I_B = 45 \times 83 \times 10^{-6}\ A = 3.735\ mA$$

collector voltage, $V_c = V_{cc} - I_c R_c$

$$= 0 - 3.735 \times 10^{-3} \times 1.2 \times 10^3$$

$$= -4.482\ V \text{ Ans}$$

$$V_B = V_{BE} + V_{EE} = 0.7 - 9 = -8.3 \text{ volts Ans}$$

eg:- ④ In the circuit shown, what should be minimum value of β such that the transistor is in saturation? Assume $V_{CE\,sat} = 0.2\ V$

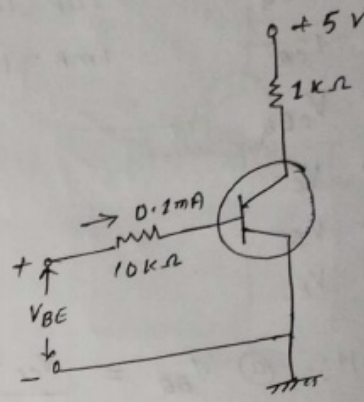
Sol^n:-

Base current $I_B = 0.1\ mA$

Base resistance, $R_B = 10\ k\Omega$

Collector resistance, $R_c = 1\ k\Omega$

Supply voltage, $V_{cc} = 5V$



Saturation collector-emitter voltage,

$$V_{CE\,sat} = 0.2\ V$$

Applying Kirchhoff's - ~~emitter~~ voltage, law to the output loop, we have,

$$V_{cc} - I_{c(sat)} R_c - V_{CE\,(sat)} = 0$$

$$\text{or, } I_{c\,(sat)} = \frac{V_{cc} - V_{CE}}{R_c} = \frac{5 - 0.2}{1 \times 10^{-3}} = 4.8\ mA$$

For transistor to be in saturation:

Base current,

$$I_B \geq \frac{I_{c\,(sat)}}{\beta}$$

$$\beta \geq \frac{I_c}{I_B} \geq \frac{4.8}{0.1} \geq 48$$

Hence minimum value of $\beta = 48$

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Extra Questions :-

(6) For emitter-stabilized bias circuit.

(a) I_{BQ}

(b) I_{CQ}

(c) V_{CEQ}

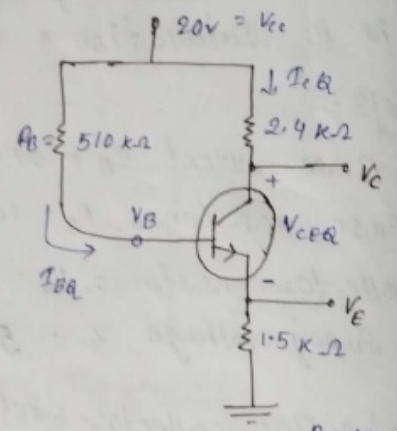
(d) V_C

(e) V_{BE}

(f) V_E

$1\mu A = 10^{-3} A$

$1mA = 10^{-4} A$



$\beta = 100$

Sol^n :- (a) $I_{BQ} = \dfrac{V_{CC} - V_{BE}}{R_B}$

$= \dfrac{20 - 0.7}{510\ k\Omega} = \dfrac{19.3V}{510\ k\Omega} = 37.84\ \mu A$

(b) $I_{CQ} = \beta I_{BQ} = (100) \times 37.84 = 3.78\ mA$

(c) $V_{CEQ} = V_{CC} - I_{CQ} R_C = 20 - (3.78\ mA) \times 2.4\ k\Omega$

$= 10.9\ V$

(d) $V_C = V_{CEQ} = 10.9\ V$

(e) $V_{BE} = 0.7V$

(f) $= 0\ V$

(7) Given the information provided.

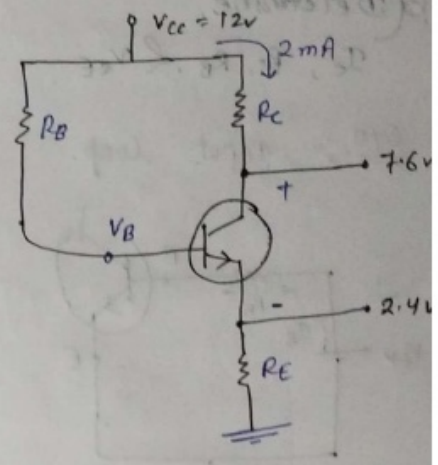
(a) R_C

(b) R_E

(c) R_B

(d) V_{CE}

(e) V_B



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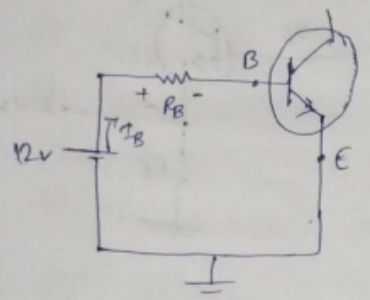
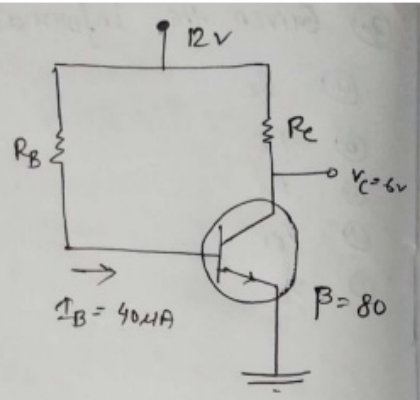
Q Determine,

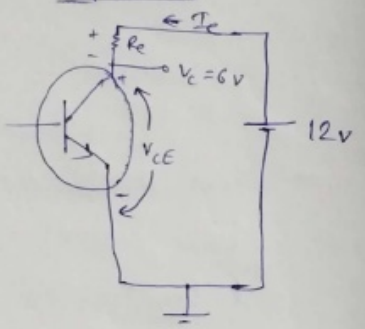
I_c, R_c, R_B & V_{CE}

Soln :- Input loop.





output loop



From output loop

$V_{cc} - I_c R_c = V_c$

$\Rightarrow 12V - I_c R_c = 6V$

$\Rightarrow I_c R_c = 12V - 6V = 6V$

Given,

$I_B = 40\mu A$.

$I_c = \beta I_B = 80 \times 40\mu A = 80 \times 40 \times 10^{-6} A$

$= 3200 \mu A$

$\boxed{I_c = 3.2 mA.}$

$\beta = \frac{I_c}{I_B}$

$\Rightarrow \boxed{I_c = \beta I_B}$

$R_c = \frac{6V}{I_c} = \frac{6V}{3.2 mA} = \frac{6}{3.2} K\Omega$

$\alpha, \beta, \gamma.$

$I_B = \frac{V_{CC} - V_{BE}}{R_B}$

$= 1.875 K\Omega$

calculation of R_B

$V_{cc} - I_B R_B - V_{BE} = 0$

$\Rightarrow 12 - I_B R_B - 0.7 = 0$

$\Rightarrow I_B R_B = 12 - 0.7 = 11.3 V$

$R_B = \frac{11.3}{I_B} = \frac{11.3}{40\mu A} = \frac{11.3}{40} \times 10^{-6} A$

$= \frac{11.3 \times 10^3}{40} K\Omega = 282.5 K\Omega$

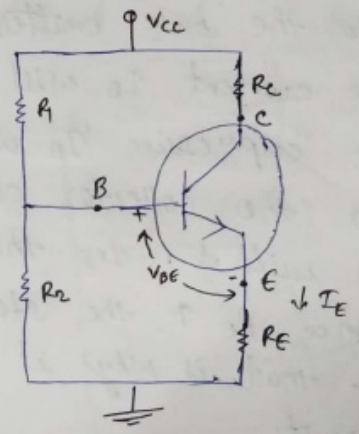
calculation of V_{CE}

$V_{cc} - I_c R_c - V_{CE} = 0$

$\Rightarrow V_{CE} = V_{cc} - I_c R_c = V_c$

$= 6V$.

Voltage Divider Biasing ckt



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In CE

$I_c = \beta I_B + (\beta+1) I_{co}$

$T\uparrow$, $I_{co}\uparrow$

$I_{co}\uparrow$, $I_c\uparrow$

$I_c\uparrow$, $I_E\uparrow$, $I_B\downarrow$

In active region of CE configuration.

$$\boxed{I_c = \underbrace{\beta I_B}_{\text{majority}} + (\beta+1) I_{co}}$$

If temperature ↑ the reverse saturation current I_{co} will ↑ for which I_c will increase. If I_c will increase then I_E will inc., If I_E will inc. then there will be more potential drop across the emitter resistor R_E which makes more reverse Bias to the base emitter junction. For which base current I_B will ~~inc.~~ dec. In the above expression I_B will ↓ β times If $I_B\downarrow$ then the collector current in the expression will ↓. In this way the emitter resistance $R_E\uparrow$ the stability of the transistor that is why it is known as self Bias circuit

The voltage divider biasing circuit can be analyse by two ways :-

(i) Exact Analysis

(ii) Approximate Analysis

(i) → In Exact Analysis we have to calculate V_{TH} & R_{TH}

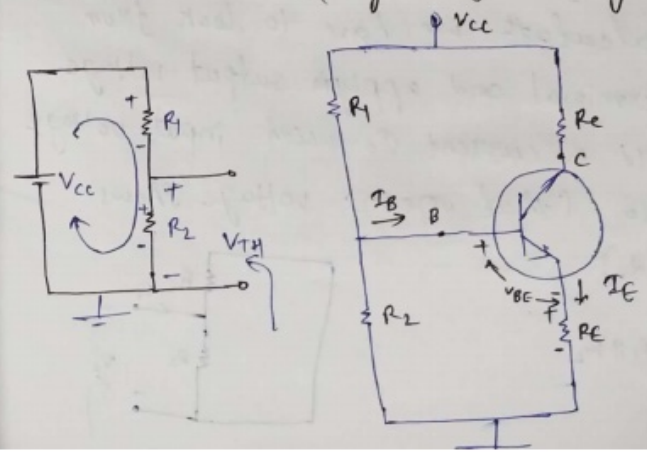
(ii) → Approximate

which satisfy the conditions.

$$\boxed{\beta R_E \geq 10 R_2}$$ (assuming $I_B \simeq 0\mu A$)

In which the current flowing through R_1 & R_2 are same.

(i) Exact Analysis of voltage divider biasing ckt



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Calculat^n of V_{TH} (V Thelmin)

→ V_{TH} is the potential drop across R_2 resistor

Let current I is flowing ~~throw~~ in the close crt

Applying KVL in the close loop

$$V_{cc} - IR_1 - IR_2 = 0$$

$$\Rightarrow V_{cc} = IR_1 + IR_2 = 0$$

$$\Rightarrow V_{cc} = I(R_1 + R_2)$$

$$\Rightarrow I = \frac{V_{cc}}{R_1 + R_2}$$

V_{TH} = potential drop across R_2 resistor $= IR_2$

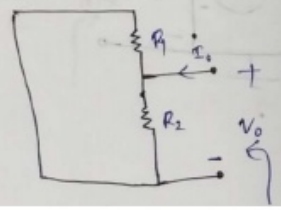
$$V_{TH} = \frac{V_{cc} R_2}{R_1 + R_2} \text{ volt.}$$

calculat^n of R_{TH}. (R. Thelmi)

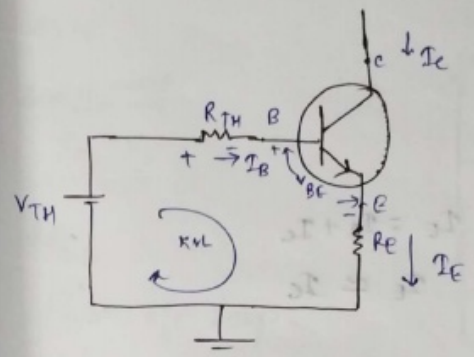
→ For R_{TH} calculat^n we have to look from the output terminal and applying output voltage V_o which resuld a current I_o with input voltage equal to Zero (that means voltage shows shot circuited.)

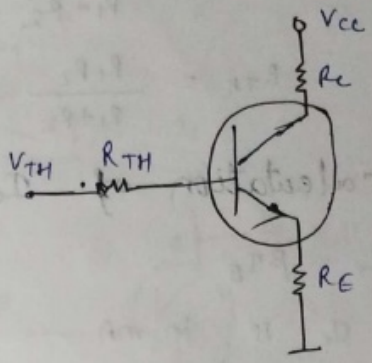
$$R_{TH} = R_{eq.} = R_1 \| R_2$$

$$= \frac{R_1 R_2}{R_1 + R_2}$$



Input loop





Applying KVL into input loop. :

$$V_{TH} - I_B R_{TH} - V_{BE} - I_E R_E = 0$$

We know $I_E = I_B + I_C$

$$= I_B + \beta I_B$$

$$I_E = I_B(1+\beta)$$

Now,

$$V_{TH} - I_B R_{TH} - V_{BE} - (\beta+1) I_B R_E = 0$$

$$\Rightarrow V_{TH} - V_{BE} = I_B R_{TH} + (\beta+1) I_B R_E$$

$$= I_B (R_{TH} + (\beta+1) R_E)$$

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta+1) R_E}$$

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where,

$$V_{TH} = \frac{V_{CC} R_2}{R_1 + R_2}$$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

calculation of I_C

$I_C = \beta I_B$

I_C is in mA

I_E is mA

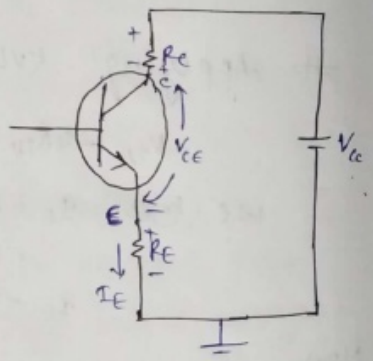
I_B is in μA

$I_E = I_B + I_C$

$I_E \simeq I_C$

Output loop :-

Applying KVL anticlock o/p. loop.



$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$

⇒ Suppose $I_C \simeq I_E$

$V_{CC} - I_C R_C - V_{CE} - I_C R_E = 0$

$\Rightarrow V_{CC} - V_{CE} = I_C R_C + I_C R_E$

$= I_C (R_C + R_E)$

$$\Rightarrow \boxed{V_{CE} = V_{CC} - I_C (R_C + R_E)}$$

calculation of V_E :-

$V_E = I_E R_E$

$V_{BE} = V_B - V_E$

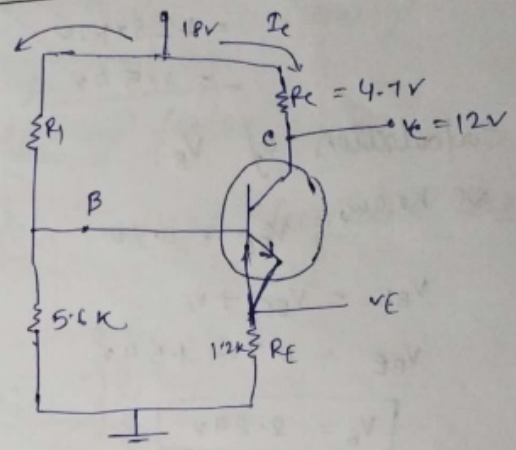
$\Rightarrow 0.7V = V_B - I_E R_E$

$$\Rightarrow \boxed{V_B = 0.7V + I_E R_E}$$

Q.17.

Determine

I_C, V_E, V_B, R_1



Soln:-

From o/p loop.

$18V - I_C R_C = 12V = V_C$

$\Rightarrow I_C R_C = 18V - 12V$

$\Rightarrow I_C R_C = 6V$

$$I_C = \frac{6V}{R_C} = \frac{6V}{4.7K} = \frac{6}{4.7} \times 10^{-3} A$$

$$I_C = \frac{6}{4.7} mA = 1.28 mA$$

(ii) we know $I_E = I_B + I_C$

$\Rightarrow I_E \simeq I_C$

$\Rightarrow I_E = 1.28 mA$

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calculation of I_E :-

$V_E - I_E R_E = 0$

$\Rightarrow V_E = I_E R_E = 1.28\,mA \times 1.2\,K\Omega$

$= 1.28 \times 1.2\,V$

$= 1.54\,V$

calculation of V_B.

we know,

$V_{BE} = 0.7\,V$

$V_{BE} = V_{BE} + V_E$

$V_{BE} = 0.7\,V + 1.54\,V$

$\boxed{V_B = 2.24\,V}$

V_B is the potential drop across resistor R_2, Here we are assuming $I_B \simeq 0$. So, the same current ~~is~~ will flow across R_1 & R_2 i.e I_E, $I_1 = I_2$

So, $V_B = I_2 \times R_2$

$\Rightarrow I_2 = V_B / R_2 = \frac{2.24}{5.6K} = \frac{2.24}{5.6K} = \frac{2.24}{5.6}\,mA = 0.4\,mA$

which is equal to I_1. i.e $I_1 = 0.4\,mA$.

calculation of R_1 :-

$18V - I_1 R_1 = V_B$

$\Rightarrow I_1 R_1 = 18V - 2.24V$

$\Rightarrow I_1 R_1 = 15.76\,V$

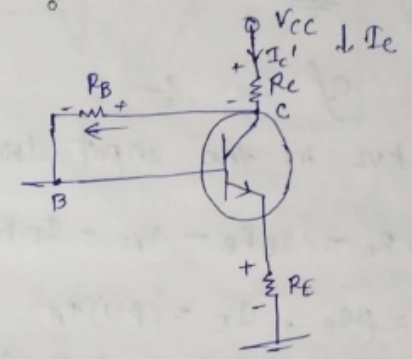
$\Rightarrow R_1 = \frac{15.76\,V}{I_1} = \frac{15.76\,V}{0.4\,mA} = \frac{15.76}{0.4}\,K\Omega$

$= 39.4\,K\Omega$

Stability factor of voltage divider Biasing circuit is 1.

$$\text{Stability} \propto \frac{1}{\text{stability factor}}$$

Base to collector voltage feedback biasing circuit :-



$R_B = R_F$ feedback Resistor connected betn collector and Base.

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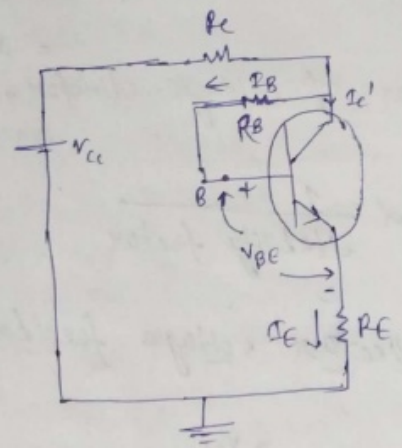
Input loop



calculation of I_B :-

→ Applying KVL in the input loop.

$$V_{CC} - I_C R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

We know, $I_C = \beta I_B$, $I_E = (\beta+1) I_B$

$$\Rightarrow V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - (\beta+1) I_B R_E = 0$$

$$\Rightarrow V_{CC} - V_{BE} = \beta I_B R_C + I_B R_B + (\beta+1) I_B R_E$$

$$\Rightarrow \quad = I_B (R_B + \beta R_C + (\beta+1) R_E)$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_C + (\beta+1) R_E} \quad ; \quad \beta+1 \simeq \beta$$

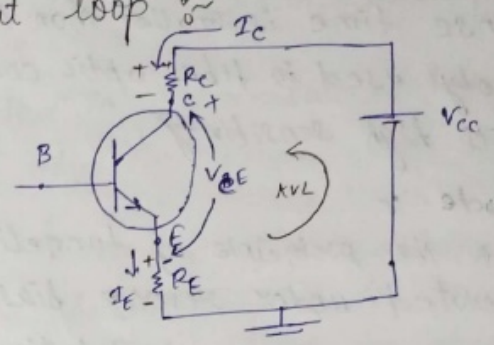
$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_C + \beta R_E}$$

$$\Rightarrow \boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta (R_C + R_E)}}$$

calculation of I_C :-

→ Assuming $I_C = I_B + I_C' = I_E$

output loop :-



Applying KVL in the output loop :-

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\Rightarrow \cancel{V_{CC} - I_C R_C = V_{CE} + I_E R_E}$$

$$\Rightarrow \text{Let } I_E \simeq I_C$$

$$\Rightarrow V_{CC} - I_C R_C - V_{CE} - I_C R_E = 0$$

$$\Rightarrow V_{CE} = V_{CC} - I_C R_C - I_C R_E$$

$$\Rightarrow \boxed{V_{CE} = V_{CC} - I_C (R_C + R_E)}$$

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Avalanche photo Diode (APD) :-

(i) Basically a photo diode along with Avalanche effect.

(ii) APD can handle large amount of power compared to PD (photo diode).

(iii) It's response time is smaller than PD.

(iv) APD is widely used in fiber optic communication because of its high sensitivity.

Zenor diode :-

(i) operates on the principle of tunneling effect.

(ii) Always operated under reverse bias.

(iii) Mainly used in voltage regulation application.

(iv) Maintains constant voltage across a load if properly biased.

photo Transistors :-

(i) Its principle of operation is photo conductive effect.

(ii) coating of photo conductive materials is done at collector base junction.

(iii) It is basically a light operated switch

(iv) n-p-n photo transistor is faster than p-n-p photo transistor.

Solar cell :-

→ It's principle of operation is photo voltaic effect.

→ We can measure terminal voltage of solar cell using voltmeter.

→ popularly used solar cells are Se cells, ~~used~~ Ni-cd cells, pbs cell.

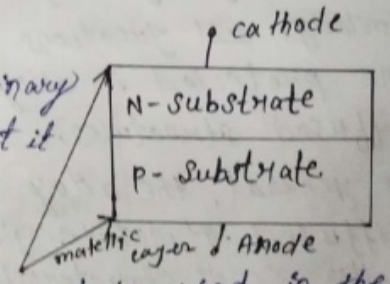
→ Ni-cd cells are rechargeable cells used in satellites

→ It is used in automatic traffic signal lightening.

→ Generally operated under open circuit condition.

Zener Diodes :- Zener diode, also sometimes called the breakdown diode, is a p-N Junction diode. specially designed for operation in the breakdown region in reverse bias condition. the diode may use either zener ~~diode~~ break down mechanism or avalanche breakdown mechanism, already discussed in detail.

construction :-



→ Zener diode is like an ordinary p-N Junction diode except that it is properly doped so as to have a sharp breakdown voltage. there are several methods used in the manufacture of Zener diodes. Such as diffused

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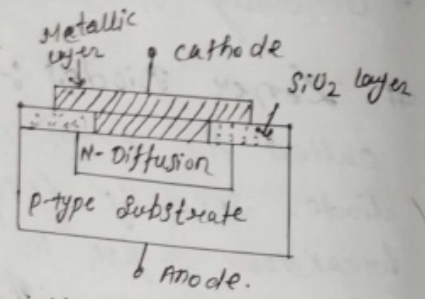
structure, diffused and passivated structure, diffused and passivated structure and alloy diffused structure, diffused and passivated structure, diffused and passivated structure and alloy diffused structure.

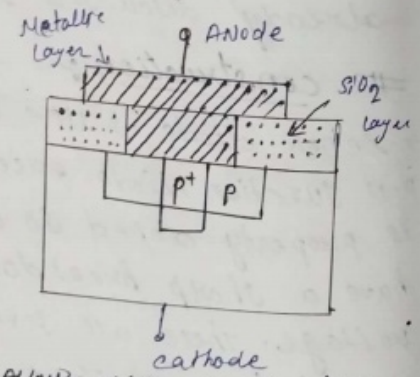
Diffused structure zener diode consists of two N- and P substrates diffused together and has metallic layers deposited on both sides to connect anode and cathode terminals as illustrated. The drawback of such a construction is that the edges of the junction are exposed to contamination.



Diffused and passivated structure of a zener diode

In passivated structure of a zener diode, the edges of a ~~zener~~ junction are covered by layer of SiO_2. Similarly, all junctions are protected in alloy diffused structures.

In general, the alloy diffused structure gives better zener characteristics at lower zener voltages. On the other hand

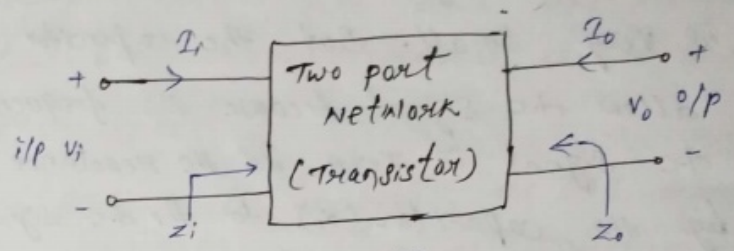


Alloy diffused structure of a zener diode

diffused and passivated zener diode is used at higher zener voltages

Small signal Analysis (AC signal Analysis)

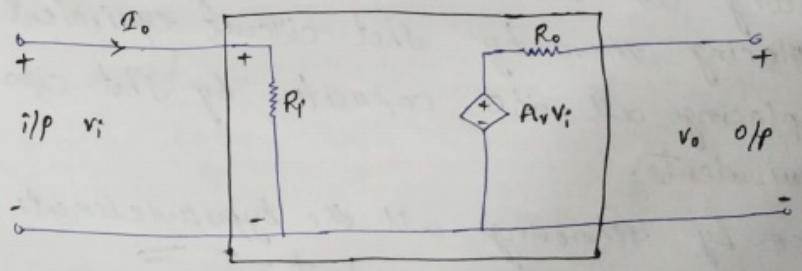
→ The 'Small' in small signal analysis indicates that the amplitude of the AC signal is very-very small and the frequency is less than 100 khz



Voltage gain $= A_V = \frac{V_o}{V_i}$

current gain $= A_I = \frac{I_o}{I_i}$

Input Impedance $= Z_i$, Z_o = output impedance



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$\Rightarrow A_v = \frac{V_o}{V_i}$ $\Rightarrow V_o = A_v V_i$

Small signal analysis is an analysis of circuit operator which permiting the use of Supper-position theorem to isolate the d.c analysis from a.c analysis.

Capacitor will allow a.c signal because the reactance offered by capacitor to the a.c signal is very small. But the capacitor will not allow d.c signal because the frequency of the d.c signal is zero. So the reactance offered by the capacitor (X_c) to the d.c signal

$$X_c = \frac{1}{2\pi f c} = \frac{1}{0} = \infty$$

In small signal analysis the following methods are to be used to obtain a.c equivalent circuit

(i) Setting all the d.c sources to zero and replacing them by short circuit equivalent.

(ii) Replacing all the capacitor by short circuit Equivalent.

(iii) ~~Rem~~ by Removing all the bypassed elements by short circuit Equivalent.

(iv) Redrawing the network in a more convient and logical form.

(v) In small signal analysis of BJT we have to determine voltage gain A_v, current gain A_i, Input impedence Z_i and output impedence Z_o using BJT small signal model. Model is a

(vi.) Model is a combination of circuit element properly choosen that best approximate the actual behiviour of a semiconductor device under specific operating condition.

(vii) In BJT small signal analysis, the BJT ~~Signal~~ symbols will be replace by BJT small signal model.

BJT small signal model :-

(i) r_e-model
(ii) h-model
(iii) hybrid-π model

r_e-model :-

$$r_e = \frac{26\,mV}{I_E}$$

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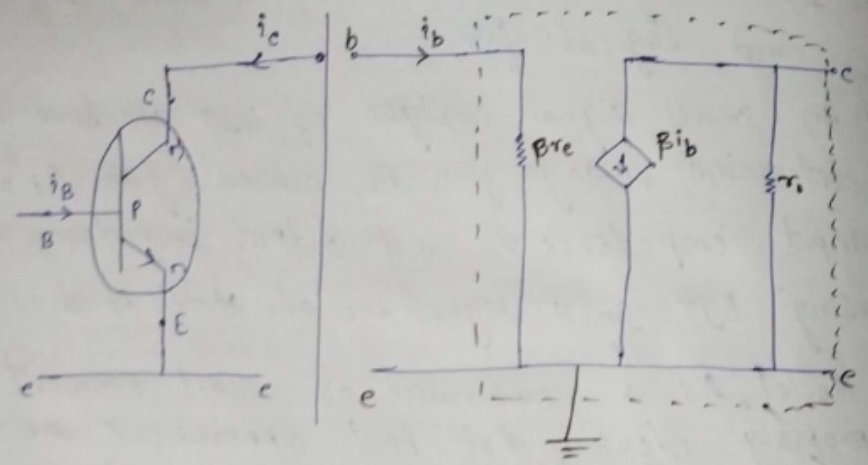
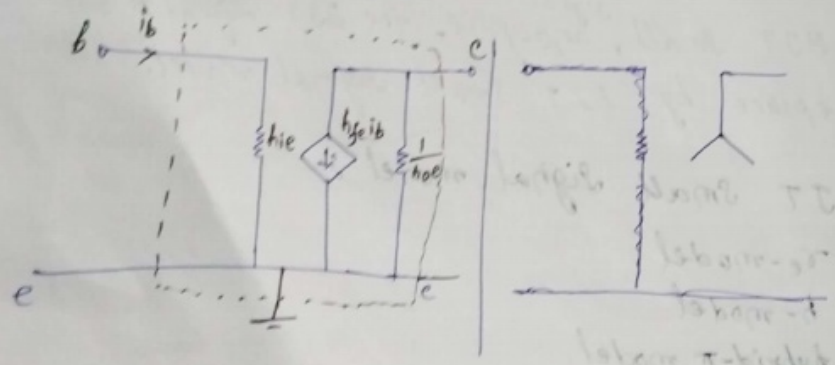


re model of npn transistor in CE configuration.

Approximate h-model.

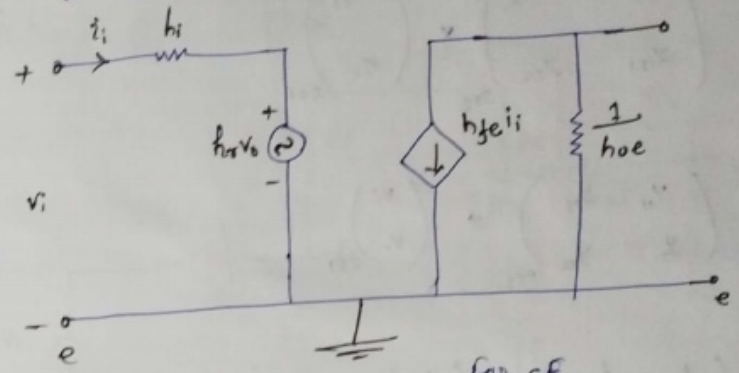


$h_{ie} = \beta r_e$

$\Rightarrow \beta i_b = h_{fe} i_b \Rightarrow \boxed{\beta = h_{fe}}$

$$\boxed{r_o = \frac{1}{h_{oe}}}$$

Exact h-model

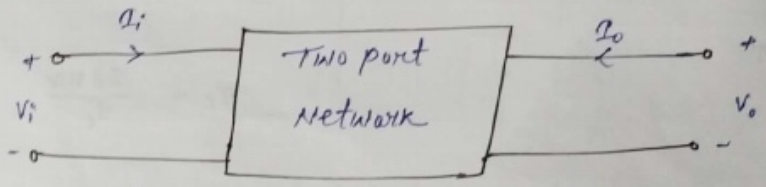


i → Input
r → Reverse
f → forward.
o → output.

For CE
h-parameter: h_{ie}, h_{re}, h_{fe}; h_{oe}

For CB
h-parameter: h_{ib}, h_{rb}, h_{fb}, h_{ob}

for CC
h-parameter: h_{ic}, h_{rc}, h_{fc}, h_{oe}.



four variables I_i, V_i, V_o, I_o

In Two port Network to determine the parameters we have to take two variables as independent variables and other two are dependent variables.

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$$\begin{pmatrix} V_i \\ V_o \end{pmatrix}_{2\times1} = \begin{pmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{pmatrix}_{2\times2} \times \begin{pmatrix} I_i \\ I_o \end{pmatrix}_{2\times1}$$

$$\begin{pmatrix} I_i \\ I_o \end{pmatrix}_{2\times1} = \begin{pmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{pmatrix}_{2\times2} \times \begin{pmatrix} V_i \\ V_o \end{pmatrix}_{2\times1}$$

$$\begin{pmatrix} V_i \\ I_o \end{pmatrix} = \begin{pmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{pmatrix} \times \begin{pmatrix} V_o \\ I_i \end{pmatrix}$$ hybrid parameter

AC analysis

$Z_i = V_i / I_i$

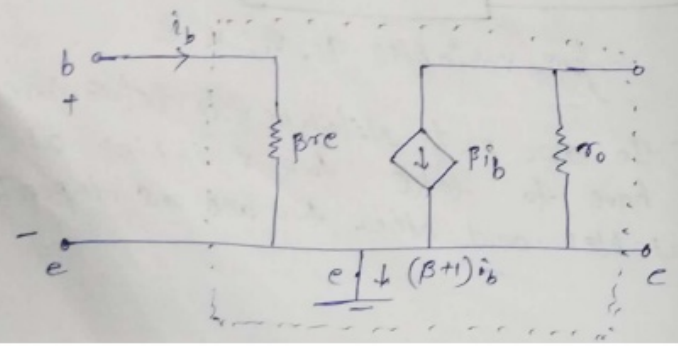
$Z_o = V_o / I_o$

$A_v = V_o / V_i$

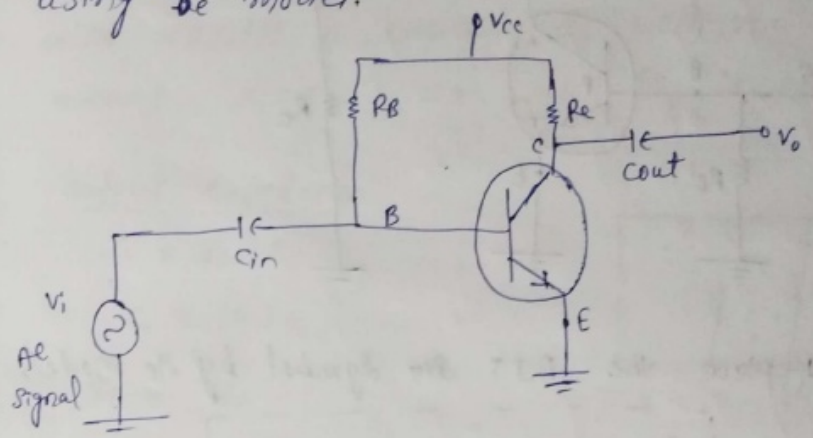
$A_i = I_o / I_i$

$r_e = \frac{26\,mV}{I_E}$

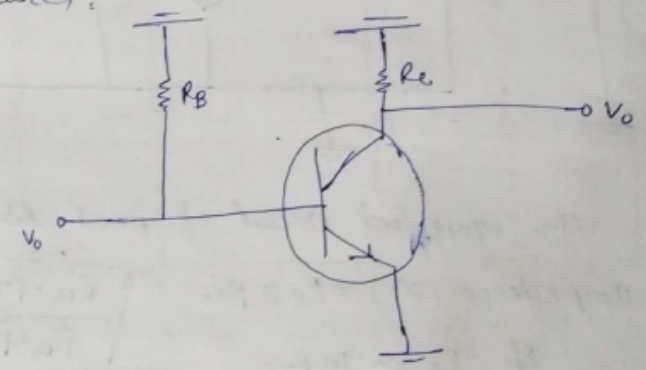
gain $= \frac{o/p}{i/p}$



The small signal analysis of fixed bias circuit using r_e model.



Step 1 :- Set D.C. voltage to zero and capacitor short circuited.



Step 2 :-

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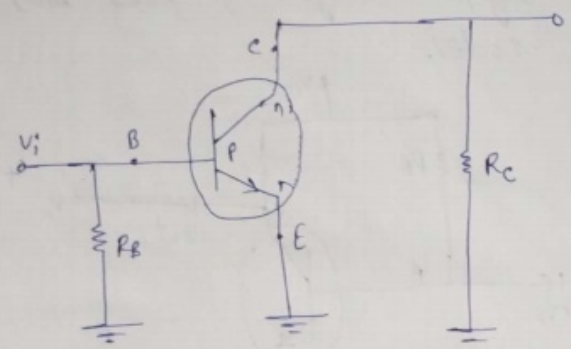
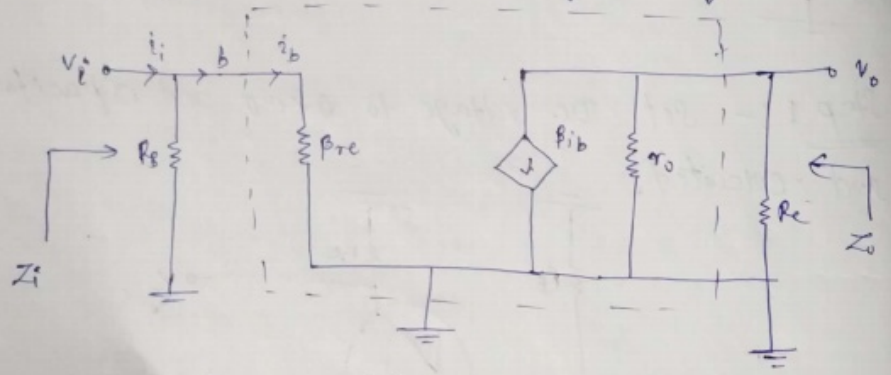


Step 3:- Replace the BJT ~~Sin~~ Symbol by re model.



a.c equivalent circuit of fixed Bias circuit.

Input Impedence (Z_i) $= R_B \parallel \beta r_e$ $\boxed{\dfrac{R_B \cdot \beta r_e}{R_B + \beta r_e}}$

If $R_B \geq 10\,\beta r_e$

$Z_i = R_B \parallel \beta r_e \simeq \beta r_e$

output Impedence (Z_o)

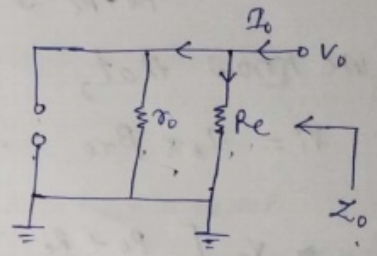
output inpedence calculation we have to apply an output voltage V_o at the output terminal which results a current I_o with V_i = zero (0) means, $V_i = 0$, $i_b = 0$, then βi_b is open circuited.

output Impedence

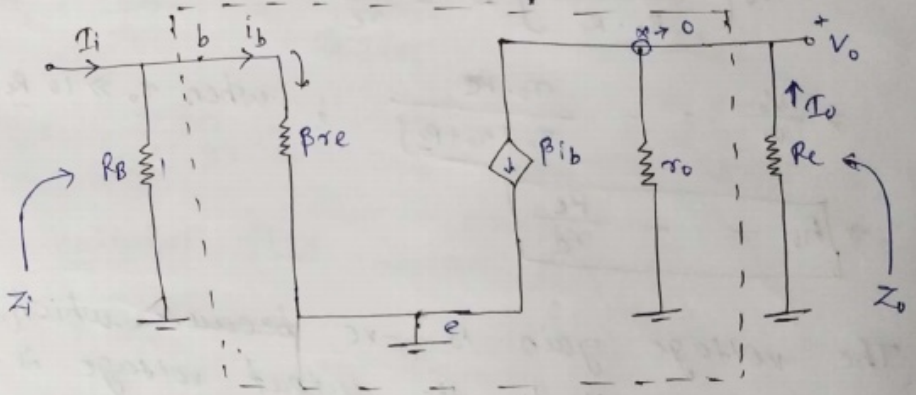
$Z_o = r_o \parallel R_e$

$r_o \geq 10\,R_e$

$Z_o = R_e$



calculation of $A_v = \dfrac{V_o}{V_i}$



$A_V = \dfrac{V_o}{V_i}$, $\boxed{V_i = I_b \times \beta r_e}$

Applying Nodel eqn :-

$$\beta i_b + \frac{V_o - 0}{r_o} + \frac{V_o - 0}{R_e} = 0$$

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$$\Rightarrow \beta I_b + \frac{V_o}{R_o} + \frac{V_o}{R_e} = 0$$

$$\Rightarrow V_o\left[\frac{1}{R_o} + \frac{1}{R_e}\right] = -\beta I_b$$

$$\Rightarrow V_o\left[\frac{R_o + R_e}{R_o + R_e}\right] = -\beta I_b$$

We know that,

$$V_i = I_b \times \beta r_e \Rightarrow I_b = \frac{V_i}{\beta r_e}$$

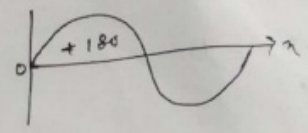
$$\Rightarrow V_o\left[\frac{R_o + R_e}{R_o + R_e}\right] = -\beta \cdot \frac{V_i}{\beta r_e}$$

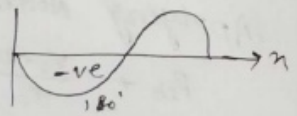
$$\Rightarrow V_o\left[\frac{R_o + R_e}{R_o \cdot R_e}\right] = -\frac{V_i}{r_e}$$

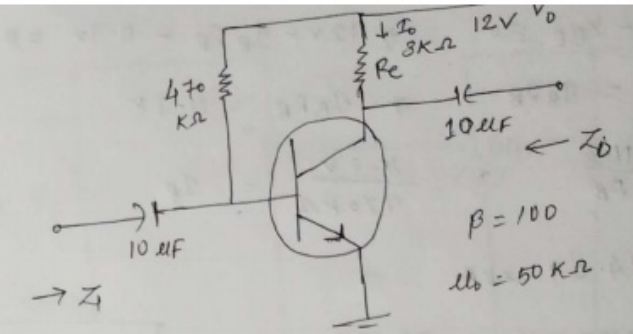
$$\Rightarrow \frac{V_o}{V_i} = -\frac{r_o \cdot R_e}{r_e[r_o + R_e]} \quad ; \text{ when } r_o \gg 10\, R_e$$

$$\Rightarrow \boxed{A_v = -\frac{R_e}{r_e}}$$

The voltage gain is -ve ~~because~~ which indicates that the output voltage is 180° phase shift with input signal.







Find:- r_e ; Z_i, Z_o, A_v, A_i

Soln:- $R_e = 3\,K\Omega$, $C_{in} = 10\,\mu F$, $C_{out} = 10\,\mu F$

$R_B = 470\,K\Omega$, $V_o = 12V$, $\beta = 100$, $r_o = 50\,K\Omega$

$$r_e = \frac{26}{I_E} = \frac{26}{I_B + I_C} = \frac{26}{I_B + \beta I_B}$$

$$= \frac{26}{I_B(1+\beta)} = \frac{26}{I_B(1+100)} = \frac{26}{I_B \cdot 101}$$

calculat^n of r_e

$$r_e = \frac{26\,mV}{I_E}, \qquad \Rightarrow I_E = 24,28.04$$

$$\boxed{I_E = 2.428\,mA}$$

We know that,

$$I_E = I_C + I_B$$

$$= \beta I_B + I_B$$

$$\Rightarrow I_E = (\beta + 1) I_B$$

$$\Rightarrow I_E = (101) \times 24.04\,\mu A$$

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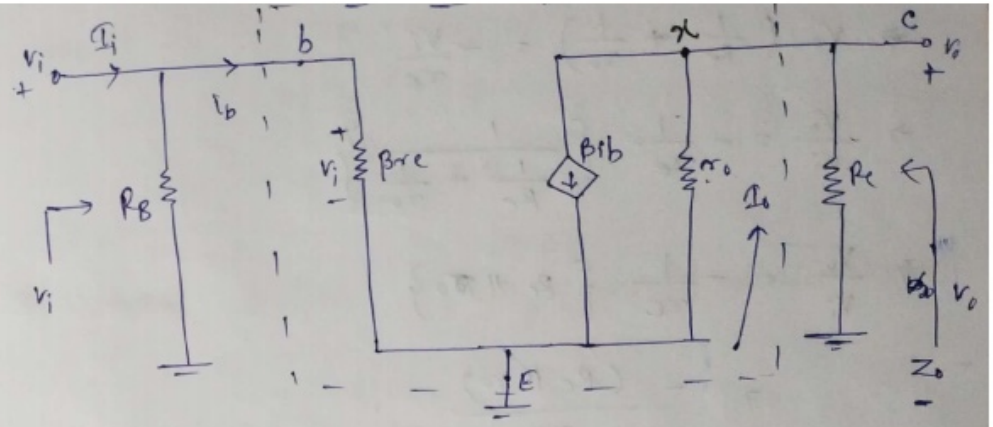
$12V - I_B R_B - V_{BE} = 0 \Rightarrow 12V - I_B R_B - 0.7V = 0$

$\Rightarrow 12 - 0.7V = I_B R_B \Rightarrow I_B R_B = 11.3V$

$\Rightarrow I_B = \frac{11.3}{R_B} = \frac{11.3V}{470K\Omega} = I_B$

$\Rightarrow I_B = 24.04\ \mu A$

$\# \ r_e = \frac{26mV}{I_E} = \frac{26\ mV}{2.428\ mA} \Rightarrow \boxed{r_e = 10.70\ \Omega}$



$Z_i = R_B \parallel \beta r_e$

$Z_o = R_o \parallel R_e$

~~#~~ voltage gain calculation (A_v)

$A_v = \frac{V_o}{V_i}$

From i/p section, $v_i = i_b \times \beta r_e$

at node x

$\Rightarrow \frac{V_o - 0}{R_e} + \frac{V_o - 0}{R_o} + \beta i_b = 0$

$\Rightarrow \frac{V_o}{R_e} + \frac{V_o}{R_o} = -\beta i_b$

$\Rightarrow V_o\left(\frac{1}{R_e} + \frac{1}{R_o}\right) = -\beta i_b$

$\Rightarrow V_o\left(\frac{1}{R_e} + \frac{1}{R_o}\right) = -\beta \times \frac{v_i}{\beta r_e}$ (As we have $v_i = i_b \times \beta r_e$ from i/p section)

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$$\Rightarrow V_o\left(\frac{1}{R_c}+\frac{1}{r_o}\right) = -\frac{V_i}{r_e}$$

$$\Rightarrow \frac{V_o}{V_i} = -\frac{1}{r_e}\left\{\frac{1}{\frac{1}{R_c}+\frac{1}{r_o}}\right\}$$

$$\Rightarrow \frac{V_o}{V_i} = -\frac{1}{r_e}\left\{R_c \parallel r_o\right\}$$

$$= -\frac{(R_c \parallel r_o)}{r_e}$$

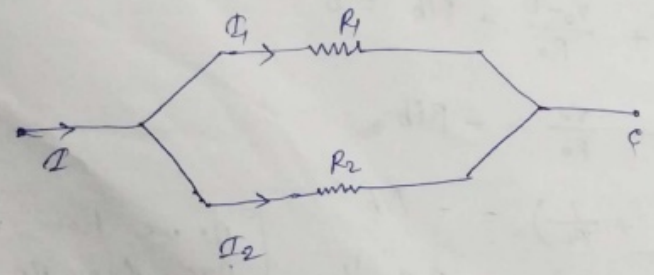
when $r_o \geq 10R_c$, $R_c \parallel r_o = R_c$

$$A_v = -\frac{1}{r_e} \times R_c \quad \text{when } r_o \geq 10R_c$$

calculation of current gain (A_I) :-

$$A_I = \frac{I_o}{I_i}$$

→ For current gain calculation we have to apply current division rule both at input section and output section.



from $I_1 = \frac{R_2}{R_1+R_2} \times I$

$$I_2 = \frac{R_1}{R_1+R_2} \times I$$

At input section applying current division rule

$$i_b = \frac{R_B}{R_B+\beta r_e} \times I_i$$

$$\Rightarrow \boxed{\frac{i_b}{I_i} = \frac{R_B}{R_B+\beta r_e}} \longrightarrow (1)$$

~~Let I_o curr.~~ At o/p section

Let I_o current is flowing through R_c

$$I_o = \frac{r_o}{r_o+R_c} \times \beta i_b$$

$$\Rightarrow \boxed{\frac{I_o}{\beta i_b} = \frac{\beta r_o}{r_o+R_c}} \longrightarrow (2)$$

multiplying eq^n (1) & eq^n (2)

$$\frac{i_b}{I_i} \times \frac{I_o}{i_b} = \frac{R_B}{(R_B+\beta r_e)} \times \frac{\beta r_o}{r_o+R_c}$$

$$\Rightarrow \frac{I_o}{I_i} = \frac{\beta R_B r_o}{(R_B+\beta r_e)(r_o+R_c)}$$

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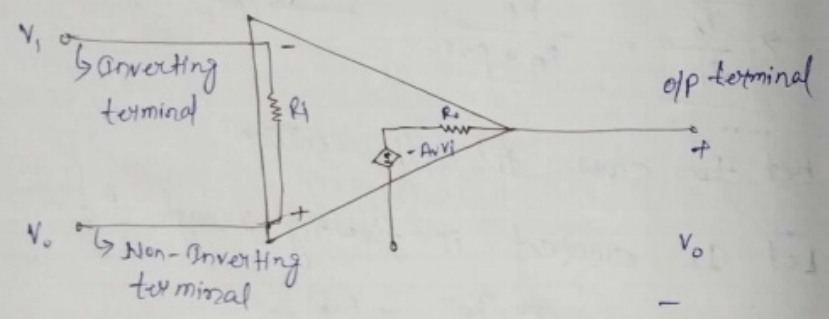
If, $R_B \geq 10\ \beta r_e$, then $R_B + \beta r_e \simeq R_B$

If, $r_0 \geq 10\ R_e$ then $r_0 + R_e \simeq r_0$

$$\Rightarrow A_I = \frac{I_0}{I_i} = \frac{\beta R_B r_0}{R_B r_0} \simeq \beta$$ where, $R_B \geq 10\ \beta r_e$ and $r_0 \geq 10\ R_e$

op-AMP & its application.



In op-AMP input Impedence is very-very high, In ideal op-AMP Input Impedence is infinite

The output Impedence of practical op-AMP is very-very low, then the output Impedence of Ideal op-AMP is zero

A_d = Differential mode gain.

A_c = common mode gain.

CMRR = common mode Rejection Ratio. $= \frac{A_d}{A_c}$

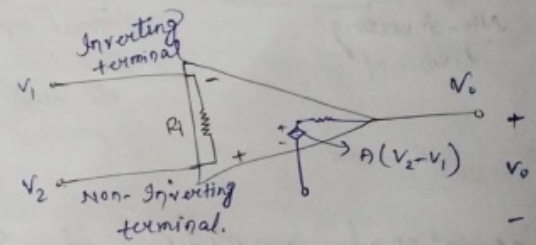
In Ideal op-AMP the common mode Rejection ratio (CMRR) is infinite, in practical CMRR is very-very high.

→ The slew rate of an ideal op-AMP is infinite

6) Write the characteristic of an ideal op-amp.

Imp

Block Diagram



$V_{id} = V_2 - V_1$

$$\text{gain} = A_v = \frac{V_o}{V_{id}} = \frac{V_o}{V_2 - V_1}$$

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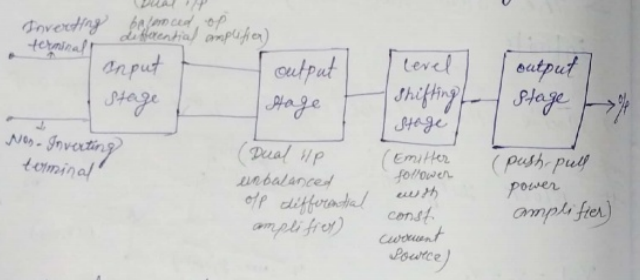
Ideal op-AMP.

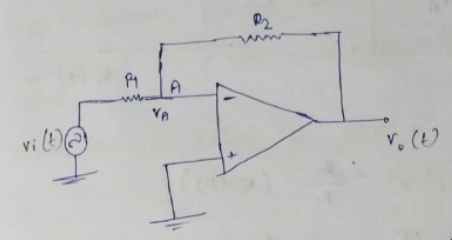
1. $R_i = \infty$
2. open loop voltage gain i.e $A_v = \infty$
3. $R_o = 0$
4. CMRR $= \infty$
5. Slew rate $= \infty$
6. Band width $= \infty$

In practical op-AMP very-very high.



The operational amplifier is a direct coupled high gain amplifier ~~consti~~ consisting of one more amplifier and usally followed by level-shifting stage and output stage.

Note:- In case of Ideal op-AMP virtual ground concept ~~arises~~. arises.



Let the voltage at node $A = V_A$ by virtual ground concept, $V_A = 0$

In this fig the Non-~~terminal~~ inverting terminal is grounded., so the voltage at non-inverting terminal is zero.

Let A is the node in the inverting terminal and the voltage at node A is V_A.

In ~~a~~ Ideal op-AMP, by virtual ground concept one terminal potential will automatically appear in the other terminal. that means there is a virtual short circuit exist between two terminal. So, by virtual ground concept $V_A = 0$.

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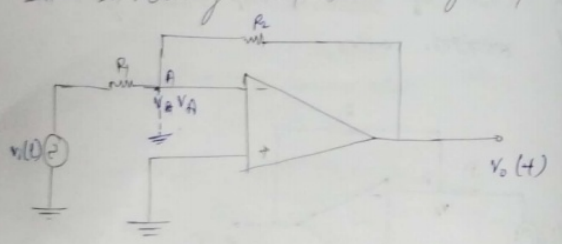
Inverting Amplifier using op-Amp



$$v_o(t) = -\frac{R_2}{R_1}\left(v_i(t)\right)$$

$$\Rightarrow \frac{v_o(t)}{v_i(t)} = -\frac{R_2}{R_1}$$

→ Let the voltage at node A is V_A Non-inverting terminal is grounded i.e zero By virtual ground concept $V_A = 0$

at node A.

$$\Rightarrow \frac{V_A - v_i(t)}{R_1} + \frac{V_A - v_o(t)}{R_2} = 0$$

$$\Rightarrow \frac{0 - v_i(t)}{R_1} + \frac{0 - v_o(t)}{R_2} = 0$$

$$\Rightarrow \frac{-v_i(t)}{R_1} = \frac{v_o(t)}{R_2}$$

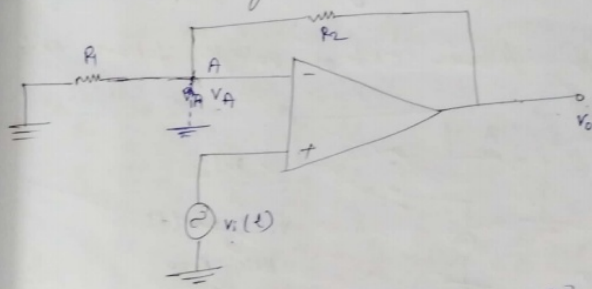
$$\Rightarrow \boxed{v_o(t) = -\frac{R_2}{R_1} v_i(t).}$$

The output voltage is out of phase of input voltage, i.e there is a phase difference of 180° between input & output voltage. that's why it is known as inverting amplifier.

Transfer function or gain $= -\frac{R_2}{R_1} = \frac{\text{output}}{\text{Input}}$

$$\frac{V_o(s)}{V_i(s)} = \frac{Y(s)}{X(s)}$$

Non-Inverting Amplifier using op-Amp.



→ Let voltage at node A is V_A, By virtual ground concept. $V_A = v_i(t)$.

at node A.

$$\frac{V_A - 0}{R_1} + \frac{V_A - v_o(t)}{R_2} = 0$$

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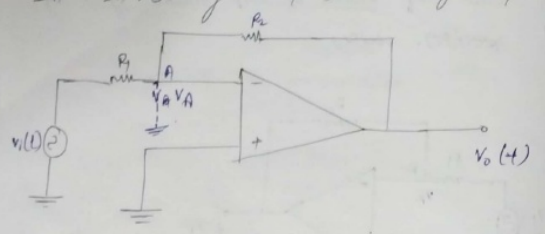
Inverting Amplifier using op-Amp



$$V_o(t) = -\frac{R_2}{R_1}(V_i(t))$$

$$\Rightarrow \frac{V_o(t)}{V_i(t)} = -\frac{R_2}{R_1}$$

→ Let the voltage at node A is V_A Non-inverting terminal is grounded i.e zero By virtual ground concept $V_A = 0$

at node A.

$$\Rightarrow \frac{V_A - V_i(t)}{R_1} + \frac{V_A - V_o(t)}{R_2} = 0$$

$$\Rightarrow \frac{0 - V_i(t)}{R_1} + \frac{0 - V_o(t)}{R_2} = 0$$

$$\Rightarrow \frac{-V_i(t)}{R_1} = \frac{V_o(t)}{R_2}$$

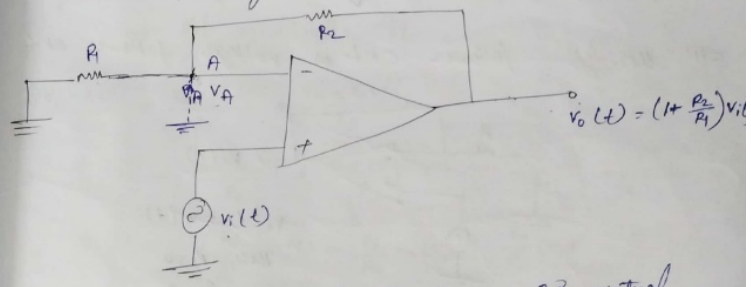
$$\Rightarrow \boxed{V_o(t) = -\frac{R_2}{R_1} V_i(t).}$$

The output voltage is out of phase of input voltage. i.e there is a phase difference of 180° between input & output voltage. that's why it is known as inverting amplifier.

Transfer function or gain $= -\frac{R_2}{R_1} = \frac{\text{output}}{\text{Input}}$

$$\frac{V_o(s)}{V_i(s)} = \frac{Y(s)}{X(s)}$$

Non-Inverting Amplifier using op-Amp.



→ Let voltage at node A is V_A, By virtual ground concept. $V_A = V_i(t)$.

at node A.

$$\frac{V_A - 0}{R_1} + \frac{V_A - V_o(t)}{R_2} = 0$$

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$$\Rightarrow \frac{v_i(t)-0}{R_1} + \frac{v_i(t)-v_o(t)}{R_2} = 0$$

$$\Rightarrow \frac{v_i(t)}{R_1} + \frac{v_i(t)}{R_2} - \frac{v_o(t)}{R_2} = 0$$

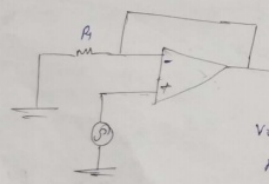
$$\Rightarrow \frac{v_i(t)}{R_1} + \frac{v_i(t)}{R_2} = \frac{v_o(t)}{R_2}$$

$$\Rightarrow v_o(t) = R_2\left(\frac{1}{R_1} + \frac{1}{R_2}\right) v_i(t)$$

$$\Rightarrow \boxed{v_o(t) = \left(1 + \frac{R_2}{R_1}\right) \cdot v_i(t)}$$

→ Here the output voltage is in same phase with the input voltage.

unity follower ckt or voltage follower ckt

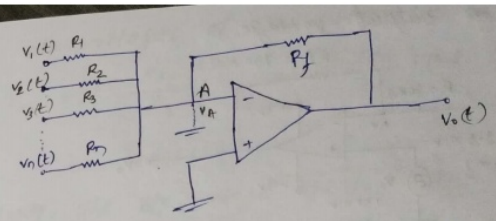


$v_o(t) = v_i(t)$

Here, $R_2 = 0$

$R_f = 0$

Summing Amplifier using op-Amp. or Weighted summer ckt)



$$v_o(t) = -\left(\frac{R_f}{R_1} \cdot v_1(t) + \frac{R_f}{R_2} \cdot v_2(t) + \frac{R_f}{R_3} \cdot v_3(t) \cdots + \frac{R_f}{R_n} \cdot v_n\right)$$

→ Let node A is virtually grounded, By virtual ground concept, $v_A = 0$

At node A:

$$\Rightarrow \frac{v_A - v_1(t)}{R_1} + \frac{v_A - v_2(t)}{R_2} + \frac{v_A - v_3(t)}{R_3} + \cdots \frac{v_A - v_n(t)}{R_n} + \frac{v_A - v_o(t)}{R_f}$$

$$\Rightarrow \frac{0 - v_1(t)}{R_1} + \frac{0 - v_2(t)}{R_2} + \frac{0 - v_3(t)}{R_3} + \cdots \frac{0 - v_n(t)}{R_n} = \frac{v_o(t)}{R_f}$$

$$\Rightarrow v_o(t) = -\left(\frac{R_f}{R_1} v_1(t) + \frac{R_f}{R_2} v_2(t) + \frac{R_f}{R_3} v_3(t) + \cdots + \frac{R_f}{R_n} v_n(t)\right)$$

→ Here the output voltage is weighted sum of the input voltage of signal.

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The o/p voltage of 2nd stage i.e.

$$V_{o2} = \left(-\frac{R_{F2}}{R_2}\right) V_{o1} = \left(-\frac{680}{22}\right)(586.66)$$

$$= -18133.33 \text{ mV}$$

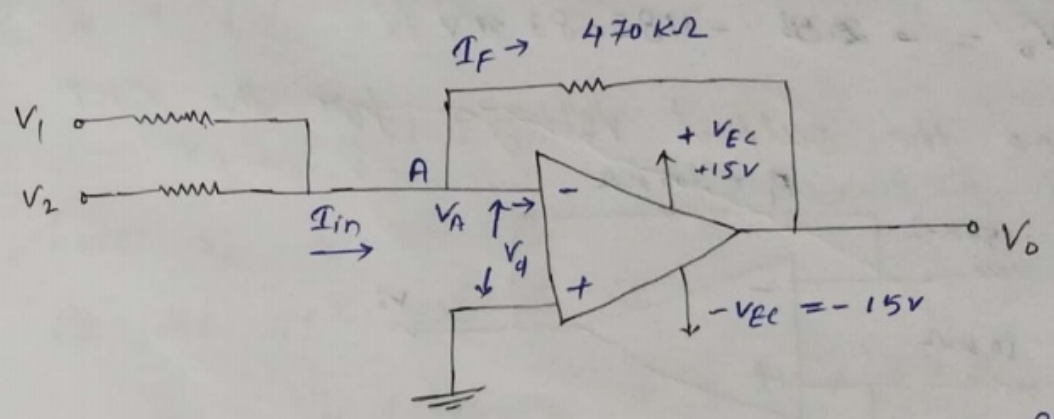
Similarly, the o/p voltage of 3rd stage i.e.

$$V_o = \left(-\frac{R_{F3}}{R_3}\right) V_{o2} = \left(-\frac{750}{33}\right)(-18133.33)$$

$$= 412121.21 \text{ mV}$$

$$= 412.12 \text{ mvolt} \qquad = \boxed{\frac{412121.21}{1000}} \rightarrow \text{mV}$$

(3.) Calculate the output voltage for the ckt with inputs of $V_1 = 40$ mV rms and $V_2 = 20$ mV rms.



Soln:- Applying virtual ground concept & considering op-amp as ideal i.e $A = \infty$ & $R_i = \infty$ R

then $V_d = 0 \Rightarrow V_{in} - V_a = 0 \Rightarrow V_{in} = V_a$

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As V_a is grounded $V_a = 0$. So $V_{in} = V_a = 0$ V.
and $R_i = \infty$ So $I_B = 0$

Applying KCL to node A.

$$\Rightarrow \frac{V_1 - V_{in}}{47\,k\Omega} + \frac{V_2 - V_{in}}{12\,k\Omega} = \frac{V_{in} - V_o}{470\,k\Omega}$$

$$\Rightarrow \frac{40\,mV}{47\,k\Omega} + \frac{20\,mV}{12\,k\Omega} = \frac{-V_o}{470\,k\Omega}$$

$$\Rightarrow 0.85\,\mu A + 1.66\,\mu A = \frac{-V_o}{470\,k\Omega}$$

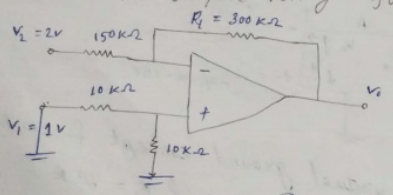
$$\Rightarrow 2.51\,\mu A = \frac{V_o}{470\,k\Omega}$$

$$\Rightarrow V_o = -2.51\,\mu A \times 470\,k\Omega$$

O/P voltage:

$$\Rightarrow V_o = -1182.83\,mV$$

(4) Determine the output voltage for the CKT.



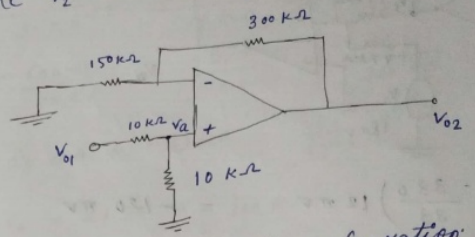
Soln:- This is an inverting configuration.

$$V_{o2} = \left(-\frac{R_F}{R_1}\right) V_2 = \left(-\frac{300}{150}\right) \times 2$$

$$\Rightarrow V_{o2} = -4V$$

where V_{o2} is the o/p voltage due to V_2.

Applying superposition principle to the terminal V_1 take $V_2 = 0$, i.e. grounded.



This is an non-inverting configuration.

$$V_a = \frac{V_1 \times 10}{10 + 10} = \frac{10}{20} = 0.5 \text{ volt.}$$

$$\Rightarrow V_{01} = \left(1 + \frac{R_F}{R_1}\right) \times V_a = \left(1 + \frac{300}{150}\right) \times 0.5$$

$$\Rightarrow V_{01} = 1.5 \text{ volt.}$$

where V_{01} is the o/p voltage due to V_1

So the net output is

$$V_a = V_{01} + V_{02} = -4V + 1.5V \Rightarrow V_o = -2.5V$$

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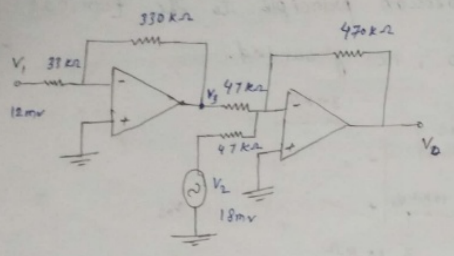
(5) Determine the output voltage for the ckt.



$\rightarrow V_3 = \left(\frac{-330}{33}\right) 12\ mV = -120\ mV$

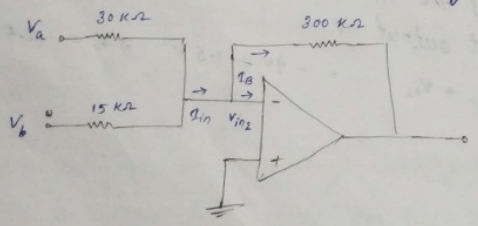
$\Rightarrow 1.66\ \mu A - 0.66\ \mu A = \frac{-V_a}{600\ k\Omega}$

$\Rightarrow V_a = -1\ \mu A \times 600\ k\Omega = -600\ mV$

Here op-amp (2) is a voltage buffer.

$\therefore V_b = -20\ mV$

op-amp (3) is a again an summing amplifier.



Applying virtual ground concept $V_{in2} = 0$ volt

& $I_B = 0$ $\therefore I_{in} = I_F$

$\Rightarrow \frac{V_a - V_{in2}}{30\ k\Omega} + \frac{V_b - V_{in2}}{15\ k\Omega} = \frac{V_{in2} - V_o}{300\ k}$

$\Rightarrow \frac{-600\ mV}{30\ k\Omega} + \frac{-20\ mV}{15\ k\Omega} = \frac{-V_o}{300\ k\Omega}$

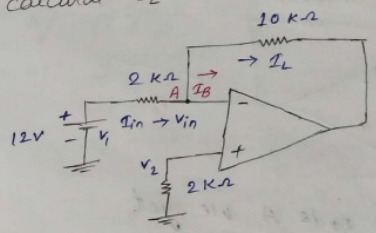
$\Rightarrow 20\ \mu A + 1.33\ \mu A = \frac{V_o}{300\ k\Omega}$

$\Rightarrow V_o = 21.33\ \mu A \times 300\ k\Omega$

$\Rightarrow V_o = 6399\ mV$

$\Rightarrow V_o = 6.399 \simeq 6.4$ volt.

(6) calculate I_L..



Applying KCL at node A

$\therefore I_{in} = I_B + I_L$

$\Rightarrow I_{in} = I_L$

$\Rightarrow I_L = \frac{V_1 - V_{in}}{2\ k\Omega} = \frac{12\ V}{2\ k\Omega} \Rightarrow I_L = 6\ mA$

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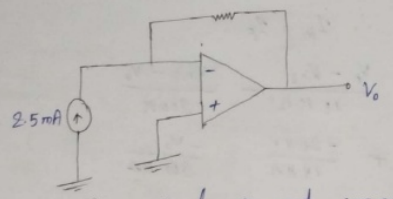
(7) calculate V_0 for the CKT above.

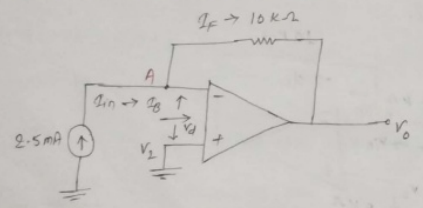


→ Applying virtual ground concept & considering op-amp is an ideal i.e. $A = \infty$ and $R_i = \infty\ \Omega$

then. $V_d = 0 \Rightarrow V_1 - V_2 = 0 \Rightarrow V_1 = V_2$

As V_2 is grounded so $V_1 = V_2 = 0V$

and $R_i = \infty$ so $I_B = 0$



Applying KCL at node A we get.

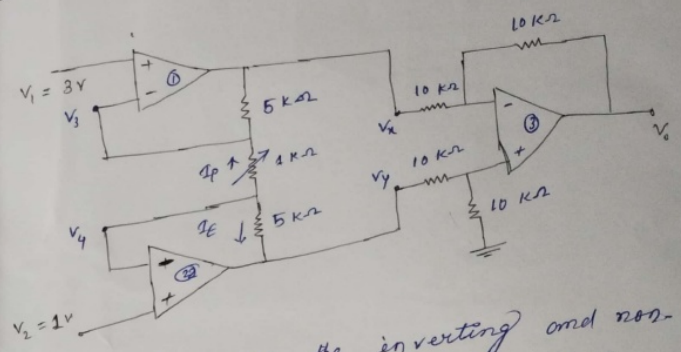
$I_{in} = I_B + I_F$

$\Rightarrow I_{in} = I_F$

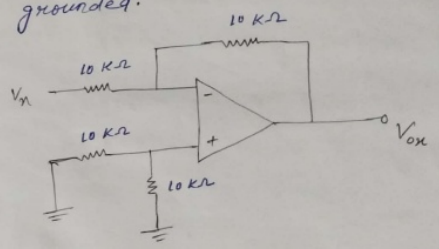
$\Rightarrow 2.5\,mA = \frac{V_2 - V_0}{10} = -\frac{V_0}{10}$

$\Rightarrow V_0 = -25\,V$

(8) calculate the output voltage V_0.



→ Let V_x & V_y are the inverting and non-inverting terminal voltages at op-amp (3) so by applying superposition principle take $V_y = 0$ i.e grounded.



$V_{ox} = \left(-\frac{10}{10}\right) \times V_x = -V_x$

and considering $V_x = 0$ i.e grounded. we get,

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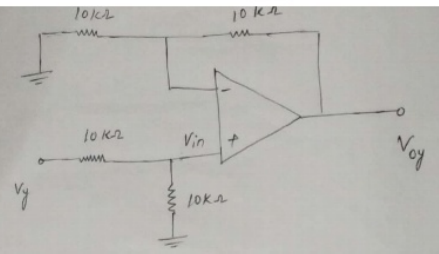


$$V_{oy} = \left(1 + \frac{10}{10}\right) V_{in} = 2 \times \frac{V_y \times 10}{10 + 10}$$

$$= 2 \times \frac{V_y \times 10}{20}$$

$$\Rightarrow V_{o2} = V_y$$

$$\therefore V_{oT} = V_{ox} + V_{oy} = V_y - V_x$$

Calculat^n for V_x & V_y

Applying virtual ground concept to op-Amp (1) & (2)

$V_3 = V_1 = 3V$ and $V_4 = V_2 = 1V$

Applying KCL at node A.

$$I_x = I_p \Rightarrow \frac{V_3 - V_x}{5} = \frac{V_4 - V_3}{1} = \frac{3 - V_x}{5}$$

$$= \frac{1-3}{1} \Rightarrow 3 - V_x = -10 \Rightarrow V_x = 13 \text{ volt}$$

Again applying KCL at node B

$$I_y + I_p = 0$$

$$\Rightarrow \frac{V_4 - V_y}{5} + \frac{V_4 - V_3}{1} = 0$$

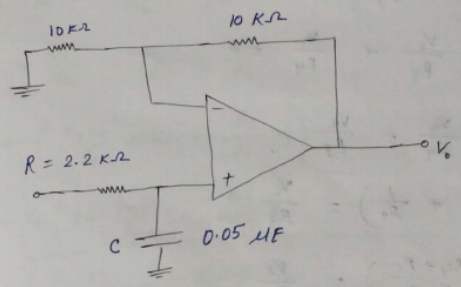
$$\Rightarrow \frac{1 - V_y}{5} + \frac{1-3}{1} = 0$$

$$\Rightarrow \frac{1 - V_y}{5} - 2 = 0$$

$$\Rightarrow 1 - V_y = 10 \quad \Rightarrow V_y = 1 - 10 = -9 \text{ volt.}$$

$$\therefore V_o = V_y - V_x = -9 - 13 = -22 \text{ volt.}$$

(9.) calculate the cut off frequency of a first order lowpass filter ckt:



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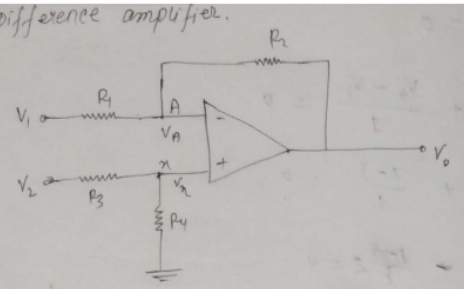
Difference amplifier.



at node x

Let the voltage at node x is V_x

Apply nodal Analysis at node x

$$\frac{V_x - V_2}{R_3} + \frac{V_x - 0}{R_4} = 0$$

$$\Rightarrow \frac{V_x}{R_3} - \frac{V_2}{R_3} + \frac{V_x}{R_4} = 0$$

$$\Rightarrow \frac{V_x}{R_3} + \frac{V_x}{R_4} = \frac{V_2}{R_3}$$

$$\Rightarrow V_x\left(\frac{1}{R_3} + \frac{1}{R_4}\right) = \frac{V_2}{R_3}$$

$$\Rightarrow V_x \times \left(\frac{R_4 + R_3}{R_3 R_4}\right) = \frac{V_2}{R_3}$$

$$\Rightarrow V_x \times \left(\frac{R_4 + R_3}{R_4}\right) = V_2$$

$$\Rightarrow V_x = \frac{R_4 V_2}{R_4 + R_3}$$

at node A

Let node A is virtually grounded.

By virtual concept.

$$V_A = V_x = \frac{R_4 V_2}{R_4 + R_3}$$

at node A.

$$\Rightarrow \frac{V_A - V_1}{R_1} + \frac{V_A - V_0}{R_2} = 0$$

$$\Rightarrow \frac{V_x - V_1}{R_1} + \frac{V_x - V_0}{R_2} = 0 \quad [V_A = V_x \text{ By virtual grounded concept}].$$

$$\Rightarrow \frac{V_x}{R_1} - \frac{V_1}{R_1} + \frac{V_x}{R_2} - \frac{V_0}{R_2} = 0$$

$$\Rightarrow \frac{V_x}{R_1} + \frac{V_x}{R_2} - \frac{V_1}{R_1} = \frac{V_0}{R_2}$$

$$\Rightarrow V_0 = \left(\frac{R_2 V_x}{R_1} + V_x - \frac{R_2}{R_1} V_1\right)$$

$$= V_x\left(1 + \frac{R_2}{R_1}\right) - \frac{R_2}{R_1} V_1$$

$$V_0 = \boxed{\frac{R_4 V_2}{R_3 + R_4} \times \left(\frac{R_1 + R_2}{R_1}\right) - \frac{R_2}{R_1} \cdot V_1}$$

Let $R_1 = R_3$, $R_2 = R_4$

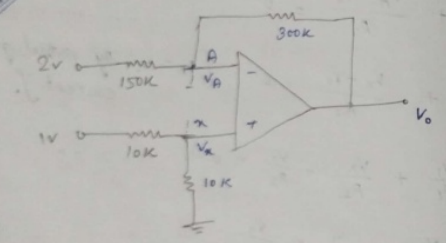
$R_3 + R_4 = R_1 + R_2$,

$$\Rightarrow V_0 = \frac{R_2 V_2}{R_1+R_2} \times \left(\frac{R_1+R_2}{R_1}\right) - \frac{R_2}{R_1} V_1$$

$$= \frac{R_2}{R_1} V_2 - \frac{R_2}{R_1} \cdot V_1$$

$$\boxed{V_0 = \frac{R_2}{R_1}(V_2 - V_1)}$$

Q.



at node x.

$$\frac{V_x - 1}{10} + \frac{V_x - 0}{10} = 0$$

$$\Rightarrow \frac{V_x}{10} - \frac{1}{10} + \frac{V_x}{10} = 0$$

$$\Rightarrow \frac{2V_x}{10} = \frac{1}{10}$$

$$\Rightarrow V_x = \frac{1}{2} = 0.5\,V$$

at node A.

$$\frac{V_A - 2}{150} + \frac{V_A - V_0}{300} = 0$$

$$\Rightarrow \frac{0.5-2}{150} + \frac{0.5 - V_0}{300} = 0$$

$$\Rightarrow \frac{-1.5}{150} + \frac{0.5}{300} - \frac{V_0}{300} = 0$$

$$\Rightarrow \frac{-1.5}{150} + \frac{0.5}{300} = \frac{V_0}{300}$$

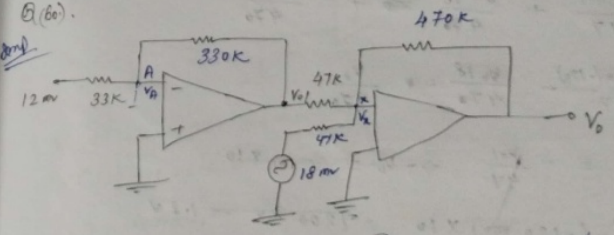
$$\Rightarrow V_0 = 300\left(\frac{-1.5}{150} + \frac{0.5}{300}\right)$$

$$\Rightarrow V_0 = -2 \times 1.5 + 0.5$$

$$\Rightarrow V_0 = -3 + 0.5$$

$$= -2.5\,V$$

Q(60).



Let node A is virtually grounded.

By virtual ground concept $V_A = 0$

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At node A.

$$\frac{V_A - 12}{33} + \frac{V_A - V_{01}}{330} = 0$$

$$\Rightarrow \frac{0-12}{33} + \frac{0 - V_{01}}{330} = 0$$

$$\Rightarrow \frac{-12}{33} = \frac{V_{01}}{330}$$

$$\Rightarrow \boxed{V_{01} = -12 \times 10 = -120\,mV}$$

Let node x is virtually grounded in 2nd op-Amp.
By virtual ground concept $V_x = 0$

at node x

$$\frac{V_x - V_{01}}{47} + \frac{V_x - 18}{470} + \frac{V_x - V_0}{470} = 0$$

$$\Rightarrow \frac{0 - V_{01}}{47} + \frac{0 - 18}{470} + \frac{0 - V_0}{470}$$

$$\Rightarrow -\frac{(-120)}{47} - \frac{18}{470} = \frac{V_0}{470}$$

$$\Rightarrow \frac{V_0}{470} = -\frac{V_{01}}{47} \quad \cancel{\Rightarrow V_0 = -V_{01} \times 10}$$

$$= -(-120\,mV) \times 10 \quad \cancel{= 1200\,mV} = 1.2\,V$$

$$\Rightarrow \frac{120 - 18}{47} = \frac{V_0}{470}$$

$$\Rightarrow V_0 = 102 \times 10\,mV$$

$$= 1020\,mV = 1.02\,V$$

and process

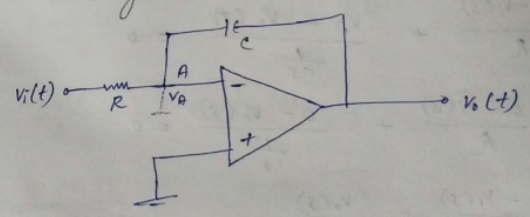
2nd op-Amp

$$V_0 = -\left(\frac{R_f}{R_1} V_{01} + \frac{R_f}{R_2} V_2\right)$$

$$= -\left(\frac{470}{47} \times (-120\,mV) + \frac{470}{47} \times 18\right)$$

$$= 1200 - 180 = 1020\,mV = 1.02\,V$$

Integrator ckt using op-AMP.



$V_0(t)$ = time domain.

$V_0(S)$ = Laplace Transform of $V_0(t)$

S = domain.

$S = \sigma + j\omega$

If $\sigma = 0$

$S = j\omega \quad \Rightarrow \omega = 2\pi f$

$$L[f(t)] = \int_0^\infty f(t)\, e^{-st}\, dt$$

Laplace Transform

$R \rightarrow R$

$C \rightarrow \frac{1}{Cs}$

$L[v_i(t) = v_i(s)$

$L[v_o(t) = v_o(s)$

$L^{-1}[v_o(s)] = v_o(t)$

$L^{-1}[v_i(s)] = v_i(t)$

current flowing accross capacitor $C \cdot \frac{dv}{dt} = C$

At node A is virtually grounded.

By virtual grounded concept $V_A = 0$

At node A

$$\Rightarrow \frac{V_A - V_i(s)}{R} + \frac{V_A - V_o(s)}{\frac{1}{Cs}} = 0$$

$$\Rightarrow \frac{0 - V_i(s)}{R} + \frac{0 - V_o(s)}{\frac{1}{Cs}} = 0$$

$$\Rightarrow \frac{-V_i(s)}{R} = \frac{V_o(s)}{\frac{1}{Cs}}$$

$$\Rightarrow \boxed{\frac{V_o(s)}{V_i(s)} = -\frac{1}{RCs}}$$ Transfer function of Integrator.

$$\Rightarrow V_o(s) = -\frac{V_i(s)}{RCs}$$

Taking Inverse Laplace Transform.

$$\Rightarrow L^{-1}[V_o(s)] = -\frac{1}{RC} L^{-1}\left[\frac{1}{s} V_i(s)\right]$$

$$\Rightarrow \boxed{V_o(t) = -\frac{1}{RC}\int_0^t V_i(t) \cdot dt}$$

at node A is virtually grounded.

By virtual ground concept $V_A = 0$

at node A

$$\frac{V_A - V_i(t)}{R} + \frac{C\, d(V_A - V_o(t))}{dt} = 0$$

$$\Rightarrow \frac{0 - V_i(t)}{R} + \frac{C\, d\{0 - V_o(t)\}}{dt} = 0$$

$$\Rightarrow \frac{-V_i(t)}{R} - C\frac{dV_o(t)}{dt} = 0$$

$$\Rightarrow \frac{C\, dV_o(t)}{dt} = -\frac{V_i(t)}{R}$$

$$\Rightarrow \boxed{\frac{dV_o(t)}{dt} = -\frac{1}{RC} V_i(t)}$$

Differentiating both sides w.r.t. to t

$$\int \frac{d\, V_o(t)}{dt} = -\frac{1}{RC}\int_0^t V_i(t) \cdot dt$$

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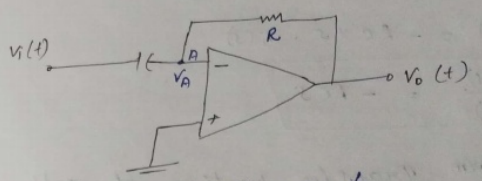
Differentiator ckt using op-Amp.



By virtual ground concept.

$V_A = 0$

at node A.

$$\frac{C\,d(V_A - V_i(t))}{dt} + \frac{V_A - V_o(t)}{R} = 0$$

$$\Rightarrow \frac{C\,d\{0 - V_i(t)\}}{dt} + \frac{0 - V_o(t)}{R} = 0$$

$$\Rightarrow -C\frac{d\,V_i(t)}{dt} = \frac{V_o(t)}{R}$$

$$\Rightarrow \boxed{V_o(t) = -RC \cdot \frac{d\,V_i(t)}{dt}}$$

$$L\left[\frac{d\,V_i(t)}{dt}\right] = S V_i(S)$$

$$L\left[\int_0^t V_i(t)\,dt\right] = \frac{1}{S} V_i(S)$$

Taking Laplace Transform both sides.

$$V_o(t) = -\frac{1}{RC}\int_0^t V_i(t)\,dt$$

Integrated provides the output voltage which is proportional to the time integral of the input voltage.

gain.

We know the transform function of Integrator is $\frac{V_o(S)}{V_i(S)} = -\frac{1}{RCS}$

$$\frac{V_o(S)}{V_i(S)} = -\frac{1}{RCS}$$

put $S = j\omega$

gain, $A_{CL} = -\frac{1}{j\omega RC} = -\frac{1}{j2\pi f RC} = \frac{j}{2\pi f RC}$

$$|A_{CL}| = \frac{1}{2\pi f RC}$$

$j^2 = -1$

$\frac{1}{j} = \frac{j}{j \times j} = \frac{j}{j^2}$

$= \frac{j}{-1} = -j$

$j = \sqrt{-1}$ $\quad \frac{1}{j} = -j$

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$$L[v_o(t)] = -RC\, L\left[\frac{d\, v_i(t)}{dt}\right]$$

$$\Rightarrow v_o(s) = -RC \times s \cdot v_i(s)$$

$$\Rightarrow \boxed{\frac{v_o(s)}{v_i(s)} = -RCs}$$

~~Transform~~ Transfer function of Differentiator ckt

Q) What is feedback ?

→ Feedback is a concept in which some part of output is injected back to the ~~inside~~ input side..

It is of two types:-

(i) Positive feedback

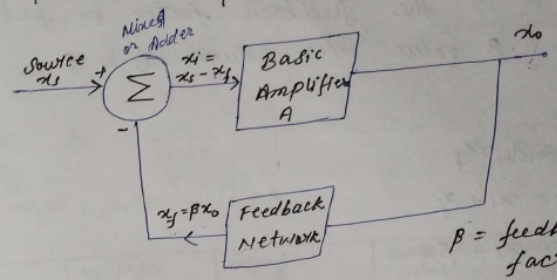
(ii) Negative feedback

→ If we are using a positive feedback than its act like a amplifier

→ If we are using a Negative feedback than its ack like a oscillator.

In case of -ve feedback the gain is decrease

Imp # Feedback Amplifier



β = feedback factor.

A = gain without feedback

A_f = gain with feedback

$$\# \quad A_f = \frac{A}{1+\beta A}$$

$$A = \frac{x_o}{x_i}, \quad A_f = \frac{x_o}{x_s}$$

gain with feedback $= A_f = \frac{x_o}{x_s}$

x_s and x_f are applied to mixer circuit so the output of the mixer circuit $x_i = x_s - x_f$

x_i is the ~~basic~~ Input ~~to~~ of the basic amplifier

x_o is the output of the basic amplifier

x_f is the output of the feedback network.

$$x_f = \beta \cdot x_o$$

where, β is the feedback factor or feedback ratio. β value lies between 0 to 1.

We have,

$$x_i = x_s - x_f$$

$$\Rightarrow x_s = x_i + x_f$$

$$\Rightarrow x_s = x_i + \beta x_o$$

gain with feedback = A_f

$$A_f = \frac{x_o}{x_s} = \frac{x_o}{x_i + \beta x_o}$$

Dividing x_i both in N^r & D^r

$$A_f = \frac{x_o/x_i}{x_i + \beta x_o/x_i} = \frac{A}{1+\beta \frac{x_o}{x_i}} = \frac{A}{1+\beta A}$$

In -ve feedback $A_f = \frac{A}{1+\beta A}$

There are four types of topologies in feedback amplifier.

(1) voltage series feedback amplifier connection.
(2) voltage shunt feedback connection
(3) current series feedback connection
(4) current shunt feedback connection.

$A_f = \frac{A}{1+\beta A}$

magic factor $= 1+\beta A$

{ series → inc.
voltage → dec }

	voltage series feedback	voltage shunt feedback	current series feedback	current shunt feedback
Z_{if}	$Z_{if} = Z_{in}(1+\beta A)$	$Z_{if} = Z_{in}/1+\beta A$	$Z_{if} = Z_{in}(1+\beta A)$	$Z_{if} = Z_{in}/1+\beta A$
Z_{of}	$Z_{of} = Z_o/1+\beta A$	$Z_{of} = \frac{Z_o}{1+\beta A}$	$Z_{of} = Z_o(1+\beta A)$	$Z_{of} = Z_o(1+\beta A)$

Imp

Derivation of Z_{if} & Z_{of} of a voltage series feedback amplifier

→ voltage series feedback.

calculate Z_{if}.

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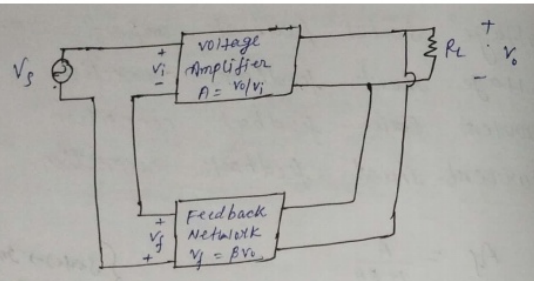
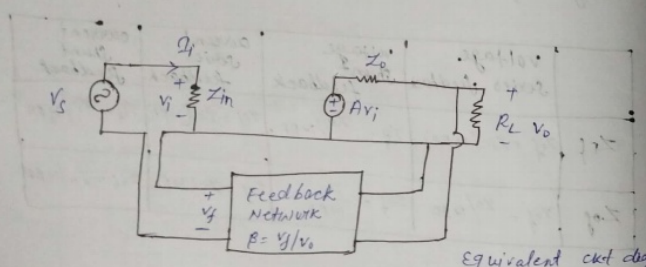


(block diagram of voltage series feedback)



Equivalent ckt diagram

In this diagram.

$Z_{in} = \frac{V_i}{I_i}$, $Z_{if} = \frac{V_s}{I_i}$

In -ve feedback amplifier,

$V_i = V_s - V_f$

$\Rightarrow V_s = V_i + V_f$

$\Rightarrow V_s = V_i + V_f = Z_{in} I_i + \beta V_o$

As $Z_{in} = V_i / I_o$

We know that $A = \frac{V_o}{V_i}$

$V_o = AV_i$

$V_s = Z_{in} I_i + \beta \times AV_i$

$= Z_{in} I_i + \beta A \times Z_{in} I_i$

$V_s = (1+\beta A) Z_{in} I_i$

Now, $Z_{if} = \frac{V_s}{I_i}$

$Z_{if} = \frac{(1+\beta A) Z_{in} I_i}{I_i}$

$$\boxed{Z_{if} = Z_{in}(1+\beta A)}$$

The input impedence with feedback Increase by a factor of $(1+\beta A)$

calculation of Z_{of}

$Z_{of} = \frac{Z_o}{1+\beta A}$

The output Impedence is determined applying a voltage V_o at the ou
R_L) which results a current I_o

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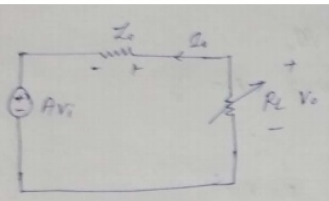


$$Z_{of} = \frac{V_o}{I_o}\Big|_{V_s=0}$$

In -ve feedback amplifier $V_i = V_s - V_f$

If $V_s = 0$, here

$V_i = -V_f \longrightarrow (1)$

Applying KVL in the input loop.

$$AV_i + Z_o I_o - V_o = 0$$

$$\Rightarrow V_o = AV_i + Z_o I_o$$

$$= A(-V_f) + Z_o I_o \quad [\text{from eq}^n\ (1)]$$

$$= -A\beta V_o + Z_o I_o$$

$$\Rightarrow V_o + \beta A V_o = Z_o I_o$$

$$\Rightarrow V_o(1+\beta A) = Z_o I_o$$

$$\Rightarrow \frac{V_o}{I_o} = Z_{of} = \frac{Z_o}{1+\beta A}$$

So, the output impedence decreases ~~with~~ by a factor $1+\beta A$ in voltage series feedback amplifier.

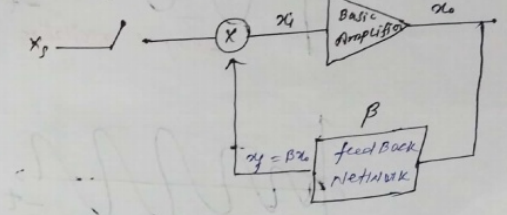
Oscillator

A circuit which can generate an ~~Ac~~ a.c wave form without using any a.c sn

→ An oscillator provide sinusoidal wave form

→ The circuit which generates non-sinusoidal waveform such as triangular wave for, square wave form etc. are called wave-form generators.

→ In oscillators sufficient positive feedback is used.

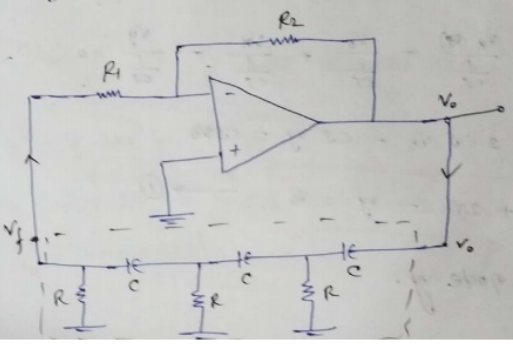


Oscillator

- Audio or low frequency oscillator
  - RC- phase shift oscillator.
    - using FET
    - using opAMP
    - using BJT
    - Wein Bridge oscillator
- Radio or high frequency oscillator
  - LC- oscillator
    - Hartly oscillator
    - colpitt's oscillator
    - clapp oscillator
  - crystal oscillator

Imp

RC phase- shift oscillator (using op-amp).



In +ve feedback,

$$A_f = \frac{A}{1-\beta A}$$

Imp

Barkhausen's criteria.

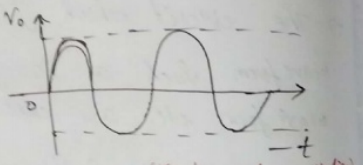
(i) $|\beta A| = 1$

(ii) $\angle \beta A = 0^\circ$ or 360° or 2π

βA = loop gain.

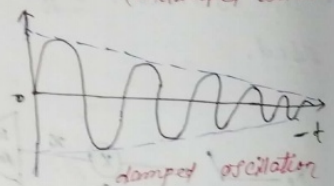
Note

(1) If $|\beta A| = 1$



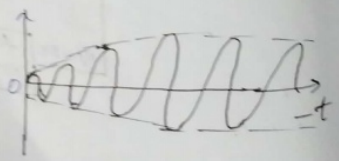
(undamped oscillation)

(2) If $|\beta A| < 1$



damped oscillation

(3) If $|\beta A| > 1$



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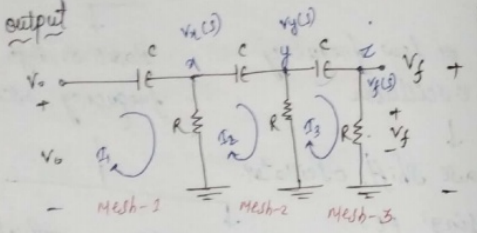
$$f_0 = \frac{1}{2\pi\sqrt{6}\,RC}$$

output



$$\frac{V_f}{V_o} = ?$$

→ at node x

$$\Rightarrow \frac{V_x(s) - 0}{R} + \frac{V_x(s) - V_o(s)}{\frac{1}{Cs}} + \frac{V_x(s) - V_y(s)}{\frac{1}{Cs}} = 0$$

$$\Rightarrow \frac{V_x}{R} + \frac{V_x}{\frac{1}{Cs}} - \frac{V_o}{\frac{1}{Cs}} + \frac{V_x}{\frac{1}{Cs}} - \frac{V_y}{\frac{1}{Cs}} = 0$$

$$\Rightarrow \frac{V_x}{R} + 2CsV_x - CsV_y = CsV_o$$

$$\Rightarrow \boxed{\frac{V_x}{RCs} + 2V_x - V_y = V_o} \longrightarrow (1)$$

→ at node y.

$$\frac{V_y - 0}{R} + \frac{V_y - V_x}{\frac{1}{Cs}} + \frac{V_y - V_f}{\frac{1}{Cs}} = 0$$

$$\Rightarrow \frac{V_y}{R} + CsV_y - CsV_x + CsV_y - CsV_f = 0$$

$$\Rightarrow \boxed{\frac{V_y}{RCs} + 2V_y - V_x = V_f} \longrightarrow (2)$$

→ at node Z.

$$\Rightarrow \frac{V_f - 0}{R} + \frac{V_f - V_y}{\frac{1}{Cs}} = 0$$

$$\Rightarrow \frac{V_f}{R} + CsV_f = CsV_y$$

$$\Rightarrow V_y = \frac{1}{RCs}V_f + V_f$$

$$\boxed{= \left(1 + \frac{1}{RCs}\right)V_f} \longrightarrow (3)$$

Putting the V_y value in eqn (1)

$$\frac{V_x}{RCs} + 2V_x - \left(1 + \frac{1}{RCs}\right)V_f = V_o$$

$$\Rightarrow V_x\left(\frac{1}{RCs} + 2\right) = V_o + \left(1 + \frac{1}{RCs}\right)V_f$$

$$\Rightarrow V_x \times \left(\frac{1 + 2RCs}{RCs}\right) = V_o + \left(\frac{1 + RCs}{RCs}\right)V_f$$

$$\Rightarrow V_x = \left(\frac{RCS}{1+2RCS}\right) \times \left(V_0 + \frac{1+RCS}{RCS} V_f\right)$$

$$\Rightarrow \boxed{V_x = \frac{RCS}{1+2RCS} V_0 + \left(\frac{1+RCS}{1+2RCS}\right) V_f}$$

from eq ②

$$\Rightarrow \frac{V_y}{RCS} + 2V_y - V_x = V_f$$

$$\Rightarrow V_y\left(\frac{1}{RCS} + 2\right) - V_x = V_f$$

$$\Rightarrow V_y\left(\frac{1+2RCS}{RCS}\right) - V_x = V_f$$

$$\Rightarrow \left(\frac{1+RCS}{RCS}\right) V_f \times \left(\frac{1+2RCS}{RCS}\right) - \left\{\frac{RCS}{1+2RCS} V_0 + \frac{1+RCS}{1+2RCS} V_f\right\} = V_f$$

$$\Rightarrow \frac{(1+RCS)(1+2RCS)}{R^2C^2S^2} V_f - \frac{RCS}{1+2RCS} V_0 - \frac{1+RCS}{1+2RCS} V_f = V_f$$

$$\Rightarrow \frac{RCS}{1+2RCS} V_0 = \frac{(1+RCS)(1+2RCS)}{R^2C^2S^2} V_f - \frac{1+RCS}{1+2RCS} V_f - V_f$$

$$= \frac{(1+RCS)(1+2RCS)^2 - (1+RCS)R^2C^2S^2 - R^2C^2S^2(1+2RCS)}{R^2C^2S^2(1+2RCS)} V_f$$

$$\Rightarrow \frac{V_f}{V_0} = \frac{R^3C^3S^3}{(1+RCS)(1+2RCS)^2 - R^2C^2S^2(1+RCS) - R^2C^2S^2(1+2RCS)}$$

$$\frac{V_f}{V_0} = \frac{R^3C^3S^3}{(1+RCS)(1+2RCS)^2 - R^2C^2S^2 - R^3C^3S^3 - R^2C^2S^2 - 2R^3C^3S^3}$$

$$\frac{V_f}{V_0} = \frac{R^3C^3S^3}{(1+RCS)(1+2RCS)^2 - 2R^2C^2S^2 - 3R^3C^3S^3}$$

$$\frac{V_f}{V_0} = \frac{R^3C^3S^3}{(1+RCS)(1+4R^2C^2S^2+4RCS) - 2R^2C^2S^2 - 3R^3C^3S^3}$$

$$\frac{V_f}{V_0} = \frac{R^3C^3S^3}{(1+4R^2C^2S^2+4RCS) + RCS\{1+4R^2C^2S^2+4RCS\} - 2R^2C^2S^2 - 3R^3C^3S^3}$$

$$\frac{V_f}{V_0} = \frac{R^3C^3S^3}{1+4R^2C^2S^2+4RCS+RCS+4R^3C^3S^3+4R^2C^2S^2 - 2R^2C^2S^2 - 3R^3C^3S^3}$$

$$\Rightarrow \boxed{\frac{V_f}{V_0} = \frac{R^3C^3S^3}{R^3C^3S^3 + 6R^2C^2S^2 + 5RCS + 1}} \longrightarrow ①$$

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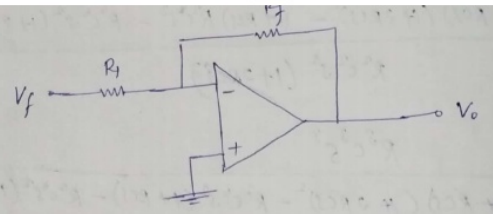


$$V_o = \left(-\frac{R_f}{R_1}\right) V_f$$

$$\Rightarrow \boxed{\frac{V_o}{V_f} = -\frac{R_f}{R_1}} \longrightarrow (2)$$

In above inverting amplifier, we get,

$$\frac{V_o}{V_f} = -\frac{R_f}{R_1}$$

Multiply eqn (1) × eqn (2)

$$\Rightarrow \frac{V_o}{V_f} \times \frac{V_f}{V_o} = \left(-\frac{R_f}{R_1}\right) \times \left(\frac{s^3R^3C^3}{s^3R^3C^3 + 6s^2R^2C^2 + 5sRC + 1}\right)$$

$$\Rightarrow 1 = \left(-\frac{R_f}{R_1}\right) \times \left(\frac{s^3R^3C^3}{s^3R^3C^3 + 6s^2R^2C^2 + 5sRC + 1}\right)$$

We have,

$$s = j\omega, \quad s^3 = (j\omega)^3 = j^3\omega^3 = j^2 \times j \times \omega^3$$

$$= -1 \times j\omega^3 = -j\omega^3$$

$$s^2 = (j\omega)^2 = j^2\omega^2 = -\omega^2$$

$$\Rightarrow \boxed{-\left(\frac{R_f}{R_1}\right) \times \frac{-j\omega^3R^3C^3}{-j\omega^3R^3C^3 - 6\omega^2R^2C^2 + j5\omega RC + 1} = 1}$$

$$\Rightarrow \left(-\frac{R_f}{R_1}\right)(-j\omega^3R^3C^3) = -j\omega^3R^3C^3 - 6\omega^2R^2C^2 + j5\omega RC + 1$$

$$\Rightarrow j\left(\frac{R_f}{R_1}\right) \times \omega^3R^3C^3 = (1 - 6\omega^2R^2C^2) + j(5\omega RC - \omega^3R^3C^3)$$

Equating both Real & imaginary part in the above eqn.

$$1 - 6\omega^2R^2C^2 = 0 \quad \& \quad \left(\frac{R_f}{R_1}\right)\omega^3R^3C^3 = 5\omega RC - \omega^3R^3C^3$$

Now, we have,

$$1 - 6\omega^2R^2C^2 = 0$$

We know, $\omega = 2\pi f$

So, $1 = 6\omega^2R^2C^2 \Rightarrow \omega^2R^2C^2 = \frac{1}{6}$

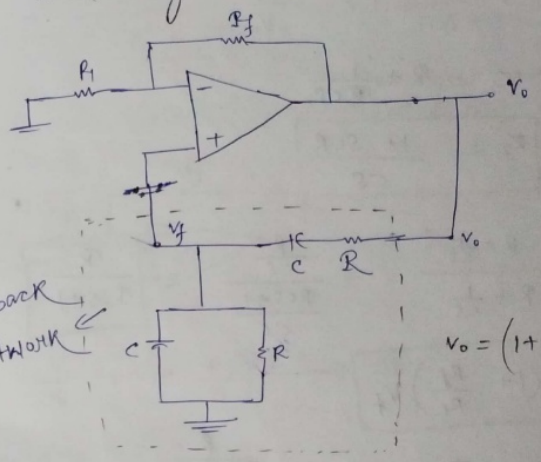
$$\Rightarrow \omega^2 = \frac{1}{6R^2C^2}$$

$$\Rightarrow \omega = \frac{1}{\sqrt{6}RC}$$

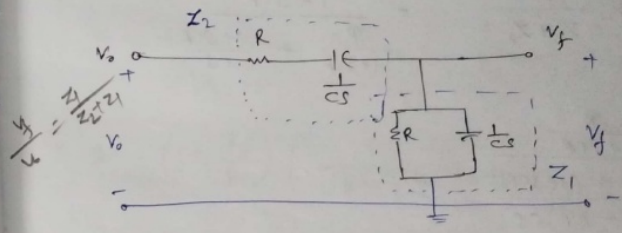
$$\Rightarrow 2\pi f = \frac{1}{\sqrt{6}RC} \Rightarrow \boxed{f = \frac{1}{2\pi\sqrt{6}RC}}$$

Exp # 11 Wein Bridge Oscillator.

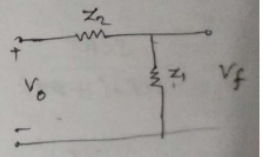
5 marks



$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_f$$



$$\frac{V_f}{V_o} = \frac{Z_1}{Z_1 + Z_2}$$



$$\frac{V_f}{V_o} = \frac{Z_1}{Z_1 + Z_2}$$

Now,

$$\omega^2 R^2 C^2 = \frac{1}{6}$$

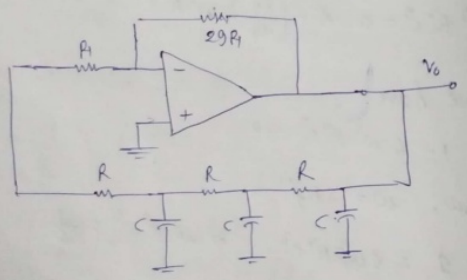
Equating imaginary part,

$$\left(\frac{R_f}{R_1}\right) \omega^3 R^3 C^3 = 5\omega RC - \omega^3 R^3 C^3$$

$$\Rightarrow \left(\frac{R_f}{R_1}\right) \omega^2 R^2 C^2 = 5 - \omega^2 R^2 C^2$$

$$\Rightarrow \frac{R_f}{R_1} \times \frac{1}{6} = 5 - \frac{1}{6} = \frac{30-1}{6} = \frac{29}{6}$$

$$\Rightarrow \boxed{R_f = 29 R_1}$$



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$$\beta V_o = V_f \Rightarrow \beta = \frac{V_f}{V_o}$$

Here,

$$Z_2 = R + \frac{1}{\beta CS}$$

$$\boxed{Z_2 = \frac{1 + SCR}{CS}}$$

$$Z_1 = \frac{R \times \frac{1}{CS}}{R + \frac{1}{CS}} = \frac{\frac{R}{CS}}{\frac{RCS+1}{CS}} = \boxed{\frac{R}{RCS+1}}$$

$$\boxed{V_o = \left(1 + \frac{R_f}{R_1}\right) V_f}$$

$$\Rightarrow \frac{V_f}{V_o} = \frac{Z_1}{Z_1 + Z_2} = \frac{\frac{R}{1+SCR}}{\frac{R}{1+SCR} + \frac{1+SCR}{CS}}$$

$$= \frac{\frac{R}{1+SCR}}{\frac{SCR + (1+SCR)^2}{(1+SCR)CS}}$$

$$= \frac{SCR}{SCR + (1+SCR)^2} = \frac{SCR}{SCR + 1 + S^2C^2R^2 + 2SCR}$$

$$= \frac{SCR}{S^2C^2R^2 + 3SCR + 1}$$

$$\frac{V_f}{V_o} = \frac{SCR}{S^2C^2R^2 + 3SCR + 1} = \frac{1}{SCR + 3 + \frac{1}{SCR}}$$

[ignoring SCR both in N^r & D^r] → (1)

$$\frac{V_o}{V_f} = \left(1 + \frac{R_f}{R_1}\right) \longrightarrow (2)$$

multiply eqn (1) & (2)

$$\frac{V_o}{V_f} \times \frac{V_f}{V_o} = \left(1 + \frac{R_f}{R_1}\right) \times \left(\frac{1}{j\omega CR + 3 + \frac{1}{j\omega CR}}\right) \quad [S = j\omega]$$

$$\Rightarrow 1 = \left(1 + \frac{R_f}{R_1}\right)\left(\frac{1}{j\omega CR + 3 + \frac{1}{j\omega CR}}\right)$$

$$\Rightarrow j\omega CR - \frac{j}{\omega CR} + 3 = 1 + \frac{R_f}{R_1}$$

$$\Rightarrow 3 + j\left(\omega CR - \frac{1}{\omega CR}\right) = \boxed{1 + \frac{R_f}{R_1}} \longrightarrow (3)$$

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equating eq^n (3)

$3 = 1 + \frac{R_f}{R_1}$, $WCR - \frac{1}{WCR} = 0$

$\Rightarrow \frac{R_f}{R_1} = 3-1$ $\Rightarrow WCR = \frac{1}{WCR}$

$= \omega^2 C^2 R^2 = 1$

$\Rightarrow \frac{R_f}{R_1} = 2$ $\Rightarrow \omega^2 = \frac{1}{R^2C^2}$

$\Rightarrow \boxed{R_f = 2R_1}$ $\Rightarrow \omega = \frac{1}{RC}$

$\Rightarrow 2\pi f = \frac{1}{RC}$

$\Rightarrow \boxed{f = \frac{1}{2\pi RC}}$

→ In wein bridge oscillator to sustain the oscillator R_f must be 2 times of R_1

power Amplifier.

and
- ① class - A power amplifier
- ② class - B "
- ③ class - AB "
- ④ class - C "
- ⑤ class - D "
- ⑥ class - E "

power Amplifier :-

→ An amplifier receives a signal from some a ~~larger~~ peak up translucent other input source and provide a larger version to some output device or another amplifier stage.

→ An input translucent signal is generally small and needs to be amplified sufficient to operate an output devices (speaker or other power handling devices)

→ In small signal amplifier the main factors are usually amplification linearity and magnitude of gain. ~~Source~~ Since signal voltage and current are small in a small signal amplifier, the amount of power handling capacity and power efficiency are little concerned.

(*) A voltage amplifier proves voltage amplification primarily to inc. the voltage of the input signal

(*) Large signal or power amplifier on the other hand primarily provide sufficient power to an output load to drive a speaker or other device., tipically a few ~~watts~~ watt, to tens of

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use to handle large voltage signal at moderate to high current levels.

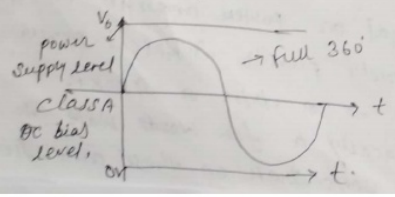
(vi) The main features of a large signal amplifier are the circuits power Efficiency the maximum amount of power that the circuit is capable of handling ~~that~~ and the impedence matching to the output devices.

(vii) One method used to catogerised amplifiers is by class.

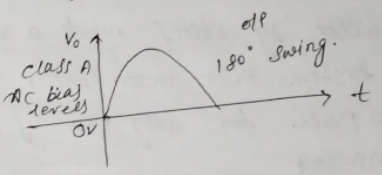
(viii) Basically amplifier class represent the amount of the output signal varies over one cycle of operation for a full cycle of amplifier.

Q. What is class A amplifier?

Ans:- The output signal varies for a ~~whole~~ full 360° of the cycle.



The fig. shows that this amplifier point to be biased at a level so that atleast half the signal swing of the output may vary up & down without going to a high enough voltage to be limited by the supply voltage level or too low to approach the lower supply level or 0V. in this description.



class B power amplifier

→ A class B circuit provides an output signal varying over one half the input signal cycle, or for 180° signal. The DC bias point for class B is 0V with the output then varying from this bias point for a half cycle. The output is not a faithful reproduction of the input if only one half cycle is present.

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possible to obtain a signal that varies over the full cycle to recreate the output from many pieces inputs signal.

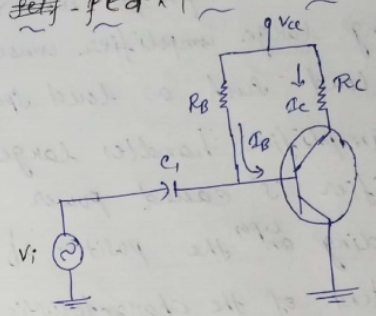
→ The measure advantages of class D operation is that the amplifier is on (using power) only for short intervals and the overall efficiency can practically be very hard.

Comparision of amplifier classes.

	AB	AB	B	C	D
operating cycle	360°	180°-360°	180°	< 180°	pulse operation
power Efficiency	20%-50%	between 25% (50%-78.5%)	78.5%	NO P.E	Tipically above 90%

class c is usally not used for delivery large amount of power thus the efficiency is not zero

~~Self~~ - fed series power class A Amplifier :-



The DC bias ~~fed~~ set by V_{CC} and R_B fixes then DC base-bias current are $I_B = \frac{V_{CC} - V_{BE}}{R_B}$

$$\Rightarrow \boxed{I_B = \frac{V_{CC} - 0.7V}{R_B}}$$

→ with the collector current, then be $\boxed{I_C = \beta I_B}$

→ with the collector Emitter voltage then ~~$V_{CC} = R_C$~~

$$\boxed{V_{CE} = V_{CC} - I_C R_C}$$

→ this simple fixed-bias circuit connection can be used to discuss the main features of a class A series-fed amplifier.

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→ A power amplifier is an amplifier which is capable of providing large ~~amplifier~~ amount of power to a load such as loud speaker. whenever the amplifier handles large single the amplifier is called power amplifier. Depanding ~~on~~ upon the position of Q-point and extend of the characteristic of power amplifiers are classifier various class of amplifier.

→ If the position of the Q point in the active region then it is class A amplifier. the conduction period of collector current is 360°. The theoritical conversion Efficiency and the practical conversion ~~effion~~ Efficiency of class amplificat° is 25%, If it is a transformer couple class A amplifier

In class B Amplifier :- The Q-point is present in the cutoff region

period of ~~con~~ collector current is 180°. Theoritical conversion Effiency of class B amplifier is ~~75%~~. 78.5%.

$$P_i(dc) = V_{dc} \times I_{dc}$$

$$P_o(ac) = I_{rms}^2 R_L$$

$$= \frac{V_{rms}^2}{R_L}$$

$$\text{conversion Efficiency } (\eta) = \frac{(P_o)_{ac}}{(P_i)_{dc}} = \frac{P_o}{P_i} \times 1$$

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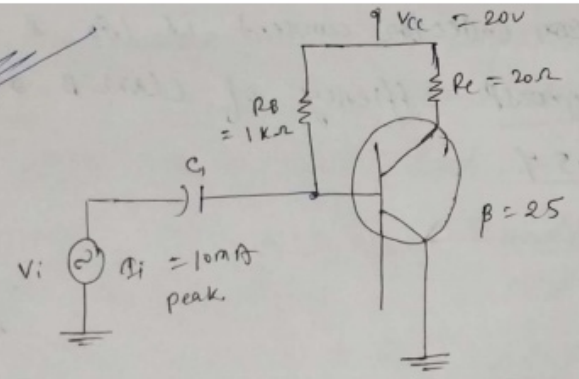
Imp



Calculate Input power, output power & efficiency of the above amplifier circuit ~~which~~ ~~result a~~ for a base current of 10 mA peak.

Soln:- Given :- $V_{CC} = 20V$, $R_B = 1K\Omega$, $R_c = 20\Omega$

$\beta = 25$, $I_b(peak) = 10mA$.

Input Loop

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$\Rightarrow I_B R_B = V_{CC} - V_{BE}$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_B = \frac{20 - 0.7}{1} \qquad \Rightarrow I_B = 19.3 mA.$$

$$I_{CQ} = \beta \times I_B = 25 \times 19.3 mA$$

$$= 482.5 mA \cong .48 A$$

$$\text{Input power} = P_i(dc) = V_{dc} \times I_{dc}$$

$$= V_{CC} \times 0.48 = \boxed{9.6 W}$$

$$I_b(peak) = 10 mA$$

$$I_c(peak) = \beta \times I_b(peak)$$

$$= 25 \times 10 mA$$

$$= 250 mA \text{ peak.}$$

$$I_c(rms) = \frac{I_c(peak)}{\sqrt{2}} = \boxed{\frac{250}{\sqrt{2}} mA}$$

$$P_o(ac) = I_{c\,rms}^2 \times R_C = \left(\frac{250mA}{\sqrt{2}}\right)^2 \times 20$$

$$= \frac{(250 \times 10^{-3})^2}{2} \times 20$$

$$\Rightarrow W = \frac{625000 \times 10^{-6}}{2} \times 20$$

$$\Rightarrow W = 625000 \times 10^{-6}$$

$$\Rightarrow \boxed{W = 0.625 \text{ watt}}$$

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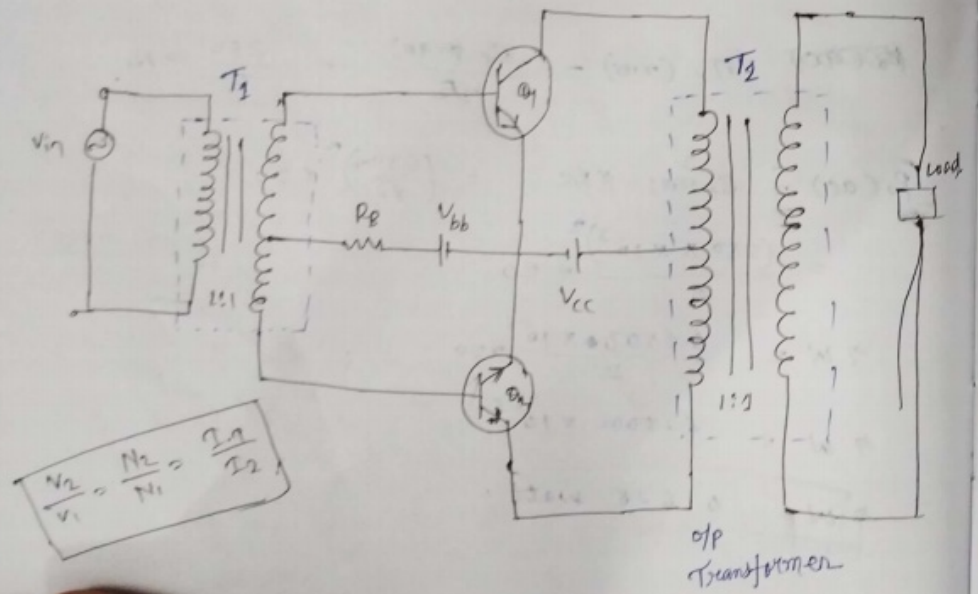
power Efficiency.

$$\eta\% = \frac{P_o(ac)}{P_i(dc)} \times 100\%$$

$$= \frac{0.625}{9.6} \times 100\%$$

$$= 6.5\%$$

Imp push-pull transformer coupled class B power Amplifier. (Two Transister)



For class B operation

$$I_{ac} = \frac{2}{\pi} I(P), \quad P_i(dc) = V_{cc} \times \frac{2}{\pi} I(P)$$

$$P_o(ac) = \frac{V_L^2(rms)}{R_L}$$

$$\text{maximum } P_o(ac) = \frac{V_{cc}^2}{2R_L}$$

$$\boxed{V_L(rms)_{max} = \frac{V_{cc}}{\sqrt{2}}}$$

Imp For a class B amplifier with $V_{cc} = 25V$ driving an 8Ω load. Determing, max. Input power, max output power, max efficiency

Ans:- given, $V_{cc} = 25V$, $R_L = 8\Omega$

(a) $P_i(dc) = V_{dc} \times I_{ac}$

$$= V_{cc} \times \frac{2}{\pi} I(P)$$

$$I_c(peak) = I(P) = \frac{V_{cc}}{R_L} = \frac{25}{8} = 3.125 A.$$

$$P_i(dc) = V_{cc} \times I_c(peak) \times \frac{2}{\pi}$$

$$= \boxed{25 \times \frac{2}{\pi} \times 3.125} = 49.74 W$$

$$P_o(ac) = \boxed{\frac{V_{cc}^2}{2R_L}} = \frac{(25)^2}{2 \times 8} = \frac{625}{16} = 39.06 W$$

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max. Efficiency $(\eta) = \frac{P_o(ac)}{P_i(dc)} \times 100\%$

$= \frac{39.66}{49.79} \times 100\%$

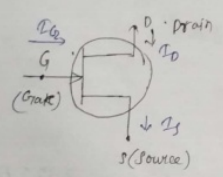
$= 78.5\%$

FET
- JFET
  - n channel JFET
  - p-channel JFET
- MOSFET

(unipolar)

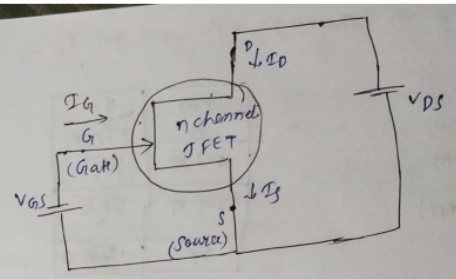
FET · Biasing (either e^- or hole)

→ fixed biasing



$I_G \simeq 0$

I_D = Drain current
I_S = Source current
Input impedance is necessary.



n channel → e^-
p chn → hole

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad \text{[Shockley's eqn]}$$

V_{GS} = Gate to Source voltage
V_P = pinch off voltage.
I_{DSS} = Drain to Source saturation current.

Imp ① Transfer characteristics (I_D vs V_{GS})
② Drain characteristics ($I_D \sim V_{DS}$).

(unipolar)
→ FET is a voltage control current device as here

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)$$ where, V_P is the pinch off voltage.

Here, the output drain current depends on the gate to source input voltage (V_{GS}). that's why FET is called voltage control device

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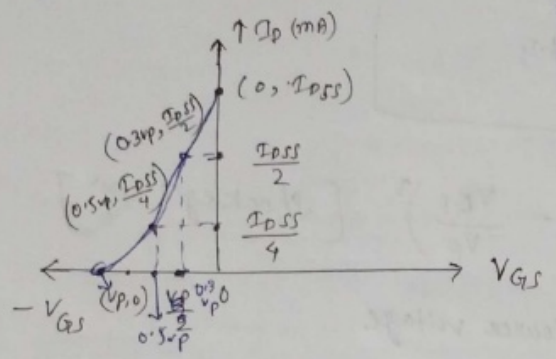
(1) Exam: putting $V_{GS} = 0$ in Shockley's eq^n we get $I_D = I_{DSS}$.

N-channel

V_{GS}	I_D
0	I_{DSS}
$-0.3\,V_P$	$\frac{I_{DSS}}{2}$
$-0.5\,V_P$	$\frac{I_{DSS}}{4}$
V_P	0



Step 2:- when $I_D = \frac{I_{DSS}}{2}$

$$\Rightarrow \frac{I_{DSS}}{2} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\Rightarrow \frac{1}{2} = \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\Rightarrow 1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{1}{2}}$$

$$\Rightarrow \frac{V_{GS}}{V_P} = 1 - \frac{1}{\sqrt{2}}$$

$$\Rightarrow V_{GS} = (1 - 0.707)V_P = \boxed{0.3\,V_P}$$

Step 3:- when $I_D = \frac{I_{DSS}}{4}$

$$\Rightarrow \frac{I_{DSS}}{4} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\Rightarrow \sqrt{\frac{1}{4}} = 1 - \frac{V_{GS}}{V_P}$$

$$\Rightarrow \frac{V_{GS}}{V_P} = 1 - \frac{1}{2} = \frac{1}{2} = \boxed{0.5}$$

$$\Rightarrow \boxed{V_{GS} = 0.V_P}$$

Imp

→ pinch-off voltage is defined as the ~~gat~~ two source voltage at which the drain current

Imp

prove that n-channel JFET Trans conductance

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{2}{|V_P|}\sqrt{I_D \times I_{DSS}}$$

Dem:- We know Shockley's eq^n

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \rightarrow (1)$$

Differenciating

$$\frac{\partial I_D}{\partial V_{GS}} = \frac{\partial}{\partial V_{GS}}\left(I_{DSS} - \left(1 - \frac{V_{GS}}{V_P}\right)^2\right)$$

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$$= 2 I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)\cdot\frac{d}{dV_{GS}}\left(1-\frac{V_{GS}}{V_P}\right)$$

$$\Rightarrow 2 I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)\times\left(-\frac{1}{V_P}\right)\times 1 \quad [V_{SG}=1]$$

$$\Rightarrow \frac{-2 I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right) \rightarrow (2)$$

$\Rightarrow$ from eq^n (1)

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

$$\Rightarrow \left(1-\frac{V_{GS}}{V_P}\right)^2 = \frac{I_D}{I_{DSS}}$$

$$\Rightarrow \left(1-\frac{V_{GS}}{V_P}\right) = \sqrt{\frac{I_D}{I_{DSS}}}$$

putting the value of $1-\frac{V_{GS}}{V_P}$ in eq^n (2)

$$g_m = -\frac{2 I_{DSS}}{V_P}\times\sqrt{\frac{I_D}{I_{DSS}}} = \frac{-2}{V_P}\sqrt{\frac{I_D\times I_{DSS}^2}{I_{DSS}}}$$

$$= -\frac{2}{V_P}\sqrt{I_D\times I_{DSS}}$$

$$\Rightarrow g_m = \frac{2}{|V_P|}\sqrt{I_D\times I_{DSS}} \quad [g_m = \text{Drain conductance}]$$

(1.) Define slew rate of OPAMP:

Ans: slew rate is defined as the maximum rate of change of an op-amp's output voltage, and is given in units of volts per microsecond. Slew rate is measured by applying a large signal step, such as one volt.

(2.) What is CMRR of OPAMP. Define CMRR

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Biasing is the setting of Initial operation condition (current & voltage) of an active device in an amplifier.

Many electronic devices such as diodes, transistor, vaccum tubes whose function is processing AC signal also require a steady that is DC current or voltage is a bias. This AC signal is applied to them is supper imposed on this DC bias current or voltage

output loop :-

$$\cancel{V_{DD} - I_D R_D - V_{DS} = 0}$$

$$V_{DS} + I_D R_D - V_{DD} = 0$$

$$\Rightarrow \boxed{V_{DS} = V_{DD} - I_D R_D}$$

Q.) When $\cancel{V_S = 0}$ $V_S = 0$, $R_G = 1 m\Omega$, $V_{DD} = 16V$, $R_D = 2 k\Omega$

$V_P = -8V$, $I_{DSS} = 10 mA$, find out what is V_{DS}; V_{GS}, V_S, I_D, V_G

$V_{DS} = V_D - V_S$

$V_{DS} = V_D - 0$

$\Rightarrow V_{DS} = V_D =$

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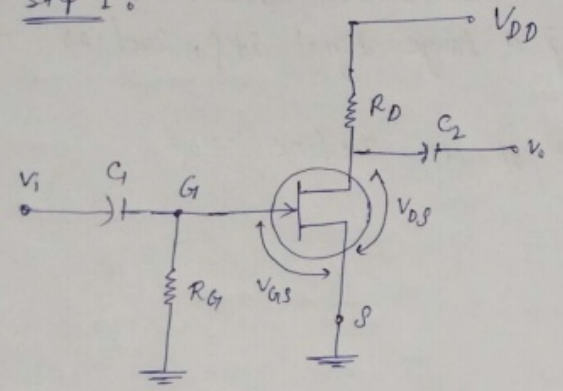
FET Biasing.

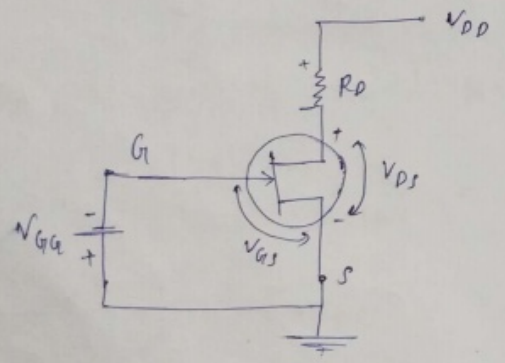
→ Fixed Biasing.

Step 1 :-



$I_G = 0\ A.$

Step 2 :-



Applying KVL into input section.

$$-V_{GG} - V_{GS} = 0$$

$$\Rightarrow \boxed{V_{GS} = -V_{GG}}$$

Biasing is the setting of initial operation condition (current & voltage) of an active device in an amplifier.

Many electronic devices such as diodes, transistor, vaccum tubes whose function is processing AC signal also require a steady that is DC current or voltage is a bias. This AC signal is applied to them is supper imposed on this DC bias current or voltage

output loop :-

$$\cancel{V_{DD} - I_D R_D - V_{DS} = 0}$$

$$V_{DS} + I_D R_D - V_{DD} = 0$$

$$\Rightarrow \boxed{V_{DS} = V_{DD} - I_D R_D}$$

Q.) When $V_S = 0$, $R_G = 1 m\Omega$, $V_{DD} = 16 V$, $R_D = 2 k\Omega$, $V_P = -8 V$, $I_{DSS} = 10 mA$, find out what is V_{DS}; V_{GS}, V_S, I_D, V_G

$V_{DS} = V_D - V_S$

$V_{DS} = V_D - 0$

$\Rightarrow V_{DS} = V_D =$

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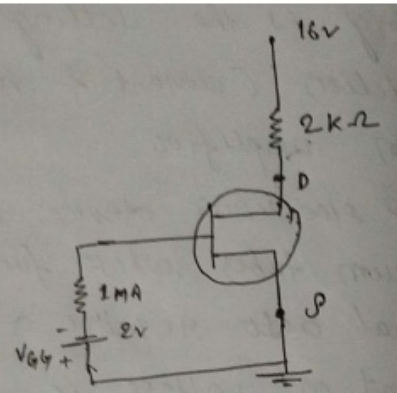
Soln:- $V_{GS} = -V_{GG}$

$\Rightarrow \boxed{V_{GS} = -2V}$



~~$V_{DS} = V_{DD} - I_D R_D$~~

~~$\Rightarrow V_{DS} = 16 -$~~

$\Rightarrow I_D = 10mA\left(1 - \frac{+2V}{+8V}\right)^2$

$= 10mA\left(1 - \frac{1}{4}\right)^2$

$= 10mA\left(\frac{4-1}{4}\right)^2 = 10mA\left(\frac{3}{4}\right)^2$

$= 10mA \times \frac{9}{16} = \frac{5}{2}mA \quad \frac{45}{8} = 5.625mA$

(iii) $V_{GS} = V_G - V_S$

$\Rightarrow -2V = V_G - 0$

$\Rightarrow \boxed{V_G = -2V}$

(iv) $\boxed{V_S = 0V}$ (Ground)

(v) Calculat^n of V_{DS}

$\Rightarrow V_{DS} = V_{DD} - I_D R_D$

$\Rightarrow V_{DS} = 16V - 5.625mA \times 2k\Omega$

$\Rightarrow = 16V - 5.625 \times 2V$

$= 16V - 11.24V$

$= 4.76V$

(vi) $V_{DS} = V_D - V_S$

$\Rightarrow 4.75 = V_D - 0$

$\Rightarrow V_D = 4.75V$

(13.) For a class B amplifier $V_{CC} = 25V$ driving 8Ω load determine.

(a.) Maximum input power.

(b.) Maximum output power.

(c.) Maximum circuit Efficiency

Soln:- Given data :-

$V_{CC} = 25V$, $R_L = 8\Omega$

find $P_i(dc) = ?$

$P_o(ac) = ?$

$\eta = ?$

→ Maximum input power.

$P_i(dc) = V_{dc} \times I_{dc}$

$P_i(dc) = V_{cc} \times \frac{2}{\pi}(I_{peak}) \longrightarrow \left[I_{dc} = \frac{2}{\pi}\right]$

$I_{peak} = \frac{V_{CC}}{R_L} = \frac{25}{8} = 3.125A$

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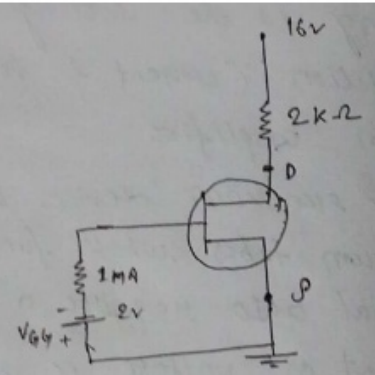
Soln:- $V_{GS} = -V_{GG}$

$\Rightarrow \boxed{V_{GS} = -2V}$



~~$V_{DS} = V_{DD} - I_D R_D$~~

~~$\Rightarrow V_{DS} = 16 -$~~

$\Rightarrow I_D = 10mA\left(1 - \frac{-2V}{-8V}\right)^2$

$= 10mA\left(1 - \frac{1}{4}\right)^2$

$= 10mA\left(\frac{4-1}{4}\right)^2 = 10mA\left(\frac{3}{4}\right)^2$

$= 10mA \times \frac{9}{16} = 5mA \frac{45}{8} = 5.625mA$

(iii) $V_{GS} = V_G - V_S$

$\Rightarrow -2V = V_G - 0$

$\Rightarrow \boxed{V_G = -2V}$

(iv) $\boxed{V_S = 0V}$ (Ground)

(v) Calculate of V_{DS}

$\Rightarrow V_{DS} = V_{DD} - I_D R_D$

$\Rightarrow V_{DS} = 16V - 5.625mA \times 2k\Omega$

$\Rightarrow = 16V - 5.625 \times 2V$

$= 16V - 11.24V$

$= 4.76V$

(vi) $V_{DS} = V_D - V_S$

$\Rightarrow 4.75 = V_D - 0$

$\Rightarrow V_D = 4.75V$

(13.) For a class B amplifier $V_{CC} = 25V$ driving an 8Ω load determine.

(a.) Maximum input power.

(b.) Maximum output power.

(c.) Maximum circuit Efficiency

Soln:- Given data :-

$V_{CC} = 25V$, $R_L = 8\Omega$

find $P_i(dc) = ?$

$P_o(ac) = ?$

$\eta = ?$

→ Maximum input power.

$P_i(dc) = V_{dc} \times I_{dc}$

$P_i(dc) = V_{cc} \times \frac{2}{\pi}(I_{peak}) \longrightarrow \left[I_{dc} = \frac{2}{\pi} I_{peak}\right]$

$I_{peak} = \frac{V_{cc}}{R_L} = \frac{25}{8} = 3.125\ A$

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$P_i(dc) = I_{peak} = 25 \times \frac{2}{3.14} \times 3.125$

$P_i(dc) = 49.76\ W.$

(2.) Maximum output power.

$P_o(dc) = \frac{V_{cc}^2}{2R_L} = \frac{(25)^2}{2\times 8} = \frac{625}{16} = 39.0625\ W.$

(3) Maximum circuit efficiency

$\eta = \frac{P_o(ac)}{P_i(dc)} = \frac{39.0625}{49.76} \times 100$

$\boxed{\eta = 78.50\%}$

(14) calculate the efficiency of a class B amplifier for a supply voltage of $V_{cc} = 22V$ during a 4Ω load with peak output voltage of

(a) $V_L(P) = 20V$

(b.) $V_L(P) = 4V$

Sol^n:- Given $V_{cc} = 22V$, $R_L = 4\Omega$, $V_L(P) = 20V$, $V_L(P) = 4V$

Find:- $\eta = \frac{P_o(dc)}{P_i(ac)} \times 100$

Solve:- $P_i(ac) = V_{dc} \times I_{dc} = V_{cc} \times \frac{2}{\pi} (I_{peak})$

$= 22 \times \frac{2}{3.14} \times 5.5$

$P_i(ac) = 77.07\ W$

$I_{peak} = \frac{V_{cc}}{R_L} = \frac{22}{4} = 5.5$

$P_o(dc) = \frac{V_{cc}^2}{2R_L} = \frac{(22)^2}{2\times 4} = \frac{484}{8} = 60.5\ W$

$\therefore \eta = \frac{P_o(dc)}{P_i(dc)} \times 100 = \frac{60.5}{77.07} \times 100$

$\eta = 78.5\%$

(16.) For class B power amplifier of fig. 15.36. calculate

(a.) Maximum $P_o(ac)$

(b.) Maximum $P_i(dc)$

(c.) Maximum $\%\eta$

(d.) Maximum power dissipated by both transistor. $V_{cc}(+30V)$

Sol^n:- given :- $V_{cc} = 30V$, $R_L = 8\Omega$, $-V_{EE} = -30V$

$P_i(dc) = V_{dc} \times I_{dc} = V_{cc} \times \frac{2}{\pi} \times \frac{V_{cc}}{R_L}$

$= 30 \times \frac{2}{3.14} \times \frac{30}{8}$

$\Rightarrow \boxed{P_i(dc) = 71.65\ W}$

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(ii) Max. $P_o(ac) = \frac{V_{cc}^2}{2R_L} = \frac{(30)^2}{2 \times 8} = \frac{900}{16} = \boxed{56.25\ W}$

(c) Maximum Efficiency $\% \eta = \frac{P_o(ac)}{P_i(dc)} \times 100$

$= \frac{56.25}{71.65} \times 100 = 78.5\%$

(d) Max. power dispicated by both ~~the~~ transistors

is $= P_i(dc) - P_o(ac) = 71.65 - 56.25$

$= \boxed{15.4\ W}$

(17.) If the input voltage to the power amplifier of fig. is 8 V_{rms} calculate:-

(i) $P_i(dc)$, (ii) $P_o(ac)$, (c) $\% \eta$

(d) power dissipated by both output transistor

Sol^n:- given :- $V_{CC} = 30V$, $-V_{CE} = -30V$, $R_L = 8\Omega$

$V_{rms} = 8$ $\quad V_{rms} = \frac{V_{cc}}{\sqrt{2}}$

(a) $P_i(dc) = V_{dc} \times I_{dc} = V_{cc} \times \frac{2}{\pi} \times \frac{V_{cc}}{R_L}$

$= 30 \times \frac{2}{3.14} \times \frac{V_{rms} \times \sqrt{2}}{R_L}$

$= 30 \times \frac{2}{3.14} \times \frac{8\sqrt{2}}{8} = 27.02\ W$

(b) $P_o(ac) = \frac{(V_{cc})^2}{2R_L} = \frac{(V_{rms} \times \sqrt{2})}{2R_L}$

$= \frac{(V_{rms})^2 \times 2}{2 \times R_L} = \frac{(8)^2}{8} = 8\ W$

(c) $\% \eta = \frac{P_o(ac)}{P_i(dc)} = \frac{8}{27.02} \times 100$

$= 29.6\%$

(d) $P_{2Q} = P_i(dc) - P_o(ac)$

$= 27.02 - 8 = 19.02\ W$

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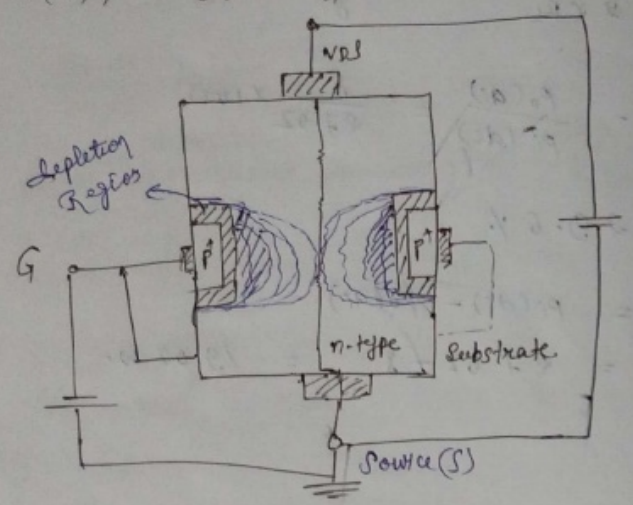
JFET

$p^+ \rightarrow$ heavily dopped
$p^- \rightarrow$ lightly dopped

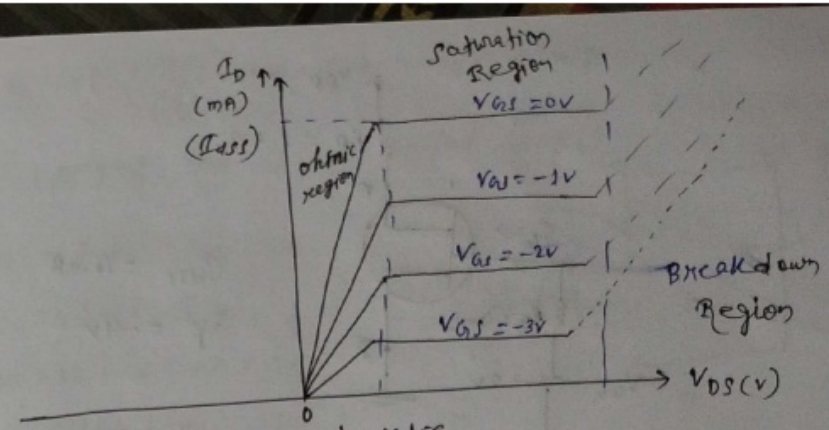
→ n-channel JFET



n-channel, $V_{GS} = -ve$, $V_{DS} = +ve$

The space between two p^+ region is know as the channal

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$



Drain characteristic.

Imp

Q.) Draw the transfer characteristics & Drain characteristic of n channal JFET and prove that $g_m = \frac{2}{|V_P|} = \sqrt{I_D \times I_{DSS}}$.

Q.) DC Biasing of JFET can be analysis by two method.

(1.) Mathematical analysis
(2.) Graphical analysis.

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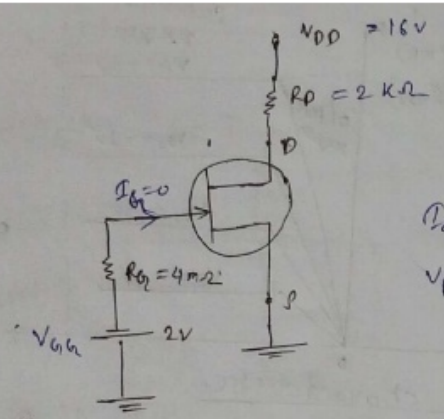


$I_{DSS} = 10mA$

$V_P = -4V$

Determine the following parameters of given circuit

(a.) V_{GSQ} (b.) I_{DQ} (c.) V_{DS} (d.) V_D (e) V_G (f) V_S

Sol^n:- Mathematical Analysis.

Applying KVL in ~~outp~~ i/p. output loop

$-2V - V_{GS} = 0$

$\Rightarrow \boxed{V_{GS} = -2V}$

The drain can be calculated by Schockley eq^n

Calculat^n of I_D

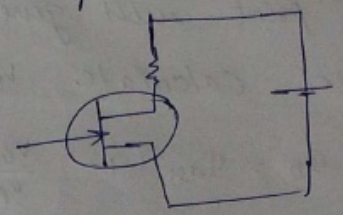
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$\rightarrow 10\left(1 - \frac{(-2)}{(-4)}\right)^2 = 10\left(1 - \frac{1}{2}\right)^2$

$= 10\left(\frac{2-1}{2}\right)^2$

$= \cancel{10\left(\frac{2}{4}\right)^2}$ $10 \times \frac{1}{4} = 2.5\ mA$

applying KVL in the output loop.



$V_{DD} - I_D R_D - V_{DS} = 0$

$\Rightarrow V_{DS} = V_{DD} - I_D R_D$

$\Rightarrow \cancel{V_{DS}} = 16 - 2.5mA \times 2K\Omega$

$V_{DS} = 16V - 5V = 11V$

$V_S = 0V$

$V_{GS} = V_G - V_S$

$\Rightarrow -2V = V_G - 0$

$\Rightarrow \boxed{V_G = -2V}$

$V_{DS} = V_D - V_S$

$\Rightarrow 11V = V_D - 0$

$\Rightarrow \boxed{V_D = 11V}$

Graphical Method

→ In graphical method. we have to draw the transfer characteristic ~~of~~ ~~one~~ curve and the load line. The eq^n which we get from the input loop is called the load line equat^n.

$V_G = -2V$

$\Rightarrow$

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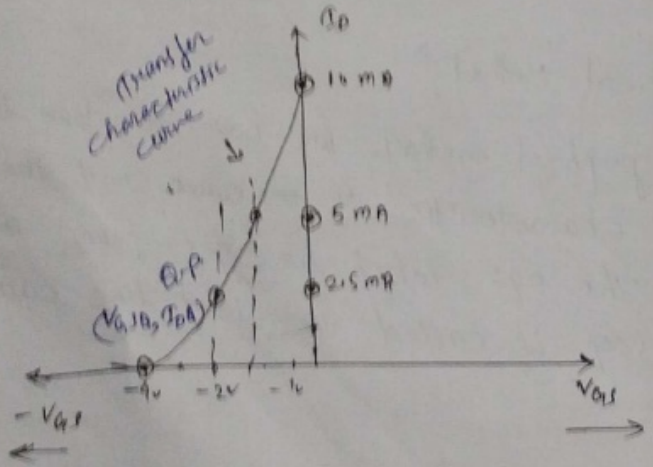
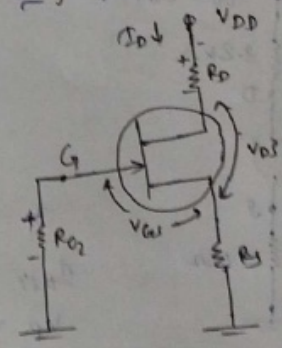
→ The intersection point of the transfer characteristic curve and the load line is the Q point. will give the value of I_{DQ} and V_{GSQ} then calculate V_{DS}.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

V_{GS}	I_D
0	$I_{DSS} = 10\,mA$
$.8\,V_P$ $= .8 \times -4 = -3.2\,V$	$\frac{I_{DSS}}{2} = 5\,mA$
$.5\,V_P$ $.5 \times -4 = -2\,V$	$\frac{I_{DSS}}{4} = 2.5\,mA$
$V_P = -4$	0



JFET Self Bias circuit.



Input

Applying KVL,

$$-V_{GS} - I_D R_D = 0$$

$$\Rightarrow V_{GS} = -I_D R_S$$

calculate of I_D

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\Rightarrow I_D = I_{DSS}\left(1 - \frac{(-I_D R_S)}{V_P}\right)^2$$

$$\Rightarrow \boxed{I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2}$$

calculate of output loop eqn

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$\Rightarrow V_{DS} = V_{DD} - I_D R_D - I_D R_S$$

$$\Rightarrow V_{DS} = V_{DD} - I_D (R_D + R_S)$$

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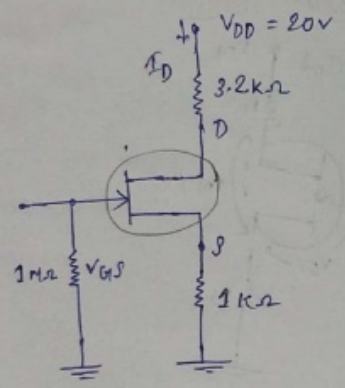

$I_D = 4mA$

$I_{DSS} = 8mA$

$V_P = -6V$

Determine V_{GS}, I_D, V_{DS}, V_G, V_D, V_S

Soln:- $V_{GS} = -I_D R_D$

$= -(4mA) \times 1k\Omega = -4V$

$V_{DS} = V_{DD} - I_D(R_D + R_S)$

$= 20 + 4(3.2 + 1)$

$= 20 + 4 \times 4.2 = 20 + 16.8 = 18.8V$

V_G

$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$= 8\left(1 - \frac{(-4)}{(-6)}\right)^2$

$= 8\left(1 - \frac{2}{3}\right)^2$

$= 8\left(\frac{3-2}{3}\right)^2 = 8\left(\frac{1}{3}\right)^2 = 8 \times \frac{1}{9} = \frac{8}{9}$

$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$= 8\left(1 - \frac{(-4)}{(-6)}\right)^2$

$= 8\left(1 - \frac{4}{6}\right)^2 = 8\left(\frac{6-4}{6}\right)^2$

$= 8 \times \left(\frac{2}{6}\right)^2$

$= 8 \times \frac{4}{36}$

$= 8 \times 10^{-3}\left(1 - \frac{4}{6}\right)^2$

Graphical Method

V_{GS}	I_D
0	8 mA
$-3V - 6 = -1.8V$	4mA
$-5V - 6 = -3V$	2 mA
$-6V$	0

Load line eqn

Applying KVL in the i/p loop,

$-V_{GS} - I_D R_S = 0$

$\Rightarrow V_{GS} = -I_D R_S$

V_{GS}	I_D
0	0
$-4V$	$\frac{I_{DSS}}{2} = 4mA$

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$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$

$\Rightarrow V_{DS} = V_{DD} - I_D (R_D + R_S)$

$= 20 - 2.6\,mA\,(3.3+1)\,k\Omega$

$= 20 - 2.6 \times 4.3$

$= 8.82\,V$

$V_S - I_D R_S = 0$

$\Rightarrow V_S = I_D R_S = 2.6\,mA \times 1\,k\Omega$

$= 2.6\,V$

$V_{GS} = V_{GS} + V_S$

$= -2.6\,V + 2.6\,V$

$= 0\,V$

$V_{DS} = \cancel{V_{DD} + V_S}\ V_D - V_S$

$\Rightarrow V_D = V_{DS} + V_S = 8$

Mathematical Analysis

From i/p Loop.

$V_{GS} = -I_D R_S$

$= -I_D \times 1\,k\Omega$

$= -I_D$

calculation of I_D

Shockley's eqn

$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$\Rightarrow I_D = 8\left(1 - \frac{-I_D}{-6}\right)^2$

$= 8\left(1 - \frac{I_D}{6}\right)^2$

$= 8\left(\frac{6 - I_D}{6}\right)^2$

$= \frac{8}{36}(1 - I_D)^2$

$36 I_D = 8\{6^2 + I_D^2 - 2.6 I_D\}$

$= 8\{36 + I_D^2 - 12 I_D\}$

$\Rightarrow \frac{36}{8} I_D = 36 + I_D^2 - 12 I_D$

$\Rightarrow 4.5 I_D = 36 + I_D^2 - 12 I_D$

$\Rightarrow I_D^2 - 12 I_D - 4.5 I_D + 36 = 0$

$\Rightarrow I_D^2 - 16.5 I_D + 36 = 0$

$\Rightarrow$ root $= \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$

$I_D = \frac{-(-16.5) \pm \sqrt{(-16.5)^2 - 4 \cdot 1 \cdot 36}}{2 \times 1}$

$\left\{ \begin{array}{l} a = 1 \\ b = -16.5 \\ c = 36. \end{array} \right.$

$I_{D1} = 2.587\,mA$

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$I_{D2} = 13.91$ mA

$I_{D2} > I_{DSS}$ which is not acceptable as $I_{DD} = 8$ mA

$I_{DQ} = 2.578 \simeq 2.6$ mA.

calculation of V_{GSQ}

$$V_{GSQ} = -I_D \times R_D$$
$$= -2.6\text{mA} \times 1\text{k}\Omega$$
$$= -2.6\text{V}$$

calculation of V_{DS}

In op side,

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$
$$\Rightarrow V_{DS} = V_{DD} - I_D (R_S + R_D)$$
$$= 20\text{V} - 2.6\text{mA}\,(1+3.3)\text{k}\Omega$$
$$= 20\text{V} - 2.6 \times 4.3$$
$$= 8.82\text{V}$$

calculation of V_D :-

$$V_{DS} = V_D - V_S$$
$$V_D = V_{DS} + V_S$$
$$= 8.82 + 2.6$$
$$= 11.42\text{V}$$

calculation of V_S

$$V_S = I_D R_S$$
$$= 2.6\text{mA} + 1\text{k}\Omega$$
$$= 2.6\text{V}$$

calculation of V_G

$$V_G = 0\text{V}$$

Common Gate configuration (CG)

Common Drain configuration

Common source configuration / source follower ckt

$$i_D = f(V_{GS}, V_{DS})$$
$$= \frac{\partial i_D}{\partial V_{GS}} \times \nabla V_{GS} + \frac{\partial i_D}{\partial V_{DS}} \times \nabla V_{DS}$$

$$\boxed{i_D = g_m V_{gs} + \frac{1}{r_d} V_{ds}}$$

$$\frac{1}{r_d} = \frac{\partial i_D}{\partial V_{DS}}$$

$$g_m = \frac{\partial i_D}{\partial V_{GS}}$$ = trans conductance.

r_d = drain resistance

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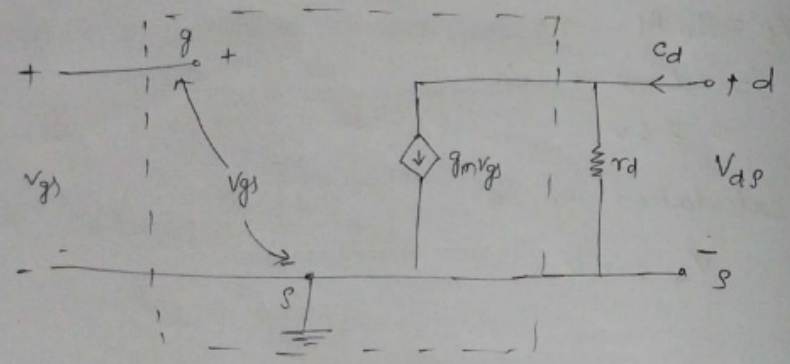
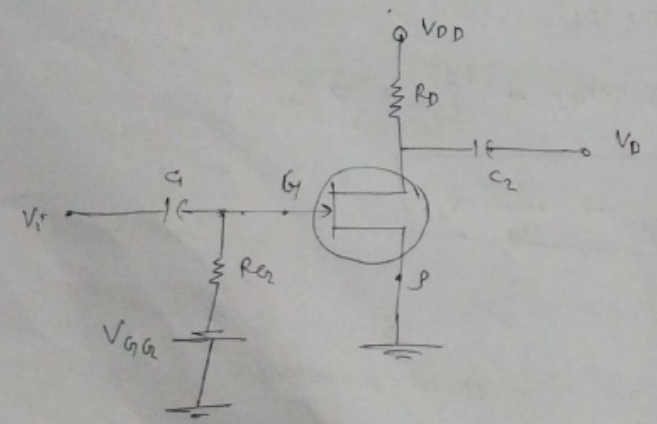
Small signal model of JFET



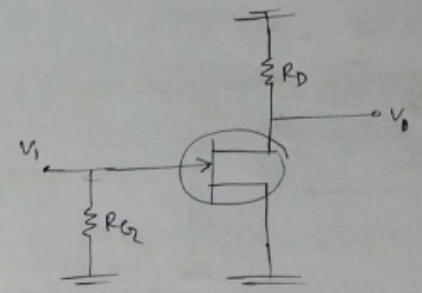
Small Signal analysis of JFET fixed bias ckt

→ In JFET current gain is ~~zero~~ Infinite.

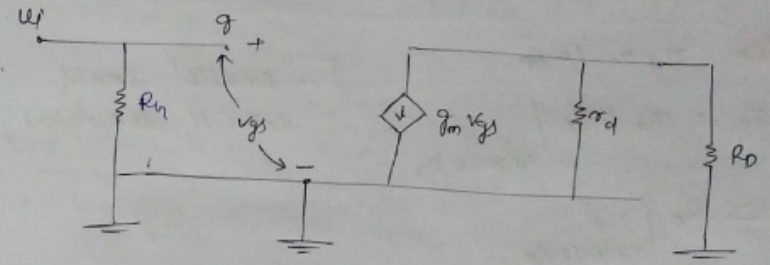
JFET Fixed Bias ckt.



Step 1 :- DC voltage grounded capacitor short circuited



Step 2 :- Now N-channel JFET symbol with its Small signal model.



(AC Equivalent ckt of JFET fixed ckt)

Calculation of Z_i

$Z_i = R_G$

Calculation of Z_o

The output impedence can be determined by applying

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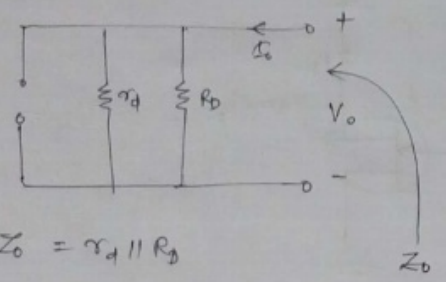
a voltage V_o at the output terminal which results a current I_o with $V_i = 0$



$Z_o = r_d \parallel R_D$

$V_i = 0$, R_G short ckted.

$V_{gs} = 0$, then $g_m V_{gs} = 0$

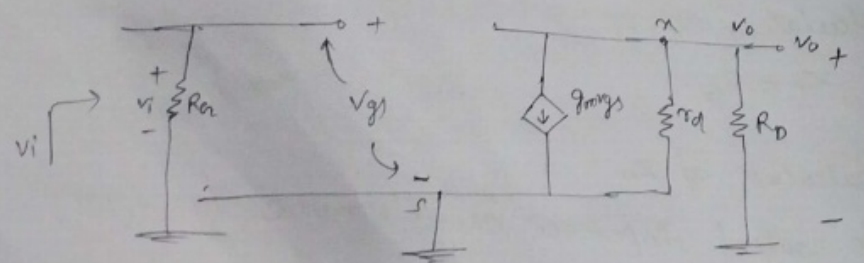
i.e open circuited.

when $r_d \geq 10 R_D$

$Z_o = r_d \parallel R_D \Big|_{r_d \geq 10 R_D}$ [in parallel small value is dominated]

$\simeq R_D \Big|_{r_d \geq 10 R_D}$

calculation of voltage Gain (A_v)



at node n

$$\frac{V_o - 0}{R_D} + \frac{V_o - 0}{r_d} + g_m V_{gs} = 0$$

$$\Rightarrow V_o\left(\frac{1}{R_D} + \frac{1}{r_d}\right) = -g_m V_{gs}$$

Applying KVL in the i/p loop.

$$V_i - V_{gs} = 0$$

$$\Rightarrow \boxed{V_i = V_{gs}}$$

$$V_o\left(\frac{1}{R_D} + \frac{1}{r_d}\right) = -g_m V_i$$

$$\Rightarrow \frac{V_o}{V_i} = \frac{-g_m}{\frac{1}{R_D} + \frac{1}{r_d}} = -g_m (R_D \parallel r_d)$$

$$\boxed{A_v = \frac{V_o}{V_i} = -g_m (r_d \parallel R_D)}$$

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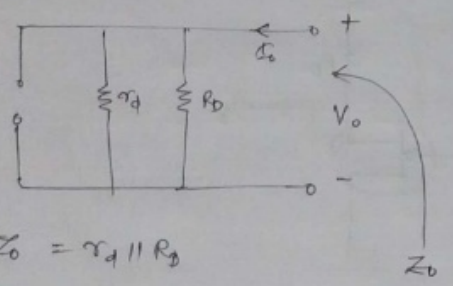
a voltage V_o at the output terminal which results a current I_o with $V_i = 0$



$Z_o = r_d \parallel R_D$

$V_i = 0$, R_G short ckted,

$V_{gs} = 0$, then $g_m V_{gs} = 0$

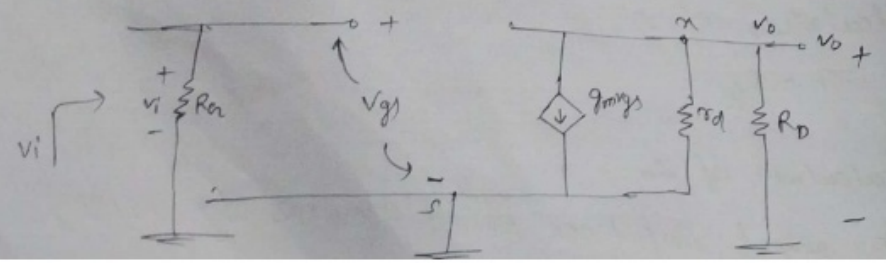
i.e open circuited

when $r_d \geq 10 R_D$

$Z_o = r_d \parallel R_D \Big|_{r_d \geq 10 R_D}$ [in parallel small value is dominated]

$\simeq R_D \Big|_{r_d \geq 10 R_D}$

calculation of voltage Gain (A_v)



at node x

$$\frac{V_o - 0}{R_D} + \frac{V_o - 0}{r_d} + g_m V_{gs} = 0$$

$$\Rightarrow V_o\left(\frac{1}{R_D} + \frac{1}{r_d}\right) = -g_m V_{gs}$$

Applying KVL in the i/p loop.

$$V_i - V_{gs} = 0$$

$$\Rightarrow \boxed{V_i = V_{gs}}$$

$$V_o\left(\frac{1}{R_D} + \frac{1}{r_d}\right) = -g_m V_i$$

$$\Rightarrow \frac{V_o}{V_i} = \frac{-g_m}{\frac{1}{R_D} + \frac{1}{r_d}} = -g_m (R_D \parallel r_d)$$

$$\boxed{A_v = \frac{V_o}{V_i} = -g_m (r_d \parallel R_D)}$$

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SCR (Silicon controlled rectifier)

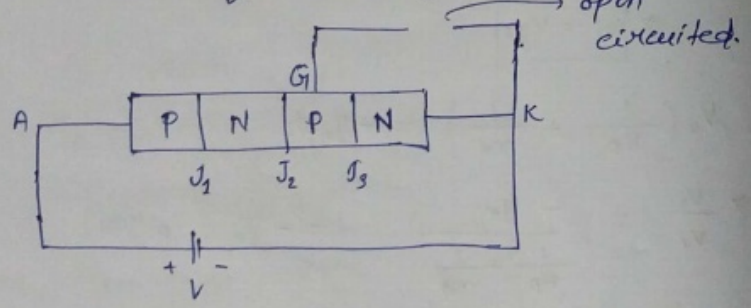
→ Modes of operation in SCR

(i) Forward Blocking Mode (off State)

(ii) Forward conducting Mode (on State)

(iii) Reverse Blocking Mode (off State)

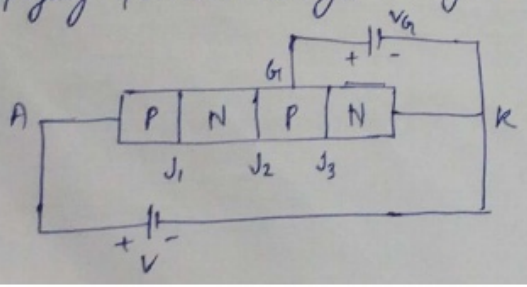
(i) Forward Blocking Mode (off State)



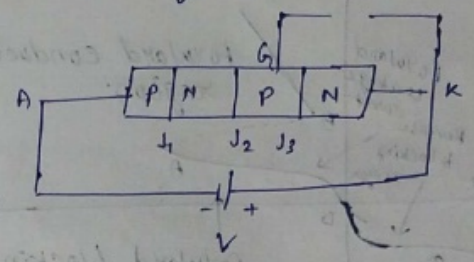
(ii) Forward conducting Mode (on State)

(i) By increasing the forward bias voltage applied between anode and cathode beyond the breakdown voltage

(ii) By applying positive voltage at gate terminal



(iii) Reverse Blocking Mode (on



V-I characteristics of SCR

→ The V-I characteristics of SCR is shown in the fig. The horizontal line in the below fig represents the amount of voltage applied cross of SCR whereas the vertical line represents the amount of current flows in the SCR.

V_A = Anode voltage, I_A = Anode current,

$+V_A$ = Forward anode voltage, $+I_A$ = Forward anode ~~current~~ current.

$-V_A$ = Reverse anode voltage, $+I_A$ = Reverse anode current.

The V-I characteristics of SCR is divided into three regions.

(i) Forward blocking region.

(ii) Forward conduction region.

(iii) Forward blocking region.

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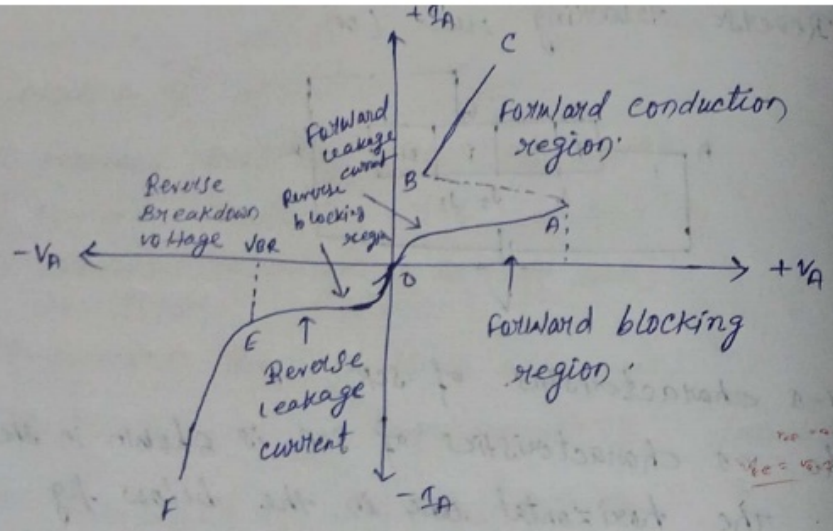
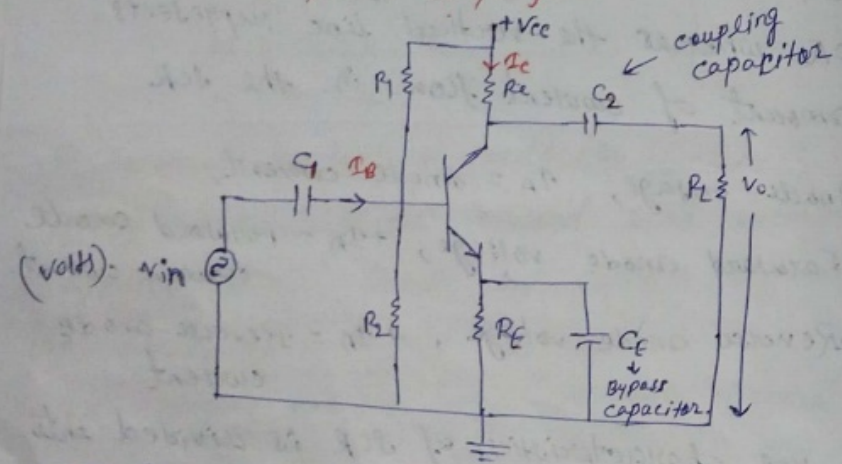
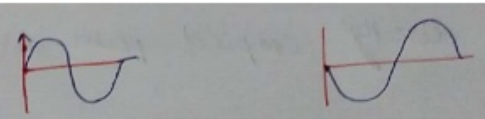


Class A power Amplifier



→ Directly coupled, single ended.



current gain.

Working

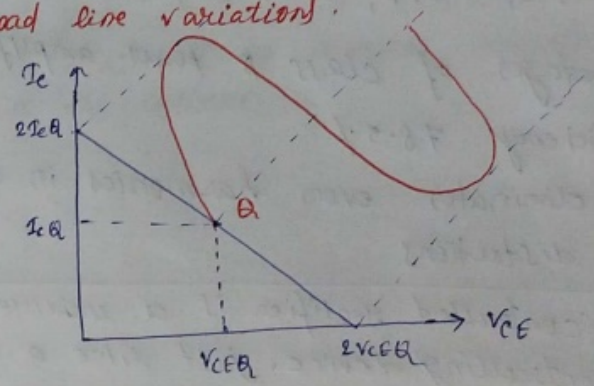
(i) During +ve half cycle of i/p = $I_C = \beta I_B$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Dec. const.

(ii) During -ve half cycle of i/p = $I_B \downarrow$, $I_C \downarrow$, $V_{CE} = \uparrow$

AC load line variations.



Characteristics of power Amplifier

→ o/p current flow for entire cycle

→ operating of amplifier restricted to smaller central region.

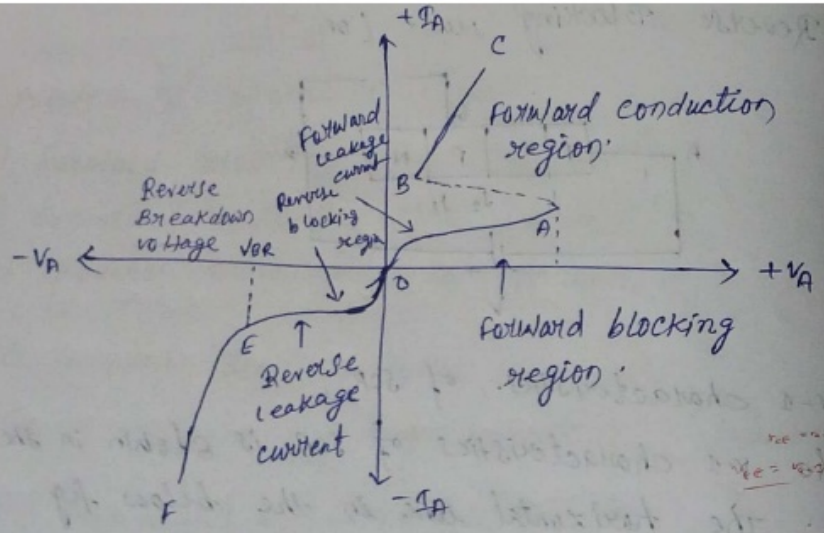
→ output is same as that of i/p

→ A.C o/p power per active transistor is less.

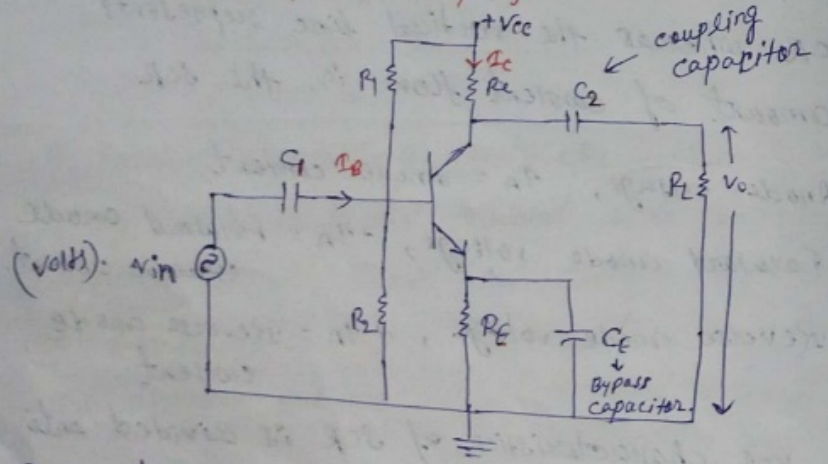
→ overall efficiency.

$$\eta_o = \frac{\text{A.C power delivered to load}}{\text{D.C i/p power.}}$$

Scanned with OKEN Scanner



Class A power Amplifier



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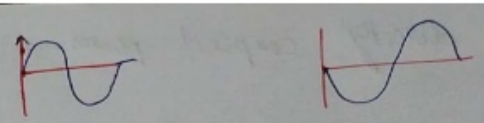

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Dec. const.

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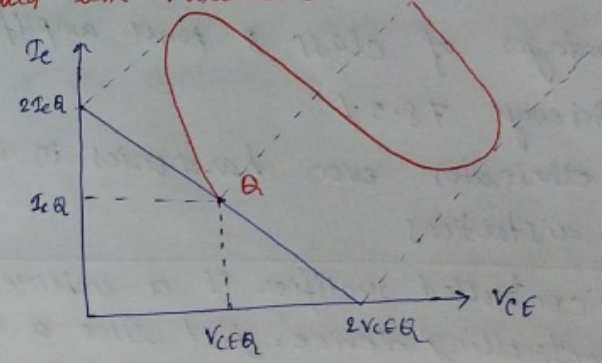

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$$\eta_o = \frac{\text{A.C power delivered to load}}{\text{D.C i/p power.}}$$

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→ Efficiency is 25% directly coupled power-A Amplifier

class B power Amplifier.

During the +ve half cycle :-

$Q_1 \rightarrow ON$, $Q_2 \rightarrow OFF$, = +ve output

During -ve half cycle

$Q_2 \rightarrow ON$, $Q_1 \rightarrow OFF$, = -ve output.

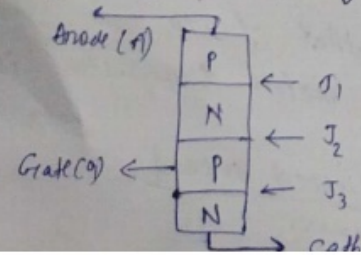
Advantages of class B power amplifier

→ Efficiency 78.5%

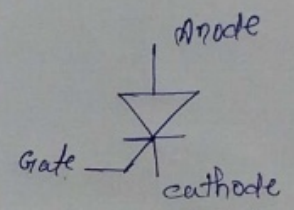
→ It eliminates even harmonics in a.c op

→ less distortions

Silicon controlled rectifier is a unidirectional current controlling device. just like a normal p-n junction diode, it allows electric current only in one direction and blocks electric current in another direction. SCR is made up of 4 semi-conductor layers of alternating p and N type material



SCR Symbols.



The anode terminal of SCR diode is connected to the first p-type material of a PNPN structure, cathode terminal is connected to the last n-type material, and gate terminal is connected to the second p-type material of a PNPN structure which is nearest to the cathode.

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