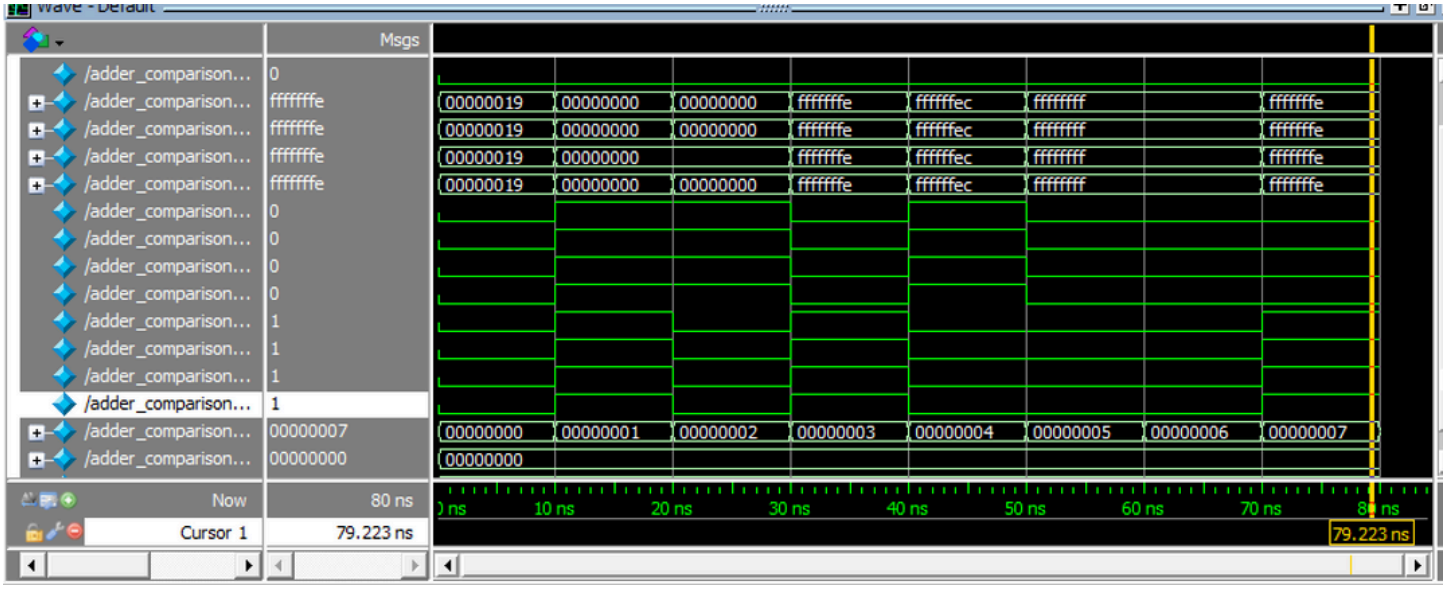
VLSI Project

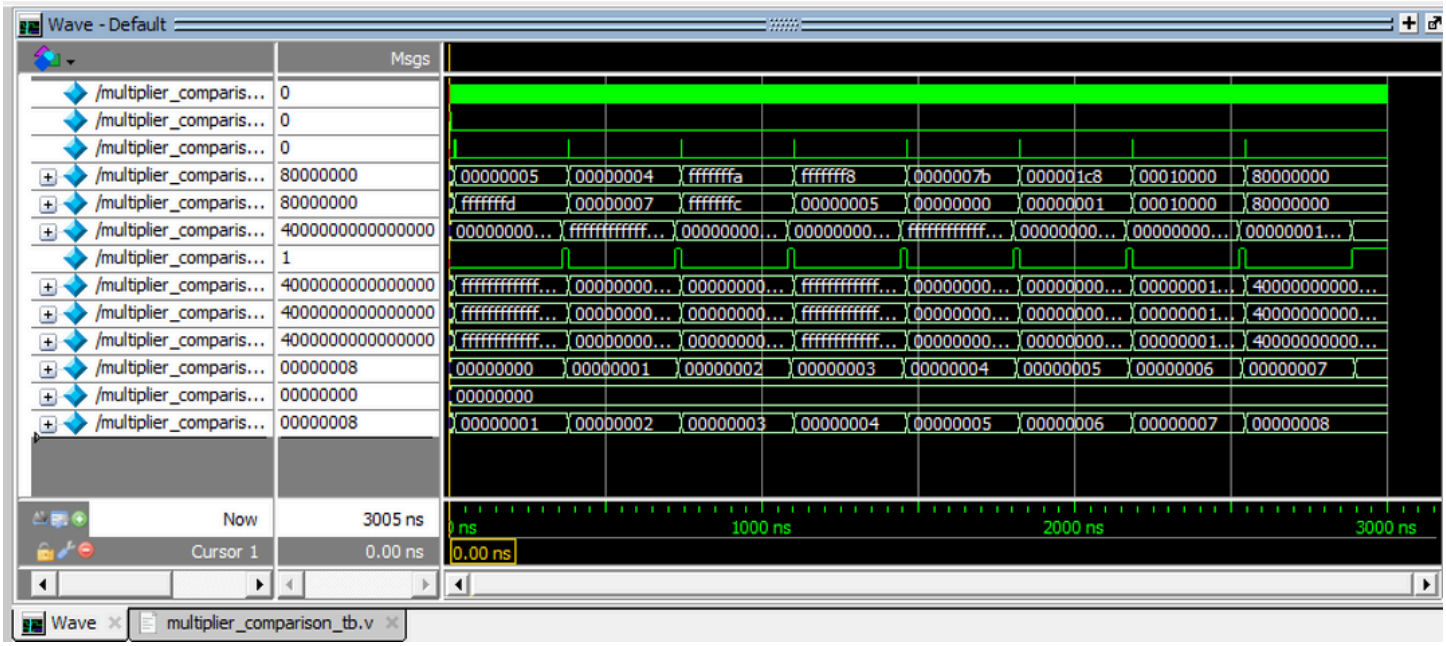
Adders




```
# === Adder Comparison Test ===
# TestCase#1: success - All adders match expected result
# TestCase#2: success - All adders match expected result
# TestCase#3: success - All adders match expected result
# TestCase#4: success - All adders match expected result
# TestCase#5: success - All adders match expected result
# TestCase#6: success - All adders match expected result
# TestCase#7: success - All adders match expected result
# TestCase#8: success - All adders match expected result
#
# === Final Report ===
# Total Test Cases: 8
# Successful Tests: 8
# Failed Tests: 0
```

	Synthesize			Placement and Routing		
Adder	Area	Utilization	Max Delay	Area	Utilization	Max Delay clock - slack -hold
Carry select adder	1729.16	0.404595	8.5333	1611.55	0.348108	20 - 6.1096 ~ 14
Ripple Carry Adder	1739.168	0.405012	8.3124	1548.99	0.360723	20 - 6.9561 ~ 13.05
Carry Look Ahead Adder	1591.52	0.30964	8.4555	1446.39	0.281402	20 - 6.9774 ~ 13.03
Carry bypass Adder	1750.4288	0.407634	8.4444	1569	0.365385	20 - 7.1668 ~12.85

Multipliers




```
# TestCase#1: success - ALL multipliers match expected result
# TestCase#2: success - ALL multipliers match expected result
# TestCase#3: success - ALL multipliers match expected result
# TestCase#4: success - ALL multipliers match expected result
# TestCase#5: success - ALL multipliers match expected result
# TestCase#6: success - ALL multipliers match expected result
# TestCase#7: success - ALL multipliers match expected result
# TestCase#8: success - ALL multipliers match expected result
#
# === Final Report ===
# Total Test Cases: 8
# Successful Tests: 8
# Failed Tests: 0
```

	Synthesize			Placement and Routing		
Multiplier	Area	Utilization	Max Delay	Area	Utilization	Max Delay
Normal (*)	11341	0.603373	28.1164	126734	0.649945	40 - 24.2824 ~ 16
Multiplier Tree (dadda)	76641.00	0.602562	15.9672	74888.1	0.58878	40 - 10.1746 ~30
Sequential Multiplier	23906	0.60448	31.2680	22390.2	0.566136	40 - 29.9043 ~ 10
Booth Algorithm	13446	0.602741	23.4551	152721	0.664294	40 - 17.1180 ~ 23

NOTES:

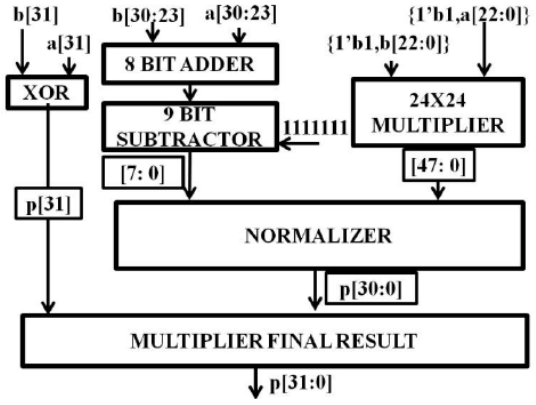
- areas are in um2
- utilization is in percentages
- delay in ns

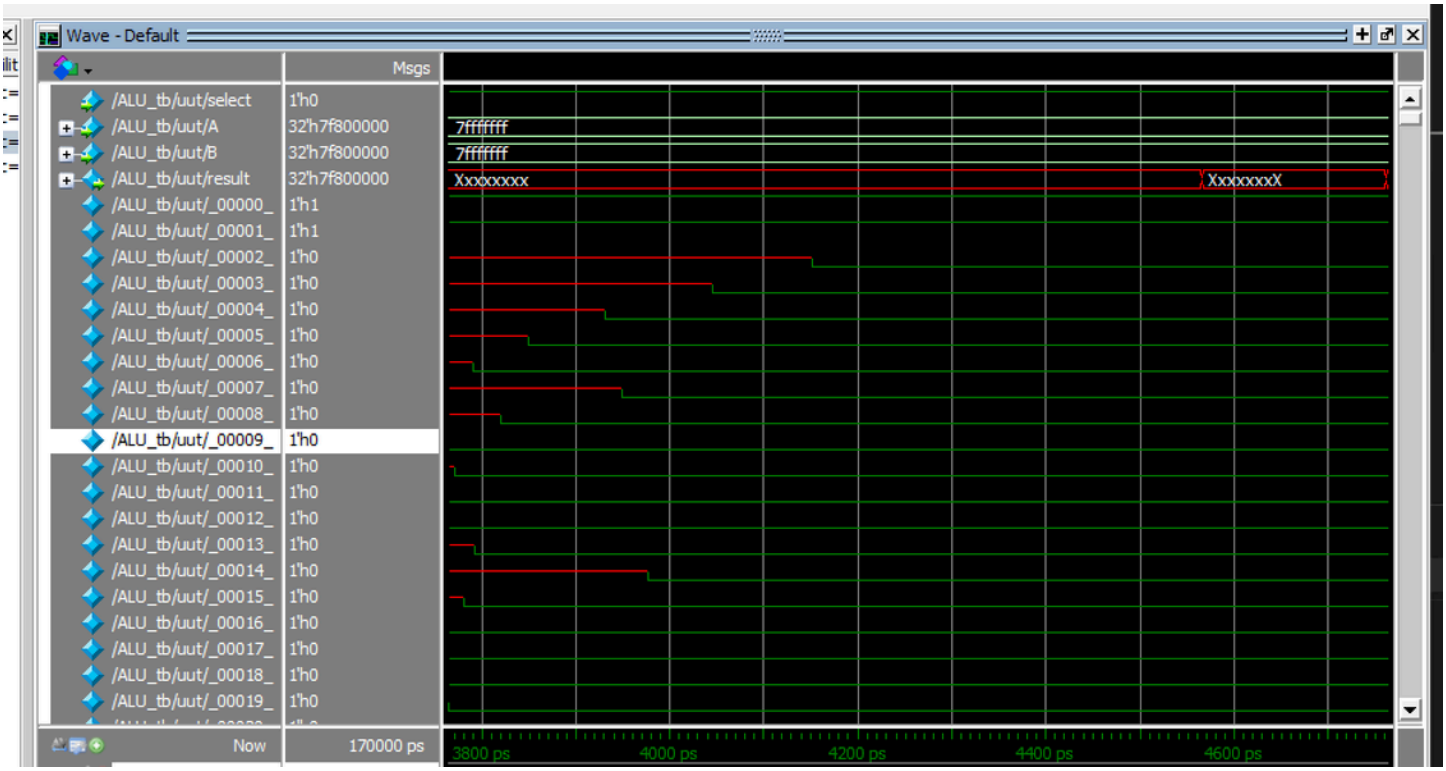
ALU Design

Implementing a floating point ALU:

– adder: using Carry-ByPass Adder as it's the best delay from our results.

– Multiplier using the normal multiplier (2nd best Area of a non-sequential multiplier)





Area	Utilization	Total Power	Timing Hold Worst Slack Corner nom_tt_025C_1v80	Timing Setup Worst Corner nom_tt_025C_1v80	Clock	Setup Worst Slack
48296.3	0.59031	0.00429	0.8920727742331439	17.647954708228387	35	1.2181

Presented by

- Amir Anwar
- Sarah Ahdy
- Bishoy Wadea
- Peter Safwat