FastEdge™ Series

CY2DP314

1 of 2:4 Differential Fanout Buffer

Features

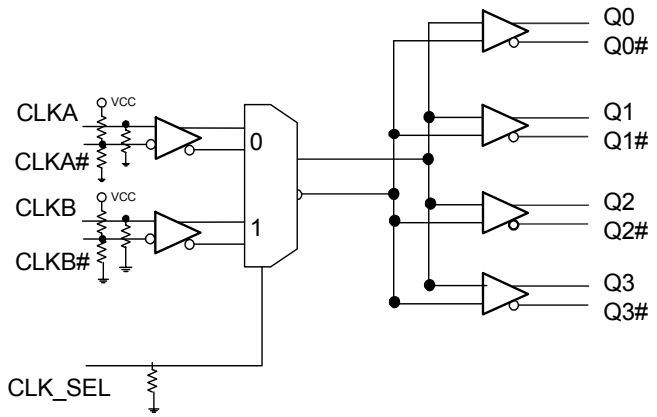
- **Four ECL/PECL differential outputs**
- **Two ECL/PECL and HSTL differential inputs**
- **Hot-swappable/-insertable**
- **50-ps output-to-output skew (typical)**
- **100-ps device-to-device skew (typical)**
- **Less than 1-ps RMS typical jitter**
- **500-ps propagation delay (typical)**
- **Operation from DC to above 1.5 GHz**
- **PECL and HSTL mode supply range: V_{CC} = 2.375V to 3.465V with V_{EE} = 0V**
- **ECL mode supply range: V_{EE} = –2.375V to –3.465V with V_{CC} = 0V**
- **Industrial temperature range: –40°C to 85°C**
- **20-pin SSOP package**
- **Temperature compensation as 100K ECL**

Description

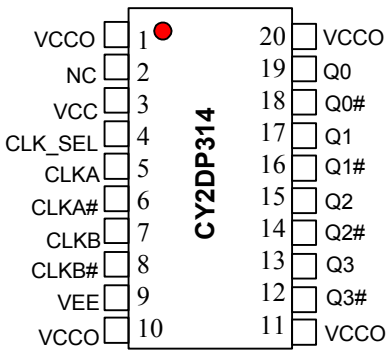
The CY2DP314 is a low-skew, low propagation delay 2-to-4 differential fanout buffer targeted to meet the requirements of high-performance clock and data distribution applications. The device is implemented on SiGe technology and has a fully differential internal architecture that is optimized to achieve low signal skews at operating frequencies of up to 1.5 GHz (full swing).

The device features two differential input paths that are multiplexed internally. This mux is controlled by the CLK_SEL pin. The CY2DP314 may function not only as a differential clock buffer but also as a signal level translator and fanout an LVCMOS/LVTTL single-ended signal to four ECL/PECL differential loads. Since the CY2DP314 introduces negligible jitter to the timing budget, it is the ideal choice for distributing high-frequency, high-precision clocks across backplanes and boards in communication systems. Furthermore, advanced circuit design schemes, such as internal temperature compensation, ensure that the CY2DP314 delivers consistent, guaranteed performance over differing platforms.

Block Diagram



Pin Configuration



20 pin SSOP

Pin Description

Pin	Name	I/O	Type	Description
1,10,11,20	VCCO	+PWR	Power	**Output power supply**
2	NC			**No connect**
3	VCC	+PWR	Power	**Power supply, positive connection**
4	CLK_SEL	I,PD	ECL/PECL	**pull down, selects between CLKA; pull up for CLKB signals**
5,6	CLKA, CLKA#	I,PD[1] I,PC	ECL/PECL	**Default differential clock input pair**
7,8	CLKB, CLKB#	I,PD I,PC	ECL/HSTL	**Alternate differential clock input pair**
9	VEE[2]	–PWR	Power	**Power supply, negative connection**
18,16,14,12	Q[0:3]#	O,OE	ECL/PECL	**Complement output**
19,17,15,13	Q[0:3]	O,OE	ECL/PECL	**True output**

Table 1.

Control	Operation
CLK_SEL	
0	Default condition (no connection to the pin)
0	CLKA, CLKA# input pair is active. CLKA can be driven with ECL or PECL compatible signals with respective power configurations.
1	CLKB, BLKB# input pair is active. CLKB can be driven by HSTL compatible signals with respective power configurations.

Governing Agencies

The following agencies provide specifications that apply to the CY2DP314. The agency name and relevant specification is listed below.

Table 2.

Agency Name	Specification
JEDEC	JESD 51 (Theta JA) JESD 8-6 (HSTL) JESD 8-2 (ECL) JESD 65-A (skew,jitter)
IEEE	1596.3 (Jitter specs)
UL	94 (Flammability rating)
Mil-Spec	883E Method 1012.1 (Thermal Theta JC)

Notes:

1. In the I/O column, the following notation is used: I = Input, O = Output, PD = Pull-down, PU = Pull-up, PC = Pull-center, O = output, OE = open emitter and PWR = Power.
2. In ECL mode (negative power supply mode), V_{EE} is either –3.3V or –2.5V and V_{CC} is connected to GND (0V). In PECL mode (positive power supply mode), V_{EE} is connected to GND (0V) and V_{CC} is either +3.3V or +2.5V. In both modes, the input and output levels are referenced to the most positive supply (V_{CC}) and are between V_{CC} and V_{EE}.

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{CC}	Supply Voltage	Non-functional	–0.3	4.6	VDC
V_{CC}	Operating Voltage	Functional	2.5 – 5%	3.3 + 5%	VDC
I_{BB}	Output Reference Current	Relative to V_{BB}	–	200	uA
VTT	Output Termination Voltage	VTT = 0V for V_{CC} = 2.5V	–	V_{CC}–2	VDC
V_{IN}	Input Voltage	Relative to V_{CC}	–0.3	V_{CC}+0.3	VDC
V_{OUT}	Output Voltage	Relative to V_{CC}	–0.3	V_{CC}+0.3	VDC
LU_I	Latch-up Immunity	Functional	300		mA
T_S	Temperature, Storage	Non-functional	–65	+150	°C
T_A	Temperature, Operating Ambient	Functional	–40	+85	°C
T_J	Temperature, Junction	Non-functional	–	150	°C
$Ø_{Jc}$	Dissipation, Junction to Case	Functional			°C/W
$Ø_{Ja}$	Dissipation, Junction to Ambient	Functional	40	60	°C/W
ESD_h	ESD Protection (Human Body Model)		2000		V
M_{SL}	Moisture Sensitivity Level				N.A.
G_{ATES}	Total Functional Gate Count	Assembled Die	50		Each
FLM	Flammability Rating		V0		N.A.

PECL/HSTL DC Specifications (V_{CC} = 2.5V ± 5% or V_{CC} = 3.3 V ± 5%,VEE = GND, Temp. = Ð40ûC to 85ûC)

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Voltage, Low		V_{CC} – 1.945	–	V_{CC}–1.625	V
V_{IH}	Input Voltage, High		V_{CC}–1.165	–	V_{CC}–0.880	V
I_{IN}	Input Current[3]	V_{IN} = [V_{ILMIN} = 2.406V or V_{IHMAX} =1.655V] at V_{CC}=3.465V	–	–	|150|	uA
Clock Input Pair CLKA, $\overline{\text{CLKA}}$ (PECL Differential Signals)						
V_{PP}	Differential input voltage[4]	Differential operation	0.1	–	1.3	V
V_{CMR}	Differential cross point voltage[5]	Differential operation	1.2	–	V_{CC}	V
I_{IN}	Input Current[3]	V_{IN} = [V_{ILMIN} = 2.406V or V_{IHMAX} = 1.655V] at V_{CC} = 3.465V	–	–	|200|	uA
Clock Input Pair CLKB, $\overline{\text{CLKB}}$ (HSTL Differential Signals)						
V_{DIF}	Differential input voltage[6]		0.4	–	1.9	V
V_X	Differential crosspoint voltage[7]		0.68	–	0.9	V
I_{IN}	Input Current	V_{IN} = Vx ± 0.2V	–	–	|150|	uA
PECL Outputs Q0–Q3, $\overline{\text{Q0–Q3}}$ (PECL Differential Signals)						
V_{OH}	Output High Voltage	IOH = –30 mA[8]	V_{CC}–1.2	–	V_{CC}–0.7	V
V_{OL}	Output Low Voltage V_{CC} = 3.3V ± 5% V_{CC} = 2.5V ± 5%	IOL = –5 ma [8]	V_{CC}–1.945 V_{CC} –1.945	–	V_{CC}–1.5 V_{CC}–1.3	V

Notes:
3. Input have internal pullup/pulldown or biasing resistors which affect the input current.
4. VPP (DC) is the minimum differential input voltage swing required to maintain device functionality
5. VCMR (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the VCMR (DC) range and the input swing lies within the VPP (DC) specification.
6. VDIF (DC) is the amplitude of the differential HSTL input voltage swing required for device functionality.
7. VX (DC) is the crosspoint of the differential HSTL input signal. Functional operations is obtained when the crosspoint is within the VX (DC) range and the input swing lies within the VPP (DC) specification.
8. Equivalent to a termination of 50 Ω to VTT.

PECL/HSTL DC Specifications (V_{CC} = 2.5V ± 5% or V_{CC} = 3.3 V ± 5%,VEE = GND, Temp. = Ð40ûC to 85ûC)(continued)

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
Supply Current						
I_{EE}	Max. Quiescent Supply Current without output termination current[9]	VEE pin	–	–	130	mA

ECL DC Specifications (V_{EE} = –2.5V ± 5% or V_{EE} = –3.3 V± 5%, V_{CC} = GND, T_A = Ð40¡C to 85¡C)

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Voltage, Low		–1.945	–	–1.625	V
V_{IH}	Input Voltage, High	Define V_{CC} and load current	–1.165	–	–0.880	V
I_{IN}	Input Current[10]	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$, V_{CC} = 3.465V	–	–	|200|	uA
Clock Input Pair CLKA, $\overline{CLKA}$ (ECL Differential Signals)						
V_{PP}	Differential input voltage[11]	Differential operation	0.1	–	1.3	V
V_{CMR}	Differential cross point voltage[12]	Differential operation	V_{EE}+1.2	–	–0.3	V
I_{IN}	Input Current[10]	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$,V_{CC} = 3.465V	–	–	|200|	uA
ECL Outputs Q0–Q3, $\overline{Q0–Q3}$ (ECL Differential Signals)						
V_{OH}	Output High Voltage	I_{OH} = –30 mA[13]	–1.2	–	–0.7	V
V_{OL}	Output Low Voltage V_{EE} = –3.3V ± 5% V_{EE} = –2.5V ± 5%	I_{OL} = –5 ma[13]	–1.945 –1.945	–	–1.5 –1.3	V
Supply Current						
I_{EE}	Maximum Quiescent Supply Current without output termination current[9]	V_{EE} pin	–	–	130	mA

AC Specifications ([ECL:V_{EE} = –3.3 VDC ± 5% or V_{EE} = –2.5V±5%, V_{CC} = GND] or [HSTL/PECL:V_{CC} = 3.3V ± 5% or V_{CC} = 2.5V±5%, V_{EE} = GND] Temp = Ð40¡C to 85¡C) [14]

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
Clock Input Pair CLKA, $\overline{CLKA}$ (PECL or ECL Differential Signals)						
V_{PP}	Differential input voltage [15]	Differential operation	0.1	–	1.3	V
V_{CMR}	Differential cross point voltage [16]	Differential operation	VEE+1.0	–	–0.3	V
F_{CLK}	Input Frequency [17]	50% duty cycle Standard load	–	–	2200	MHz
T_{PD}	Propagation Delay CLKA or CLKB to Q0–Q3 pair	660-MHz 50% duty cycle Standard load Differential Operation	280	400	750	ps
Clock Input Pair CLKB, $\overline{CLKB}$ (HSTL Differential Signals)						
V_{DIF}	Differential input voltage[18]	660-MHz 50% duty cycle Standard load Differential Operation	0.4	–	1.9	V
V_X	Differential cross point voltage[19]	660-MHz 50% Standard load Differential Operation	0.68	–	0.9	V

Notes:
9. Power Calculation: V_{CC} * I_{EE} + 0.5 (I_{OH} + I_{OL})(V_{OH} - V_{OL})(number of differential outputs used)
10. Input have internal pullup / pulldown or biasing resistors which affect the input current.
11. VPP (DC) is the minimum differential input voltage swing required to maintain device functionality.
12. VCMR (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the VCMR (DC) range and the input swing lies within the VPP (DC) specification.
13. Equivalent to a termination of 50 Ω to VTT.
14. AC characteristics apply for parallel output termination of 50 Ω to VTT.
15. VPP (AC) is the minimum differential ECL/PECL input swing required to maintain AC characteristics including tpd and device-to-device skew.
16. VCMR (AC) is the crosspoint of the differential ECL/PECL input signal. Normal AC operation is obtained when the crosspoint is within the VCMR(AC) range and the input swing lies within the VPP(AC) specification. Violation of VCMR(AC) or VPP(AC) impacts the device propagation delay, device and part-to-part skew.
17. The CY2DP314 is fully operational up to 1.5 GHz with full PECL swing. Reduced swing up to TBD GHz.
18. VDIF (AC) is the minimum differential HSTL input voltage swing required to maintain AC characteristics including tkpd and device-to-device skew
19. VX(AC) is the crosspoint of the differential HSTL input signal. Normal AC operation is obtained when the crosspoint is within the VX(AC) range and the input swing lies within the VDIF(AC) specification. Violation of VX(AC) or VDIF(AC) impacts the device propagation delay, device and part-to-part skew.

AC Specifications ([ECL:V_{EE} = –3.3 VDC ± 5% or V_{EE} = –2.5V±5%, V_{CC} = GND] or [HSTL/PECL:V_{CC} = 3.3V ± 5% or V_{CC} = 2.5V±5%, V_{EE} = GND] Temp = Ð40¡C to 85¡C)(continued)[14]

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
F_{CLK}	Input Frequency	50% duty cycle Standard load Differential Operation	–	–	2200	MHz
T_{PD}	Propagation Delay CLKA or CLKB to Q0–Q3 pair	660-MHz 50% duty cycle Standard load Differential Operation	280	400	750	ps
ECL Clock Outputs (Q0–3, Q0–3) (Differential)						
$Vo_{(P-P)}$	Differential output voltage (peak-to-peak)	Differential PRBS fo < 50 MHz fo < 0.8 GHz fo < 1.0 GHz	 0.45 0.4 0.375	–	–	V
tsk(o)	Output-to-output skew	50% duty cycle Standard load Differential Operation	–	–	50	ps
tsk(PP)	Output-to-output skew (part-to-part)	50% duty cycle Standard load Differential Operation	–	–	500	ps
$t_{JIT(CC)}$	Output cycle-to-cycle jitter (Intrinsic)	50% duty cycle Standard load Differential Operation	–	–	1	ps rms
tsk(P)	Output pulse skew[20]	50% duty cycle Standard load Differential Operation	–	–	50	ps
tr, tf	Output Rise/Fall time	50% duty cycle Differential 20%–80%	–	–	0.3	ns
TTB	Total Timing Budget	660-MHz 50% duty cycle Standard load	–	–	250	ps
D_j	Deterministic/Intrinsic Jitter	50% duty cycle Standard load	–	–	1	ps rms

Timing Definitions

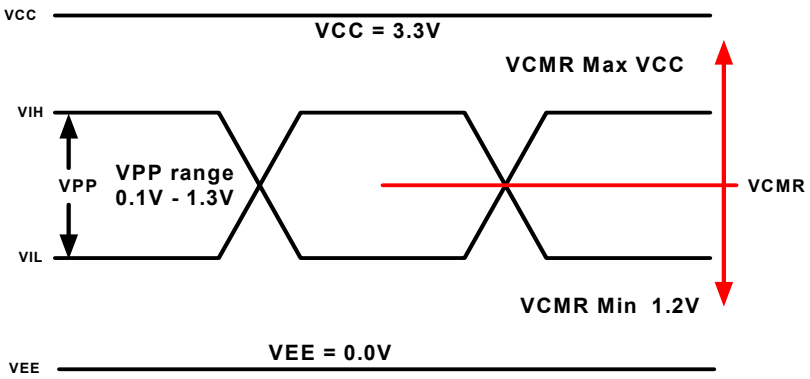


Figure 1. PECL Waveform Definitions

Note:
20. Output pulse skew is the absolute difference of the propagation delay times: | tPLH – tPHL |.

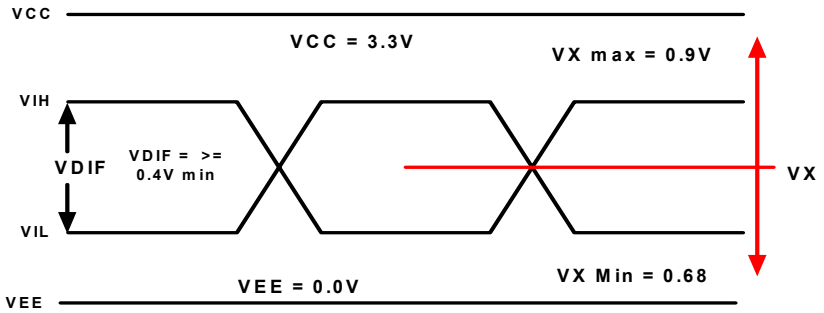


Figure 2. HSTL Differential Waveform Definitions

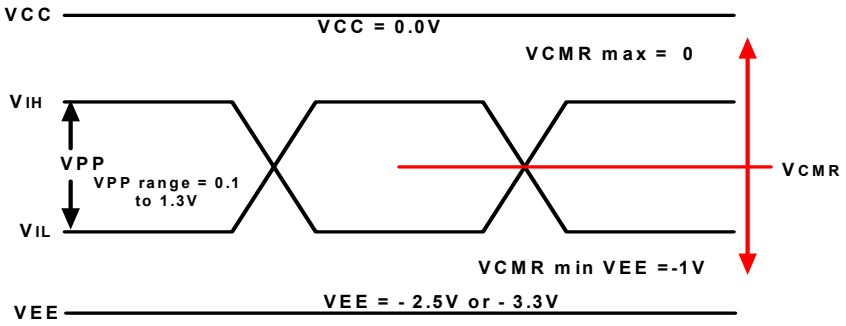


Figure 3. ECL Differential Waveform Definitions

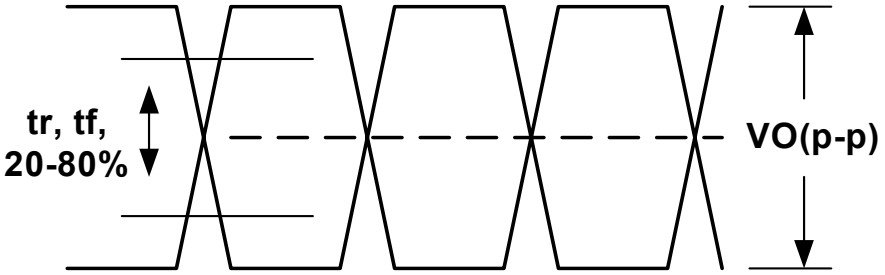


Figure 4. ECL/LVPECL Output

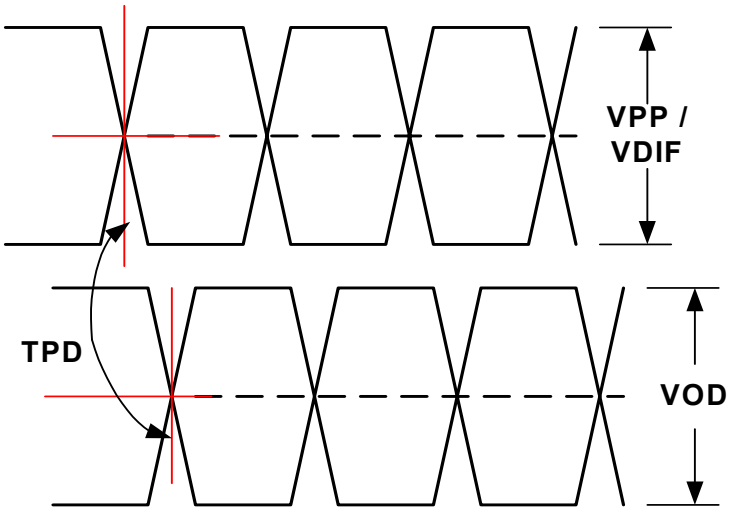
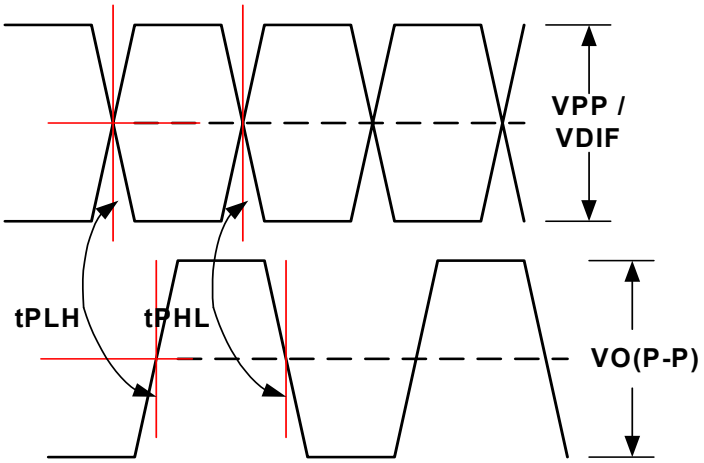


Figure 5. TPD Propagation Delay of Both CLKA or CLKB to Q0–Q3 Pair PECL/ECL/HSTL to PECL/ECL



tsk(P) Output pulse skew
= | tPLH - tPHL |

Figure 6. Output Pulse Skew

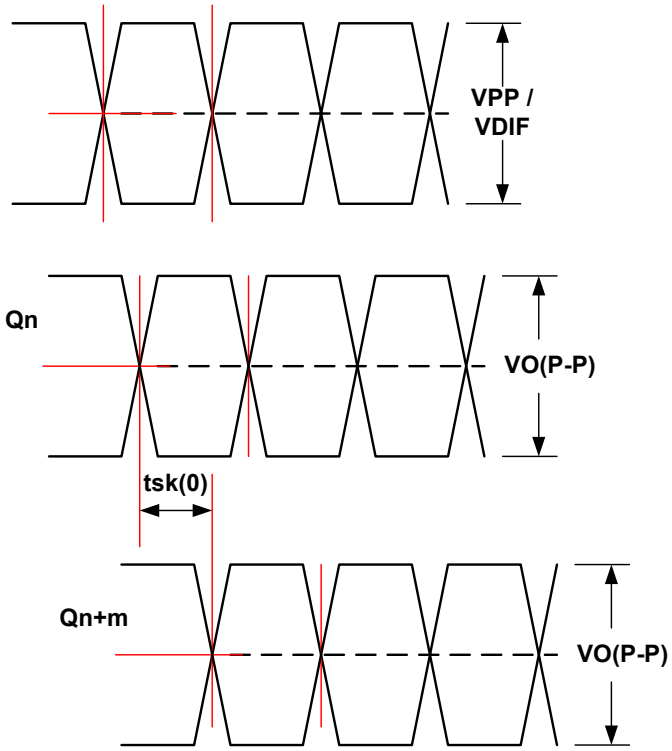


Figure 7. Output-to-Output Skew

Test Configurations

Standard test load using a differential pulse generator and differential measurement instrument.

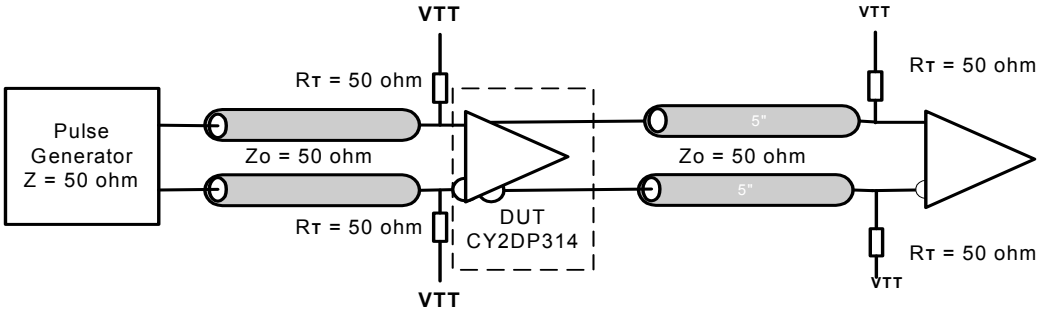


Figure 8. CY2DP314 AC Test Reference

Applications Information

Termination Examples

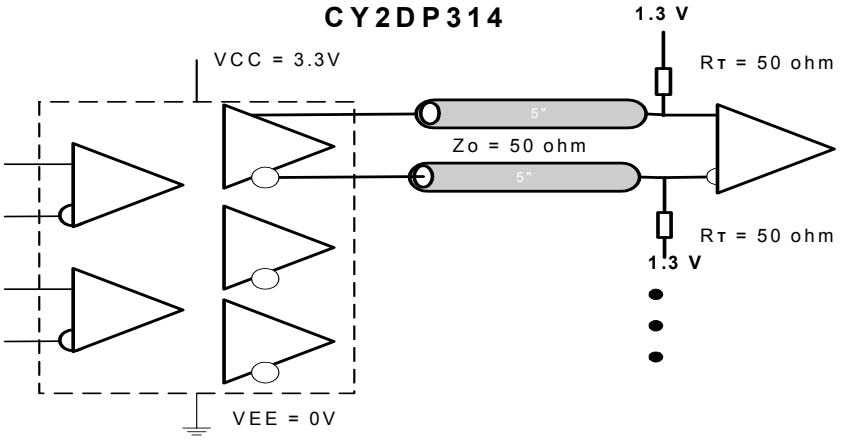


Figure 9. Standard LVPECL – PECL Output Termination

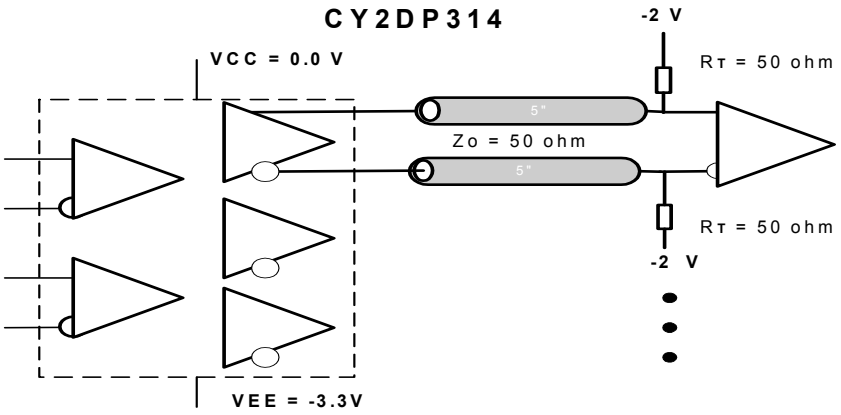


Figure 10. Standard ECL Output Termination

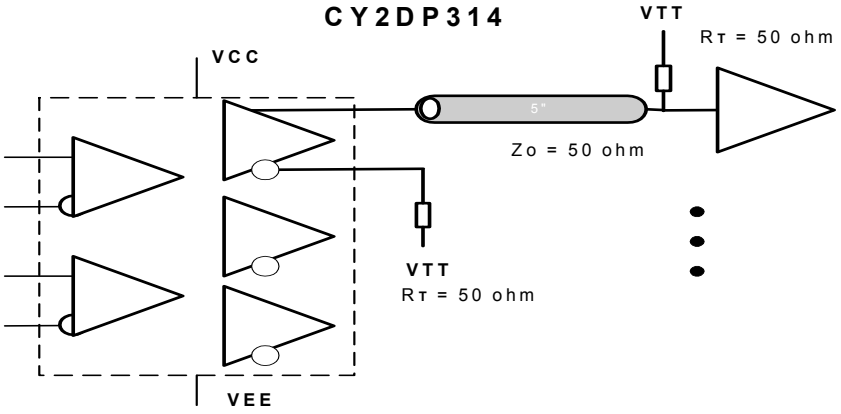


Figure 11. Driving a PECL/ECL Single-Ended Input

Evaluation Material

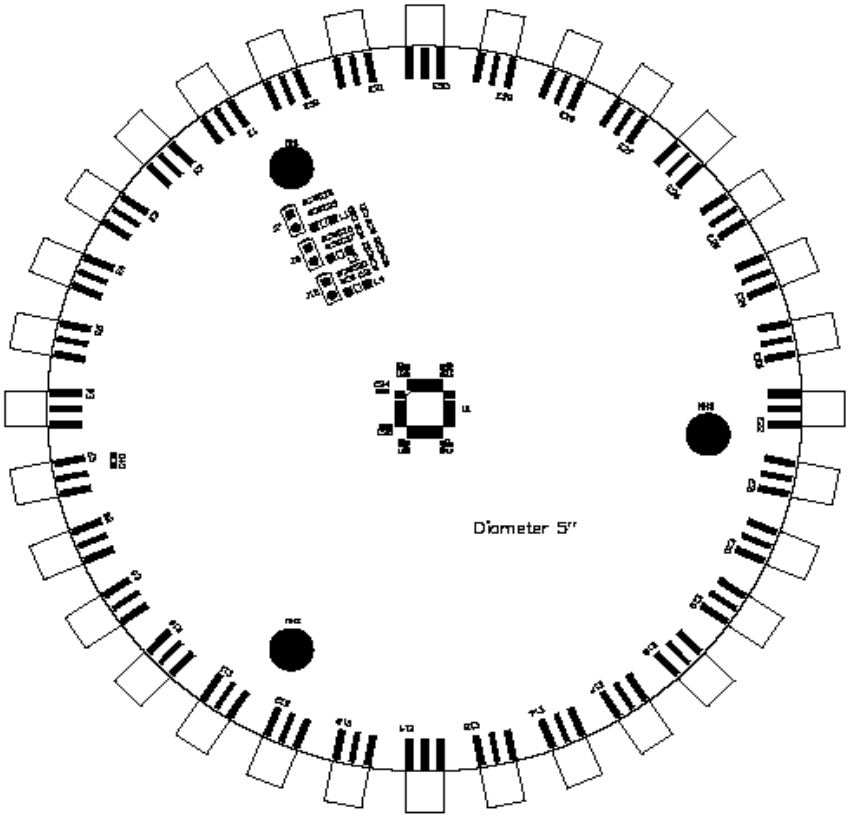
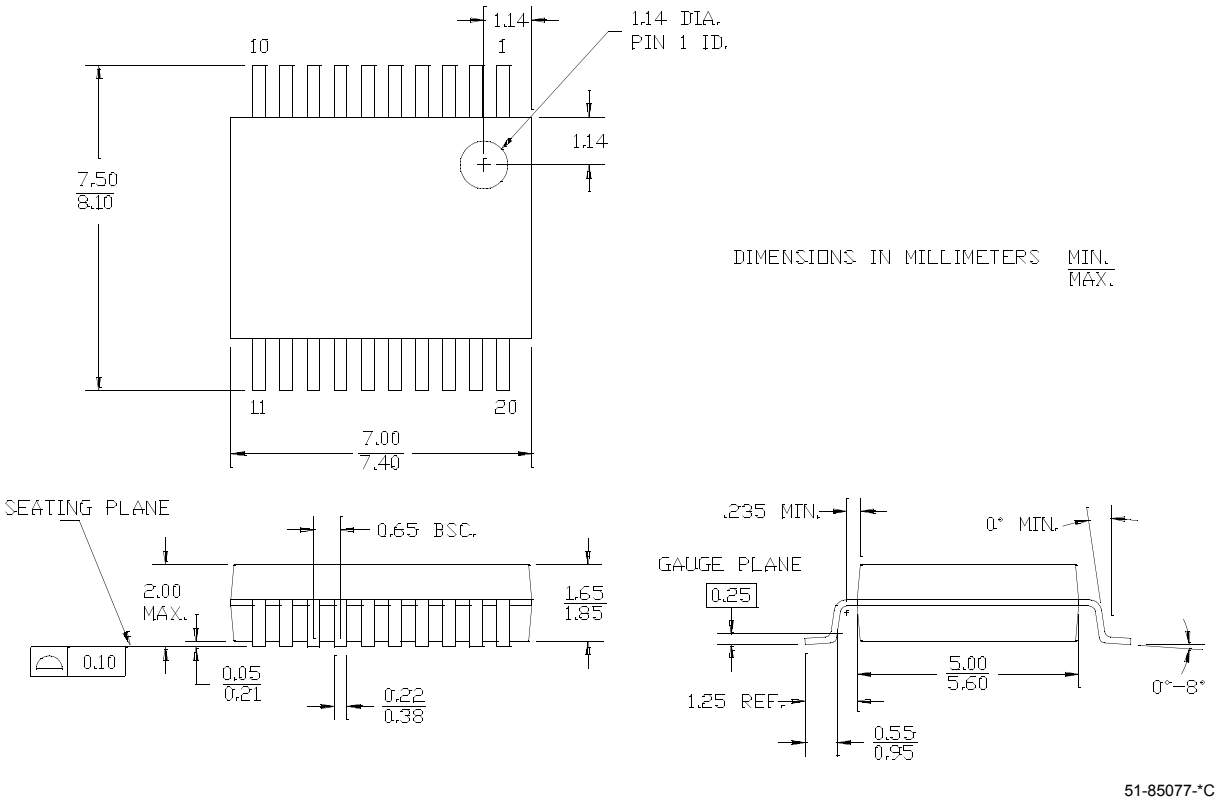


Figure 12. Demonstration PCB

Part Number	Package Type	Product Flow
CY2DP314OI	20 SSOP	Industrial, –40° to 85°C
CY2DP314OIT	20 SSOP-pin Tape and Reel	Industrial, –40° to 85°C

Package Drawing and Dimensions

20-Lead (5.3 mm) Shrunk Small Outline Package O20



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Document History Page

Document Title: CY2DP314 FastEdge™ SERIES 1 of 2:4 Differential Fanout Buffer Document #: 38-07550				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	126779	06/13/03	RGL	New Data Sheet
*A	128940	08/19/03	RGL	Changed the operation value from 1.5 GHz, reduced swing to 3 GHz to from DC to above 1.5 GHz Changed V_{CC} value in the I_{IN} parameter from 3.6V to 3.645V. Changed the V_{OL} min value from V_{CC}–1.9 to V_{CC}–1.945 Changed the I_{EE} max value from 48 mA to 130 mA Specified the max input frequency (F_{CLK}) to 2200 MHz Specified the TTB max value to 250 ps
*B	See ECN	207710	RGL	Added Junction Temperature(T_J) parameter in the Absolute Max. Conditions Table Replaced I_{CC} calculation with power calculation in the footnote