Building A Serial Digital Interface For A Multi-Format Video System

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Mandated by the FCC, television stations around the US have started to make the transition to digital television (DTV). Since not all households might have the capability of receiving DTV terrestrial broadcast signals professional video equipment manufacturers and broadcasters face two key challenges: being ready to support both digital and analog broadcasts, and being ready to support programming in both the DTV subgroups of HD (high-definition) and SD (standard definition). In other words, broadcasters must be prepared to support a multi-format video system. Beginning with the history of DTV, this article will look at challenges faced in building a serial digital interface (SDI) for a multi-format video system and possible solutions for such implementations.

The Revolution

The last big revolution in the television industry was the shift from monochrome to color television broadcasting. Today there is a new revolution, a shift from analog to digital broadcasting. In countries like Japan this transition is already underway. In the US, the Federal Communications Commission's (FCC) *Fifth Report and Order*, dated April 21, 1997 included an aggressive eight-year strategy for transition to DTV. This has triggered a revolution in which analog systems are being progressively replaced by digital. Broadcasters are supposed to follow a pre-approved course: set a standard, buy equipment and begin broadcasting. The FCC mandate clearly specifies dates for broadcasters to begin DTV transmission; if these deadlines are not met, broadcasters must be prepared to turn in their FCC licenses. This shift to digital from analog TV is driven by two main reasons: higher resolution and noise immunity.

Key Challenges

One important consideration throughout the evolution of DTV has been that there should be no disruption of service to the viewing public during the transition period.

Hence, in the early stages of the digital rollout, broadcasters will be required to broadcast program material on channels in both digital and analog formats. In addition, to ensure that they are ready for a full digital broadcast, professional studio equipment must support multi-format digital video -- HD as well as SD. For example, to combine locally-generated advertising, programming and logos that are now available in a variety of different HD and SD formats, with network-generated programming, the professional studio equipment must support multi-format digital video. Thus, there are two key challenges in the television broadcasting and professional video equipment world:

- Compatibility and interoperability: how to ensure that both digital and analog are broadcast simultaneously
- Multi-format: how to ensure that both HD and SD formats are supported

We will focus here on an important aspect of the second challenge. In order to fully understand the aspects of this challenge, different formats of DTV must be understood.

DTV Formats

There are different DTV formats summarized in Table 1, all of which fall into two main categories: HDTV and SDTV

Table 1. Most common Digital Video Parameters for different formats of 4:2:2 Component Digital Video

No of active lines per frame (M)	No of Active Luminance samples per line (N)	No of samples in the digital blanking interval of each line Bn (Excluding EAV and SAV)	Total number of lines per frame including vertical blanking	Interlaced (I) or Progressive (P)	Aspect Ratio	Sampling Rate of the Luminance channel (MHz)	Frame Rate (Hz)	SMPTE Bit - Parallel Interface Specification	SMPTE –Serial Digital Interface Specification	HDTV or SDTV
720	**1280**	**362**	**750**	**P**	**16:9**	**74.25 Or 74.25/1.001**	**60 or 60/1.001**	**SMPTE 296M**	**SMPTE 292M**	**HDTV**
720	**1280**	**692**	**750**	**P**	**16:9**	**74.25**	**50**	**SMPTE 296M**	**SMPTE 292M**	**HDTV**
1080	**1920**	**272**	**1125**	**I**	**16:9**	**74.25 or 74.25/1.001**	**30 or 30/1.001**	**SMPTE 274M**	**SMPTE 292M**	**HDTV**
1080	**1920**	**712**	**1125**	**I**	**16:9**	**74.25**	**25**	**SMPTE 274M**	**SMPTE 292M**	**HDTV**
480	**720**	**268**	**525**	**I**	**4:3**	**13.5**	**29.97**	**SMPTE 125M**	**SMPTE 259M**	**SDTV**
576	**720**	**280**	**625**	**I**	**4:3**	**13.5**	**25**	**ITU BT.656**	**SMPTE 259M ITU BT.656**	**SDTV**

With its higher resolution and superior picture quality, HDTV has been slowly generating a lot of interest, with lifelike pictures and digital sound. The higher resolution produces clarity never achievable with a CRT, and movies retain their original width -- enhancing the home theater experience. But HDTV comes with its own set of issues.

The most significant problem faced with HDTV is exactly the same problem faced with introducing color TV in the 1950s. There are approximately 600 million television sets in the world and approximately 70% of them are color TVs. An important and critical consideration was whether the new HDTV standard should be compatible with the existing color TV standards, supplant the existing standards, or be simultaneously broadcast with the existing standards (with the understanding that the existing standards would be faded out over time).

Multi-Format

Within the last year, HDTV has been one of the industry's most revolutionary technologies. Several things have come together to bring HDTV to this stage:

- Video cameras now come equipped with both 720P and 1080I interfaces, the most common HDTV formats. So operators of remote trucks, for example, don't have to invest in two different types of cameras. Additionally, investment in expensive conversion equipment to support all existing HD formats is kept to a minimum
- HDTV equipment cost has dropped enough in price to the extent that it will generate sufficient ROI sooner rather than later
- On the programming distribution side, the major US broadcasters and cable operators are all offering prime time programming in HD

With HDTV generating so much buzz, SDTV is by no means out of the picture. The SMPTE 259M standard that defines SD broadcasting has been around long enough for most of the broadcasters to have already begun programming and broadcasting in SD. Because a compressed SDTV digital signal is smaller than a compressed HDTV (SMPTE 292) signal, broadcasters can transmit up to five SDTV programs simultaneously instead of just a single HDTV program. This is often referred to as multicasting. Multicasting is an attractive feature because television stations can receive additional revenue from the additional advertising opportunities these extra programs provide. The FCC mandate leaves it open for the broadcasters to decide whether to broadcast SDTV or HDTV programs. Most broadcasters have opted to broadcast SDTV during daytime and HDTV during prime time.

Growing customer interest in HDTV, widespread SDTV programming, and the mandate to go digital has fuelled local broadcasters' migration from being single NTSC service providers to multi-format DTV service providers. Many local broadcasters are now realizing that the first few stations in a market to support multiple digital programming formats have a better chance of survival than the rest. In addition, once the investment to switch from analog to digital has been made, adding multi-format DTV programs can be done with a low incremental cost per channel. Broadcasters, both commercial and public television stations, have begun to realize the importance of offering multi-format DTV services. This increases market penetration, provides a cutting edge, and generates a better revenue stream (for the commercial stations). So any equipment (video production switchers, editing platforms or storage servers, for example) that stores, processes or distributes DTV must accept and deliver either SD or HD streams. The different DTV conversion formats (up, down, side) provide added benefits to a multi-format system.

However, implementing such a system comes with its own set of challenges. Lets look at one of the key challenges faced in designing a multi-format video system -- designing the serial digital interface.

SDIs For Multi-Format Video Systems

The move to DTV has forced professional video equipment manufacturers to build interfaces and transmission media that will allow studios and broadcast stations to carry DTV data, at professional video quality, at either HD or SD formats from one point to another. Most of the professional video systems prefer serial rather than parallel connections between the delivery and acceptance systems. Serial connections are usually necessary because parallel connections are not feasible for distances greater than 50 m for SDTV and 20 m for HDTV, due to the technical issues involved in delivering multiple bits of data at high speeds with respect to a common clock over a single bus. As a result the parallel data needs to be converted to a single serial stream before delivery and the serial data needs to be converted to a parallel bus after receipt.

A serializer/deserializer (PHY) is an important part of the SDI, present at any point where serial data is converted to 10-bit video data, or 10-bit video data is converted to serial digital data. Examples of professional video equipment that require SDI interfaces include professional video cameras, video editing equipment, video production servers, video switchers, video format converters, SD-to-HD up-converters, HD-to-SD down-converters, and HD-to-HD side converters.

The parallel component video for SDTV consists of 10-bit data transmitted at a clock rate of 27 MHz. This results in a serial data-rate of 270 Mbit/s for SD-SDI. The parallel component video for HDTV consists of two 10-bit data-streams, a 10-bit luminance channel (Y) and a 10-bit color-difference channel (Cb/Cr) transmitting at a clock rate of 74.25 MHz or 74.25 ÷ 1.001 MHz (74.17582 MHz), resulting in a serial data-rate of 1.485 Gbit/s or 1.485 ÷ 1.001 Gbit/s (1.483516 Gbit/s) for HD-SDI. In order to generate a single HD-SDI stream from two parallel data streams (Y and Cb/Cr), the Y samples and Cb/Cr samples are interleaved into a single 10-bit data-stream (see Fig. 1) and then serialized with a 10-to-1 serializer.

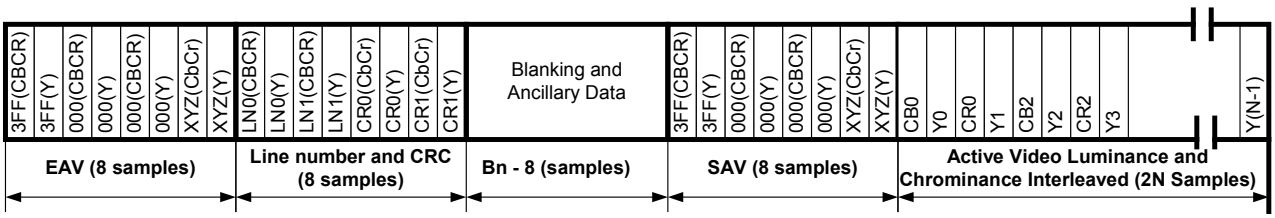

Fig. 1: Interleaving of luminance (Y) and color-difference channels (Cb/Cr) to form a single 10-bit data-stream that can be serialized to a single HD-SDI stream

The specifications for SD-SDI and HD-SDI are documented in SMPTE 259M and SMPTE 292M respectively.

The following section will look at the block diagrams of an SDI transmitter and receiver. It will also cover, in detail, the challenges, issues and solutions for designing each sub-section of an SDI transmitter and receiver to support multi-format HD and SD operation.

SDI Transmitter

The block diagram of an SDI transmit channel is shown in Fig. 2.

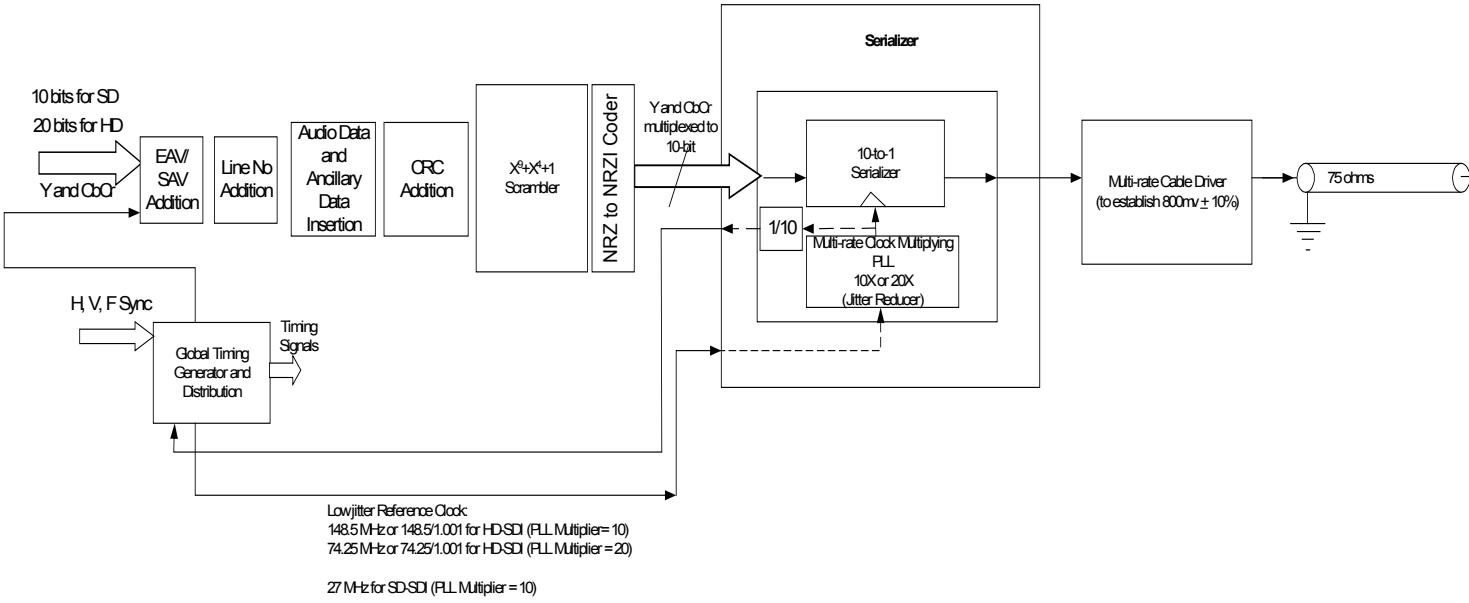

Fig. 2: Block Diagram of SDI Multi-Format Transmitter

SDI Transmitter Requirements For Multi-Format Video

Cable Driver and Output Driver Requirements:

The purpose of the cable driver is to drive the signal over coaxial cable with an 800 mV ±10% serial output swing. The amplitude needs to be tightly controlled to allow the equalizer in the far-end to perform adaptive equalization based on the received signal amplitude. These cable drivers need to be capable of operating at both HD-SDI data-rates (1.485 Gbit/s) and SD-SDI data rates (270 Mbit/s).

Although professional video equipment has multiple output channels, it is desirable to have multiple redundant outputs per channel in the serializer sub-section. This is very beneficial when the same SDI channel output must be broadcast to more than one location, a requirement very common in professional studio environments. This can be accomplished by having redundant output buffers for each SDI transmit channel (see Fig. 3). If this feature is not present, for redundancy, the same data should be serialized through another channel or a 1:2 buffer should be added.

The serializer IC's output is typically a differential pair. Since coaxial cable transmission uses only one end of the signal, the other end can be used to send the data to a different location. Since SDI data is NRZI encoded, it is free of polarity, thereby allowing negative outputs to be directly tied to positive inputs and vice versa.

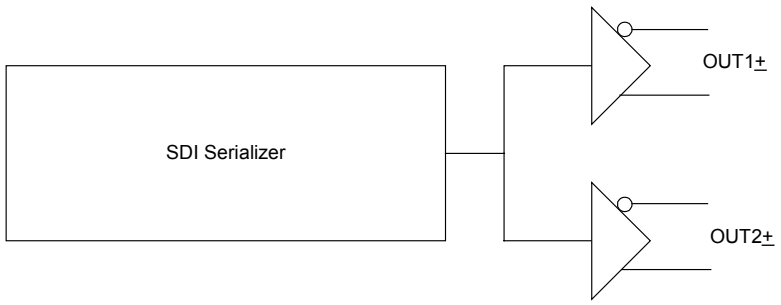

Fig. 3: Redundant Output Drivers For Each Channel

Serializer Requirements (10-bit or 20-bit):

The serializer is a parallel-to-serial converter. For SD-SDI it accepts 10-bit parallel data and serializes it using a multiply-by-10 serial clock internally generated within the clock multiplying PLL that is integrated into the IC. For HD-SDI, the parallel-input data is 20-bits wide (10-bit for luminance and 10-bit for color-difference). For HD-only applications it may be desirable to serialize the 20-bits directly to a single serial stream using multiply-by-20 clock. To make the same serializer compatible for both HD-SDI serialization as well as SD-SDI serialization, there are two approaches:

1. The HD-SDI luminance channel and color-difference channel data could be interleaved as shown in Fig. 1 to a single 10-bit data-stream at a 148.5 MHz clock speed and fed to a common 10:1 serializer. The same serializer will work with no issues for SD-SDI, since the parallel digital component data for this format is 10-bits wide
2. The SD-SDI data could be de-interleaved to produce separate luminance and color-difference channel data at a 13.5 MHz clock speed. Serializing the de-interleaved data is more complex than expected, because the EAV, SAV and digital blanking samples for each line of SDTV are common for both luminance and color-difference channels. Hence, they cannot be duplicated for each de-interleaved stream.

Transmit Clock Multiplying PLL requirements:

The purpose of the transmit clock multiplying PLL is to produce a low-jitter serial-bit clock that will be used for serialization. The PLL will produce either a multiply-by-10 clock or multiply-by-20 output of the reference clock input provided. The PLL also needs to have a multiply-by-20 option for HD-SDI along with the multiply-by-10 option to allow lower frequency timing references (74.25 MHz or 74.17582 MHz). This feature provides the benefit of using a half-rate clock (74.25 MHz for HD) as reference clock, thereby not worrying about designing traces and circuits for a higher speed full-rate clock of 148.5 MHz.

The PLL must be frequency-agile, able to operate over a wide range of frequencies. This will provide the benefit of operating at either the SD-SDI input frequency of 27 MHz or HD-SDI input frequency of 74.25 MHz (148.5 MHz with 10x multiplier) or 74.17582 MHz (148.3516 MHz with 10x multiplier). The integration of the PLL and its corresponding VCO and loop-filters into the serializer IC ensures that PLL performance is not affected by noise and there is no need to change the loop-filter component values when switching from HD-SDI to SD-SDI or vice versa.

The transmitter output jitter is dependent on the amount of jitter present in the reference clock input to the transmit clock multiplying PLL. The transmit clock multiplying PLL by itself attenuates high-frequency jitter and only passes low-frequency jitter. The output jitter at the cable driver must meet the requirements specified in SMPTE 259M and SMPTE 292M for SD-SDI and HD-SDI, respectively. There is a separate requirement for timing jitter and alignment jitter. Video test equipment vendors offer solutions to measure these jitter components (timing and alignment) individually. The conventional method of measuring jitter is through eye-diagrams. Figs. 4 and 5 show SD-SDI and HD-SDI output eye-diagrams of a multi-format serializer with in-built clock multiplying PLL, VCO and loop-filter. For multi-format SDI, the serial outputs should be compliant to both SMPTE 259M as well as SMPTE 292M jitter requirements. The latter is more a stringent spec to meet and requires a high performance transmit PLL and serializer to ensure compliance.

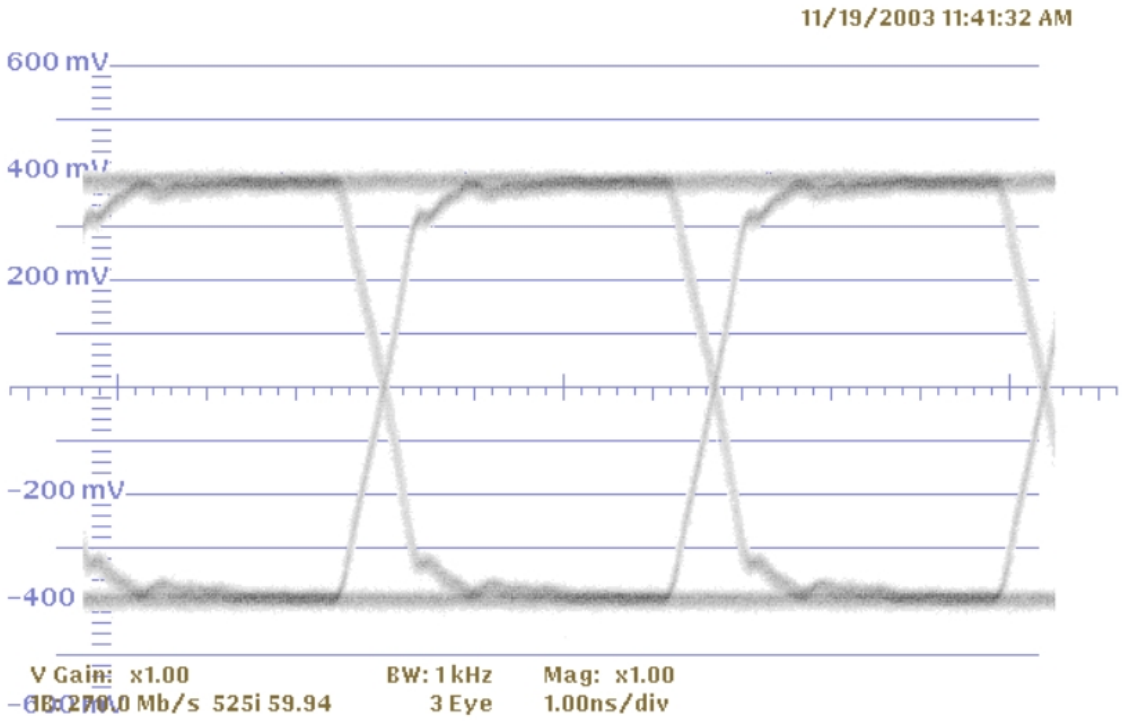

Fig. 4: SD-SDI output eye-diagram (obtained from Cypress Semiconductor's HOTLink II transceiver's serial output using a Tektronix WFM700M waveform monitor)

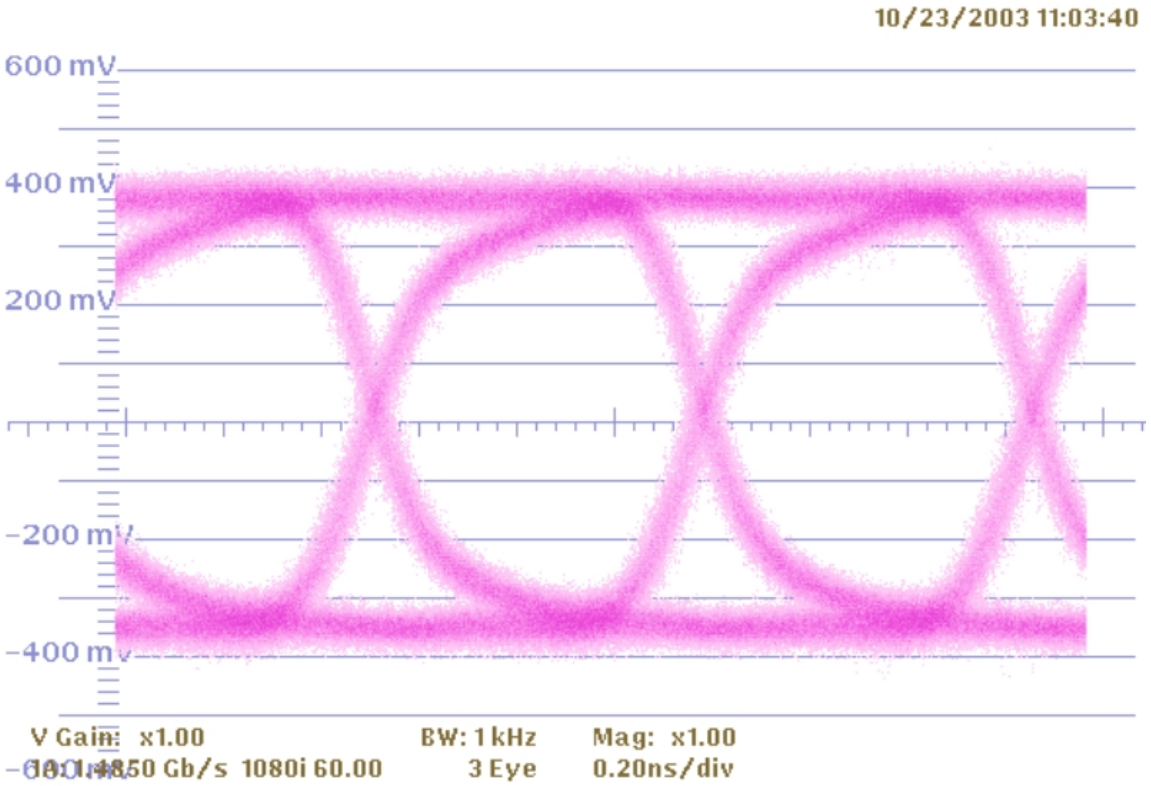

Fig. 5:. HD-SDI output eye-diagram (obtained from Cypress Semiconductor's HOTLink II transceiver serial output using a Tektronix WFM700M waveform monitor)

Scrambler Requirements:

Scrambling is used to increase the transition density of the serial bit-stream, and to attempt to limit the maximum run-lengths of continuous zeros or ones that can occur when sending certain characters. A high transition density is required for the remote receivers to be able to extract the clock from data and retime the received data.

Although SMPTE 259M and SMPTE 292M recommend that the scrambling be done in the serial bit stream, there are advantages in performing these operations in the 10-bit parallel domain. From a performance and speed standpoint, it is easier and more reliable to implement this logic in the parallel data domain that operates at $1/10^{th}$ the serial clock speed. To make the same scrambler compatible for HD-SDI and SD-SDI, it is preferred to convert the two 10-bit parallel channels (Y and Cb/Cr) at 74.25 MHz to a single 10-bit interleaved data-stream at 148.5 MHz (Fig. 1, again). For HD-only applications, the scrambling can be directly performed on 20-bit interfaces, thereby reducing the speed by half to 74.25 MHz.

Integrated Multiple Channels:

Most of the video equipment with SDI has more than one input node and one output node per box, thereby requiring multiple channels of serializers. An SDI device that has multiple channels (quad or dual) in the same IC will result in a considerable amount of savings in board space as well as cost.

Independent Clocking of Each Channel:

In a system with multi-channel serializers, it is desirable to clock each channel at a different rate, in order to simultaneously transmit SD-SDI and HD-SDI across multiple channels or to create a custom system configuration. In this case, the serializer should be capable of accepting separate reference clock inputs for each channel.

Benefits of Independent Clocking and Independent Configuration for Each Channel:

The independent clocking and configuration capability of a multi-channel serializer can be used by digital video system designers in two types of applications:

1. Multiple formats and serial data rates over different channels. Each channel can transmit and receive traffic from a different protocol. For example, Channel A can be configured to pass SMPTE 292M data at 1.485 Gbit/s (HD-SDI), while Channel B can be configured to pass HD-SDI at 1.483516 Gbit/s, and Channel C can be configured to pass SMPTE 259M data (SD-SDI) at 270 Mbit/s. An example of this application is in Fig. 6. This allows system designers to take advantage of the integration of multiple channels along with the ability to operate each channel independently at a different rate. Designers will benefit from a large savings in board space and reduction in the number of components
2. Multiple channels pass traffic from the same protocol but different sources: Each channel can transmit traffic in the same format and data rate but each individual channel can be referenced by a different clock (different timing domains) that need not be synchronous to the others. So, the reference clocks for each channel can have a frequency offset with respect to one another. An example of this application is in Fig. 7. This could be applied to a situation where data from four different professional digital cameras need to be transported to the same video server.

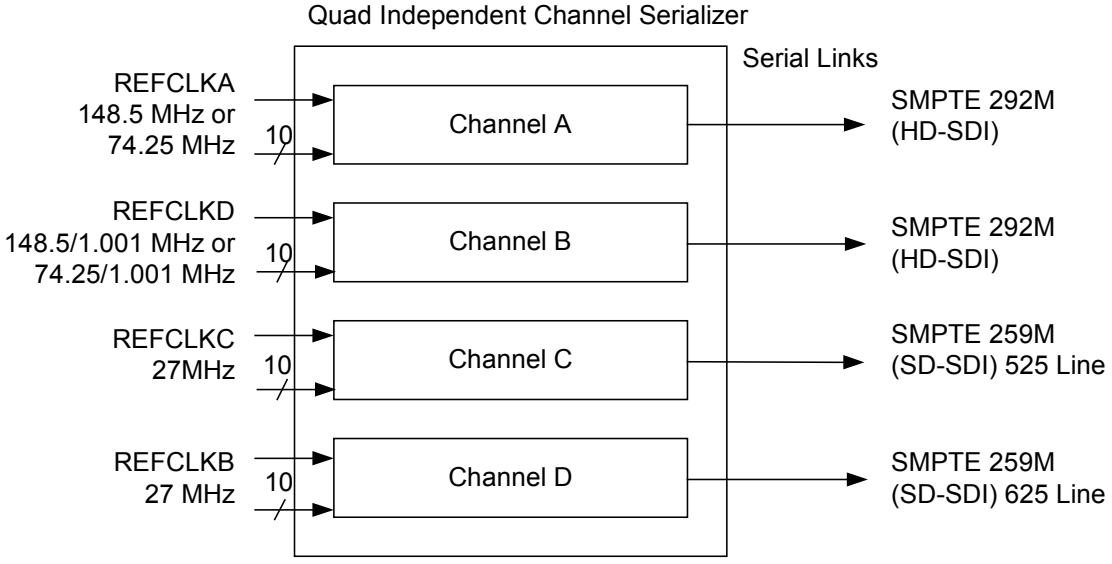

Fig. 6: Multiple formats and rates over different channels

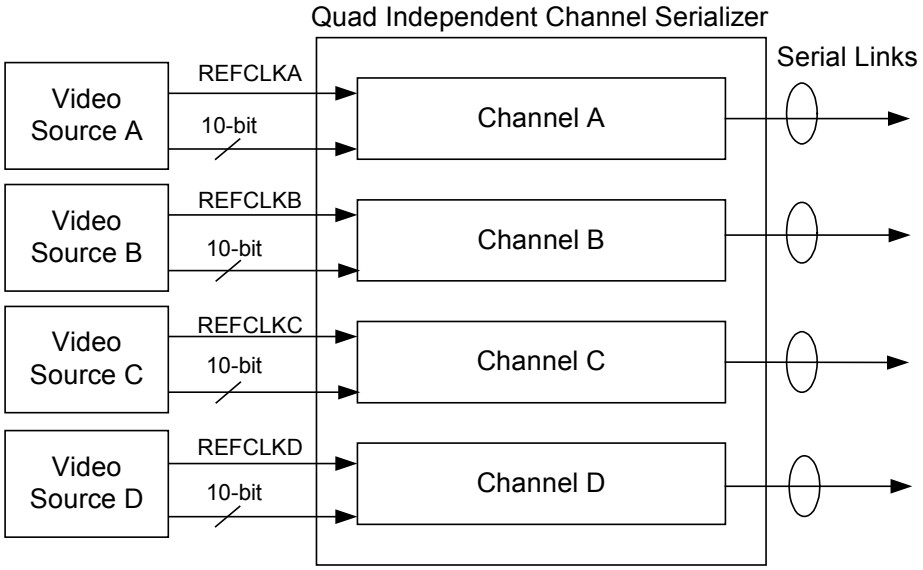

Fig. 7: Multiple channels pass traffic with the same protocol but different sources

SDI Receiver

The block diagram of an SDI receiver is shown in Fig. 8.

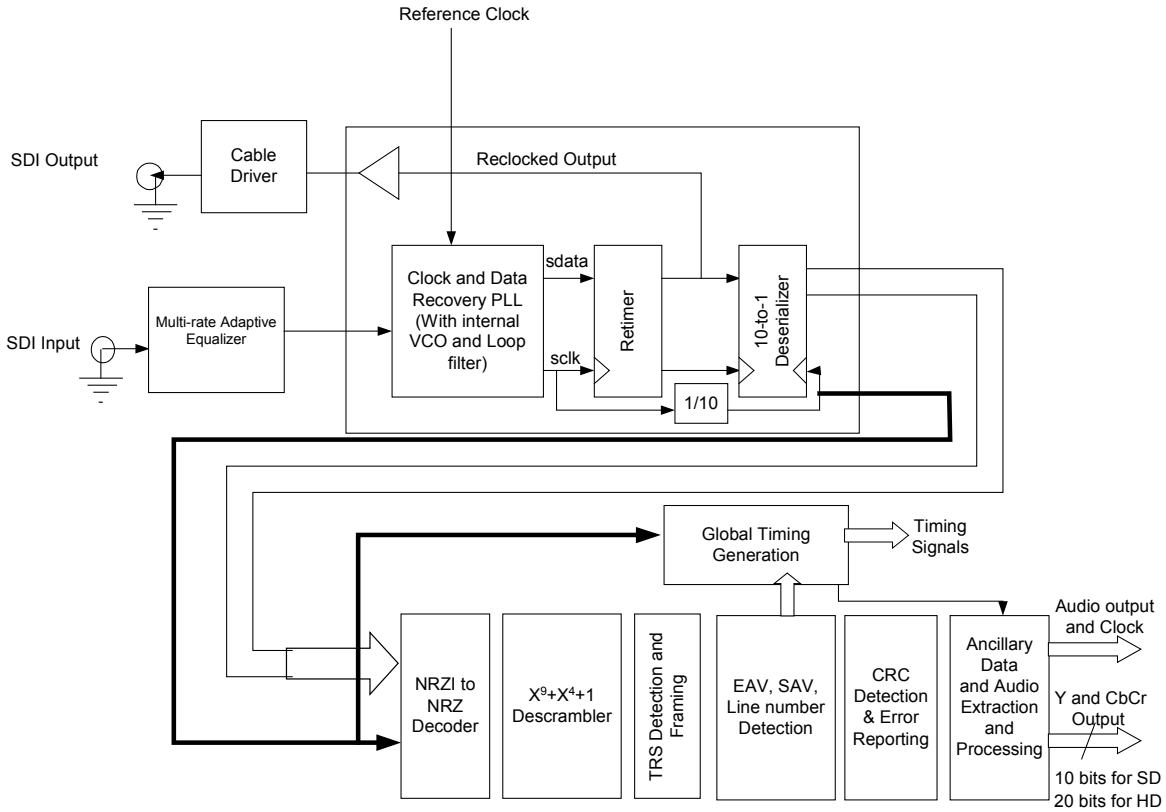

Fig. 8: Block diagram of an SDI receiver

SDI Receiver Requirements For Multi-Format Video Systems

Equalizer Requirements:

The maximum-allowable cable length is different for SD-SDI and HD-SDI. For SD-SDI the length of each link from transmitter to the receiver can typically be up to 300 m (Belden 8281, for example). For HD-SDI, it can typically be up to 100 m (same cable). For such long cable lengths, the Inter-Symbol Interference (ISI) created by the frequency-dependent attenuation of the cable causes the receive input at the remote receiver to be severely attenuated with large amounts of data-dependent jitter. The purpose of the equalizer is to apply a filter that has the inverse frequency response of the transmission channel followed by a gain-stage, thereby restoring the attenuated signal to its original amplitude and also removing the data-dependent jitter.

An equalizer in multi-format video systems should be capable of equalizing both HD-SDI as well as SD-SDI signals. For any given cable length the amount of equalization needed for HD-SDI is greater than SD-SDI, due to the difference in the data rate. This forces a requirement upon the equalizer to be capable of automatically-adjusting its gain based on the length of the cable and the incoming serial data rate.

The equalizer should also have a carrier-detect output (CD) that reports the presence of a valid signal level in the SDI input. It should have a standards selection control input that allows the equalizer to be configured for either HD-SDI or SD-SDI. This input can be controlled by logic that automatically detects if the incoming stream is HD or SD.

Clock and Data Recovery PLL Requirements:

In SDI the data is transported as a single serial data stream that has no accompanying clock. The clock is embedded within the serial data stream and extracted using a clock and data recovery (CDR) PLL. In order to allow the CDR PLL to recover the clock, the incoming data needs to have a high transition density. The scrambler in the remote transmitter ensures that the data has sufficient transitions.

The CDR PLL must be frequency-agile over a wide range, giving the benefit of being able to recover clock and data from either an HD-SDI stream (1.485 Gbit/s) or an SD-SDI stream (270 Mbit/s). Similar to the SDI transmit clock multiplying PLL, the integration of the CDR PLL and its corresponding VCO and loop-filters into the deserializer IC ensures that PLL performance is not affected by noise. There is also no need to change the loop-filter component values when switching from HD-SDI to SD-SDI or vice versa.

The CDR PLL typically uses a local reference clock at a frequency of approximately $1/10^{th}$ the serial data rate to center the CDR PLL on the correct frequency and reduce the lock time. For correct centering, the local reference clock must be within a certain frequency offset from $1/10^{th}$ the incoming serial data-rate. For HD-SDI, the incoming serial data can be at either 1.485 Gbit/s or 1.483516 Gbit/s. Hence, the $1/10^{th}$ clock frequency can be either 148.5 MHz or 148.3516 MHz. If the maximum allowed frequency offset between the incoming serial data-rate and local reference clock is much greater than 1000ppm, HD-SDI data can be recovered for either data rates using just one reference clock source (148.5 MHz or 148.3516/1.001 MHz). For HD-only applications, it will be desirable to have the option to use a $1/20^{th}$ of the serial rate reference clock to center the PLL.

Automatic Rate Detection and Clock Frequency Adjustment:

For multi-format cards, it is desirable for the receiver to detect the incoming serial data format and adjust the operating frequency of the CDR unit to the correct frequency. Performing this operation using analog circuitry will increase the lock time of the PLL. It is easier and straightforward to poll the incoming SDI signal for either data rate (HD-SDI or SD-SDI). This can be done by selecting a default start-up reference clock (HD or SD, whichever is more common for your application) and looking at the link fault indicator (LFI) output of the PLL to report a PLL Lock. If the PLL does not lock within the specified lock time, the reference clock can be switched to the other valid frequency to achieve a lock. The reference clock can be switched from one frequency to another (HD to SD or vice versa) using two approaches:

1. Use a 2:1 clock multiplexer that selects the reference clock to be used by the CDR from one of the two clock frequencies (148.5 MHz or 74.25 MHz for HD-SDI and 27 MHz for SD-SDI). The select-input of the multiplexer is controlled by flipping it to the opposite polarity whenever the output of the simple logic state machine indicates that PLL has been out of lock for a duration that is longer than the specified maximum lock time
2. Use a programmable clock buffer, that can program its output to be either 148.5 MHz (or 74.25 MHz) or 27 MHz based off a standard reference clock input. The clock buffer should be capable of being dynamically-reprogrammed whenever the state machine demands a change in the reference clock frequency

Any switch in reference clock frequencies must also be accompanied by reconfiguring the rate-select input of the equalizer to the appropriate standard (HD or SD).

Reclocked Output:

Once the clock is recovered from the data stream, the data is retimed by sending it to a flip-flop. The retimed data is then sent to the deserializer. In SDI applications it is desirable to have a buffered version of the retimer output signal available to the external world. This reclocked output can be retransmitted to another remote location, while the deserialized output is sent for higher-layer processing. The reclockers can also be used to extend the total link length within a studio by having intermittent reclockers. The number of reclockers that can be cascaded in a row is limited by the jitter gain of the CDR PLL in each stage and the amount of input jitter that can be tolerated by the CDR PLL of the receiver in the final stage.

Multiple Channel Independent Clocking Receiver:

Similar to the benefits listed in the SDI transmitter section, integration of multiple channels of receivers within the same IC will result in considerable savings in space, cost and component count. To receive multi-format SDI data, any two channels in the same device must be able to operate simultaneously at different format rates (1.485 Gbit/s, 1.483516 Gbit/s or 270 Mbit/s). The channels should also be able to automatically detect the format and reconfigure the system to recover the data.

If the automatic detection and reconfiguration control listed earlier are available, each receive channel can act as a plug-and-play re-clocker for either format (HD-SDI or SD-SDI).

Pathological Compliance:

Under normal conditions a scrambled output has high transition density with a good ratio of ones to zeros. The pathological conditions are specific long run-length patterns with very low transition density -- patterns that may be generated by the SMPTE scrambler for specific combinations of scrambler state and scrambler inputs. Although the probability of the specific inputs and specific scrambler state occurring at the same time in real video data is very low, component vendors are expected to be compliant to the specified pathological conditions. The pathological serial digital signals are often very challenging for SDI receivers to handle. SMPTE EG34-1999 documents the pathological patterns that may occur in a SMPTE scrambled system that also must be recovered by SDI receivers with no errors. System designers need to select components that are tested to work under these pathological conditions. The various pathological conditions that may occur are the following:

1. Run-length of 44 bits with no transitions
2. Repetition of 20 ones followed by 20 zeros for the duration of an entire active video line. This test stresses the CDR PLL and ensures that it will remain locked and recover error free data for this pattern
3. Repetition of 19 ones followed by 1 zero or 19 zeros followed by 1 one for the duration of an entire active video line. This test stresses the equalizer and ensures that it will equalize patterns that have significant low frequency content and baseline wander

Descrambler Requirements:

Following reception and deserialization, the 10-bit data is routed through an NRZI-to-NRZ converter and then descrambled. The descrambler removes the additional transitions added by the transmit data path and returns the data to its original bit-stream form. If a 1:10 bit deserializer is used, the same 10-bit descrambler can be used for both HD-SDI and SD-SDI descrambling as long as it is able to run at a 148.5 MHz clock speed. For HD-only applications that use a 1:20 bit deserializer, the descrambler also needs to accept and process 20-bit data at 74.25 MHz.

TRS Framer Requirements:

The descrambled data (at this point) has no available reference to identify the start or end of each 10-bit character. The operation of finding the character boundary in the data stream is known as framing. Framing is the function of determining where (in a serial data stream) characters begin and end. Framing of an SDI video stream uses specialized hardware to detect a bit pattern known as the timing reference signal (TRS) that is embedded between the EAV and SAV of the video line. Once the TRS is detected, the framer hardware adjusts output boundaries to align the 10-bit output character to the correct boundaries.

For SD-SDI, the TRS consists of a three characters sequence of 0x3FF, 0x000, and 0x000 (10 bit hex) respectively. For HD-SDI, the TRS consists of a six characters sequence of 0x3FF, 0x3FF, 0x000, 0x000, 0x000 and 0x000 (10 bit hex) respectively. Note that this TRS sequence still has the SD-SDI TRS (0x3FF, 0x000, 0x000) sequence embedded within the six characters in the same order, as it would occur in HD-SDI. Therefore, as long as the framer corrects the character boundaries based on detection of the pattern 0x3FF-0x000-0x000 it will work for both SD-SDI as well as HD-SDI.

Summary

In the United States, the FCC is pushing for the rollout of DTV broadcast signals. During this rollout professional studios must handle, transport and broadcast video in multiple digital formats. This forces professional video equipment manufacturers to design multi-format SDI interfaces that can support HD or SD DTV signals. There are challenges in designing a multi-format SDI. By building a multi-format SDI using frequency-agile, multi-channel, independent-clocking serializers and deserializers with integrated PLLs many of these challenges can be overcome. This also results in considerable savings in board space and cost.

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Background Information

Conventional NTSC analog television in the US offers 480 lines of vertical resolution: 480 scanned lines stacked on top of one another. Each of these lines is 720 pixels wide . So, conventional TV is also described as 480 by 720. Because these signals are interlaced (alternate lines are scanned twice to complete the frame vs. progressive-scan in which a full frame scanned from top to bottom once), analog TV signals are often referred to as 480I. While 480I is the best quality available in NTSC, it is the lowest quality signal in DTV. The highest resolution signal in DTV is the 1920 x 1080 that HDTV offers. With higher noise immunity due to bigger noise margins that results in a much sharper image, DTV is all set to take over analog. Local decrees, growing consumer interest and aggressive deadlines merely add fuel to the fire.

Separate, new, channels were assigned to most broadcasters for DTV signals. Once the DTV transition is complete, broadcasters will be required to surrender the channels used for analog transmission. In an effort to make sure the viewing habits of NTSC viewers are not disrupted during the transition, the

plan is to have a phased-in simulcast (transmission of both analog and digital signals) before NTSC is eliminated. By December 31, 2003 all commercial television stations in the US that had both their NTSC and DTV operations on in-core channels were required to elect which of their two core channels to use for DTV operations after the transition. Non-commercial stations that have both their NTSC and DTV operations on in-core channels have until the end of 2004 to elect their post-transition DTV channel. In addition, to provide broadcasters with an incentive to provide full replication of NTSC coverage with DTV service, it was determined that, after December 31, 2004, whatever portion of a commercial broadcaster's NTSC Grade B contour is not replicated with its digital television signal will cease to be protected in the DTV Table of Allotments. Non-commercial DTV licensees were given until December 31, 2005 in which to replicate or lose such DTV interference protection.

As of May 2003, more than 1,000 stations were on the air with DTV signals, and every major TV market was served by at least one DTV station. The target date for the completion of the transition to DTV is December 31, 2006. However, that date may be extended until most homes (85%) in an area are able to view DTV programming. At that point, broadcasting on the analog channels will end and that spectrum will be put to other uses. Until the transition to DTV is completed, television stations are required to broadcast simultaneously both digital and analog signals.

HDTV is a wide-screen (16:9 aspect ratio), near-film-quality format featuring Dolby Digital audio (though not necessarily 5.1-channel). The two most common HDTV formats are 1080-line interlaced scan (1080I) and 720-line progressive scan (720P). 1080I has 1080 lines of vertical resolution and 1920 pixels across each line. 720P has 720 vertical lines with 1280 pixels across each line.

SDTV offers significantly less resolution than HDTV. All SDTV formats are either 480P or 480I. Still, even the lowest resolution SDTV signals produce better picture quality than current analog broadcasts. That's because digital broadcasts don't suffer from analog distortion such as "snow" or "ghosting." With digital broadcasts, viewers see either a clear picture, or if the digital signal is too weak, no picture at all.

Digital Representation

In professional studios, the most common format in which the digital data is stored, processed and transported within the studio is uncompressed digital component form (YCbCr or GBR). The data is MPEG-encoded and/or modulated only when necessary for broadcast or distribution.

Even prior to DTV transmission, studios preferred to transport and store video data in uncompressed component digital video format due to the following reasons:

- Easier effects processing and editing
- Lower distortion
- Noise immunity
- Prevention of NTSC/PAL encoding artifacts
- Easier transformation/cross conversion from one format/frame-rate to another
- Longer equipment life and equipment reliability
- All operations can be software/computer controlled
- No lossy compression artifacts

Professional Digital Video Quality

Professional studios demand the highest quality of video and are willing to pay for the higher cost incurred for transport, storage and processing of uncompressed and high-resolution video. The quality of digital video is dependent on the sampling rate, the number of bits per sample and careful maintenance of the timebase (video timing).

Component Digital Video: YCbCr

Component Digital Video consists of digitized luminance (Y), B-Y color-difference Cb, and R-Y color-difference Cr. The digital component standards originated as formats that would allow legacy monochrome receivers to receive a color signal and still work fine. The luminance signal represents the black and white (monochrome) portion of the signal. The chrominance signals (color-differences) represent the blue minus luminance (Cb) and red minus luminance(Cr). Using the values of Y, Cb and Cr, the values of components Red (R), Blue (B) and Green (G) can easily be calculated. Note that the conversion is slightly different for HDTV.

4:2:2 YCbCr Component Digital Video

Component Digital Video is obtained by sampling the analog video components Y, Cb and Cr. Samples are obtained by using ADCs. For every two samples of Y only one sample each of Cb and Cr are stored (Fig. a). While reconstructing the picture for display, the missing Cb and Cr samples are obtained by interpolating from the surrounding samples. Since the human eye is more sensitive to details and changes in brightness levels than color, the luminance signal should have higher resolution.

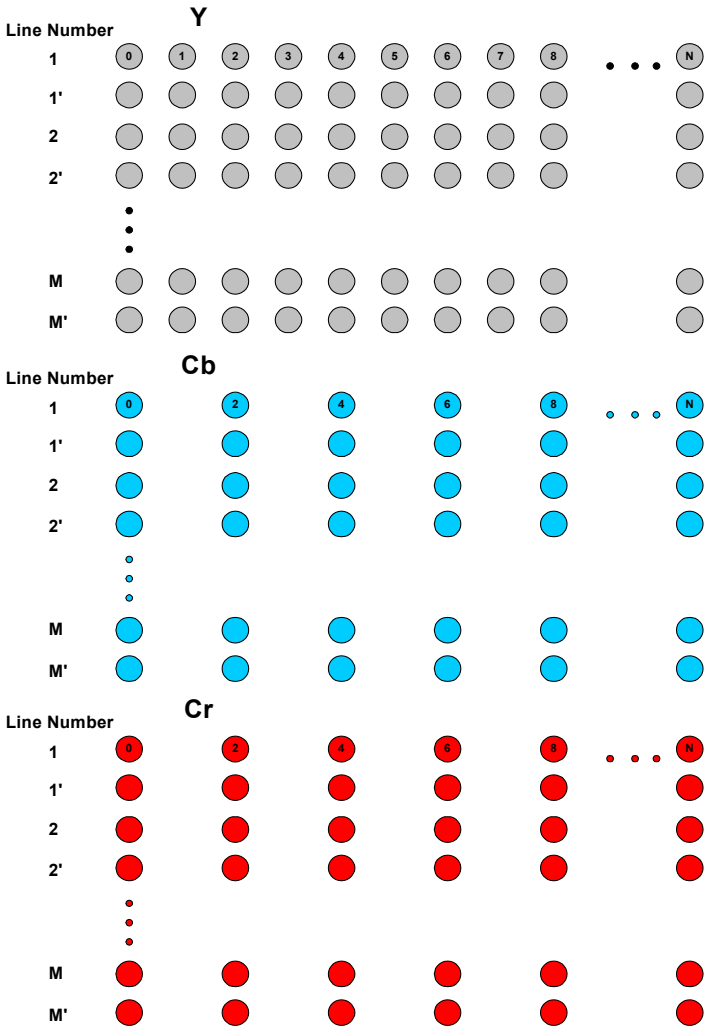

Fig. a 4:2:2 Sampling for Component Digital Video

The sampling rate of Y for 4:3 aspect ratio SDTV is 13.5 million samples per second. Hence, the sampling rate for Cb and Cr signals is 6.75 million samples per second each. This sampling rate was chosen for two reasons: it was close to 4 times the color subcarrier frequency and it also gave the same number of samples per active video line, 720 samples/per line, for both NTSC and PAL.

The sampling rate of Y for 16:9 aspect ratio HDTV is 74.25 million samples per second for 30 Hz and 25 Hz frame rates and 74.176 million samples per second for 29.97 Hz frame rates. Hence, the sampling rate for Cb and Cr signals are 37.125 million samples per second or 37.088 million samples per second each.

10-Bit and 8-Bit Video

The number of bits per sample affects the SNR of the reconstructed video signal. Each additional bit gives around 6 dB of increase in the SNR. Some older professional video interfaces and non-professional component digital interfaces for SDTV have 8-bit digital video component interfaces. The quantizing distortion is noticeable as contouring in places where the video signal level changes

gradually. Adding two additional bits to each sample makes the quantization distortion small enough to the extent that it is not visible to the human eye. Due to this, current SDTV and HDTV component digital interfaces use 10 bits per sample. However, current SDTV equipment is required to be backwards compatible to 8-bit video.

Parallel Digital Representation of 4:2:2 Data for SDTV

Parallel transport interfaces for component digital video were defined for both SDTV and HDTV. The bit-parallel interface for component digital video for SDTV is documented in SMPTE 125M-1995. Although, the standard calls for maximum transmission length of 300 m, it is not practically feasible to carry 10-bits of data plus a source synchronous clock over 300 m of parallel cable. It is impossible to carry the same piece of data for 300 m without equalization. Hence, this standard is only actually used for relatively small installations (50 m). The recommended connector is a 20-pin D-Sub connector. However, it is important to gain an understanding of this interface and data format requirements to understand the corresponding SDI for 4:2:2 YCbCr component digital video documented in SMPTE 259M.

The 10-bit video data is transmitted as 10 data signals (DATA0 through DATA9) synchronous to a 27 MHz clock signal. The Y, Cb and Cr samples of the active video portion sampled (Fig. b) are arranged in the10-bit data-stream as shown in the timing diagram of Fig. c. The Y samples occur every alternate clock cycle satisfying a sampling rate of 13.5 million samples per second. The Cb and Cr samples occur every fourth sample respectively satisfying a sampling rate of 6.75 million samples per second each.

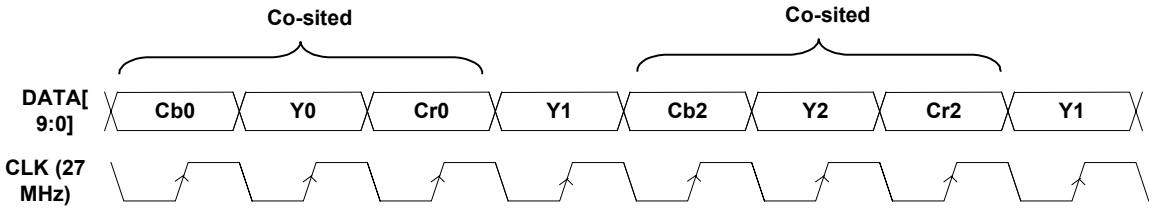

Fig. b: Arrangement of luminance and color-difference samples in 10-bit component video

Digitizing the blanking interval between two active video lines would be waste of bandwidth since the blanking interval carries only timing information. The majority of the data during the blanking interval is used for ancillary data transport such as embedded audio, teletext, closed captioning and CRC checksums. The timing information of the video signal is captured in TRSs that indicate the start of active video line (SAV) and end of active video line (EAV). The arrangement of blanking period, EAV, SAV and active video for each digital video line in the 10-bit data stream is shown in Fig. c.

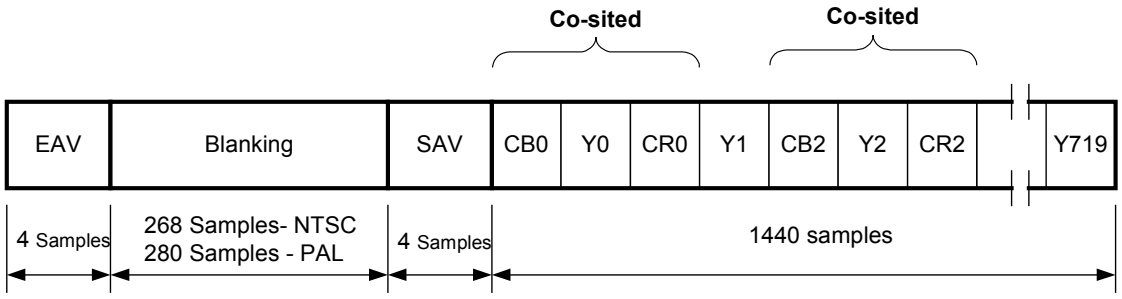

Fig. c: Data structure for each digital video line for 4:2:2 component digital video

The EAV and SAV Timing Reference Sequences consist of 4 words that have 10-bit hex values of 0x3FF, 0x000, 0x000 and XYZ. XYZ is a status word that has the following bits:

- F = "0" for Field 1; "1" for Field 2
- V= "1" for lines during vertical blanking interval
- H= "0" at SAV; "1" at EAV
- P3, P2, P1, P0 = Parity bits for error correction and detection of values present in F, V and H bits
- Parallel Digital Representation of 4:2:2 Data for HDTV

The bit-parallel digital interface for component digital video for HDTV is documented in SMPTE 274M (Active resolution = 1920 x 1080) and SMPTE 296M (Active resolution = 720 x 1280). The parallel connection between systems is accomplished using a 93-pin multi-pin connector cable. The nominal distance of transmission using this connector is approximately 20 m. These formats of parallel Component Digital Video can be serialized to produce a HD-SDI stream as specified in SMPTE 292M.

Unlike SDTV, the bit parallel component digital interface for HDTV consists of a 20-bit data-stream (two 10-bit sub-data-streams, one for luminance and one for the color differences) and a clock. The clock frequency is equal to the Y-sampling frequency, which is either 74.25 MHz or 74.176 MHz. The timing diagram in Fig. d shows arrangement of the active samples of Y, Cb and Cr shown in Fig. 1 with respect to the sampling clock. The first data stream is the 10-bit representation of the luminance samples (Y). The second data-stream is the 10-bit representation of the both color-differences (Cb followed by Cr) multiplexed in the same stream.

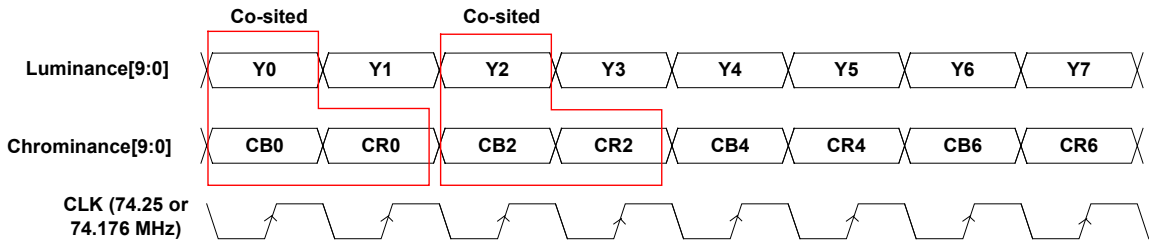

Fig. d: Arrangement of luminance/color-difference samples in 20-bit component video for HDTV

Both data streams (luminance and chrominance samples) have individual digital blanking intervals that consist of TRS sequences (EAV, SAV) and ancillary data. The arrangement of blanking period, EAV, SAV and active video for each digital video line for the luminance data-stream and chrominance data-stream is shown in Fig. e.

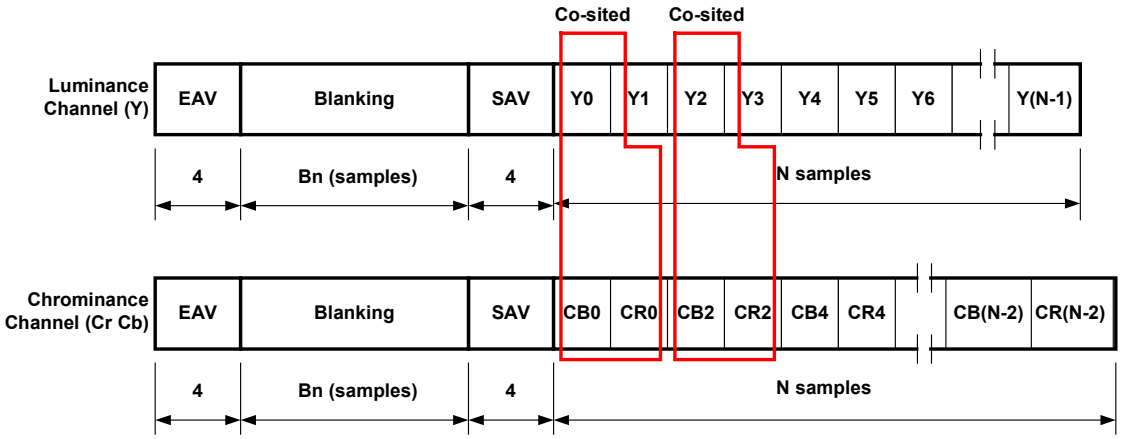

Fig. e: Data structure for each luminance and chrominance channel video line for 4:2:2 component digital video for HDTV

HDTV has multiple formats with different frame-rates and resolutions. The values of N and Bn shown in Fig. c are listed for the different HDTV formats in Table 1. The most commonly used HDTV formats are 1920 x 1080 (interlaced) and 1280 x 720 (progressive). The table also lists the parameters for other common 4:2:2 component digital video formats.

The scrambler generator polynomial is listed in"

$G1(X)= X^9+X^4+1$

Logic block diagrams of a serial implementation of a scrambler/NRZI encoder, and NRZI decoder/descrambler are shown in Fig. f. Each rectangle containing a D represents a D-type flip-flop. These flip-flops are connected to form a specialized shift register that implements the scrambler polynomial. The scrambled data is NRZI encoded to increase the transition density in the serial data stream. Moreover, it also allows the data stream to be phase independent; i.e., an inverted data stream will decode to the same signal as a non-inverted stream. The NRZI encoder polynomial is:

$G2(X)=X+1$

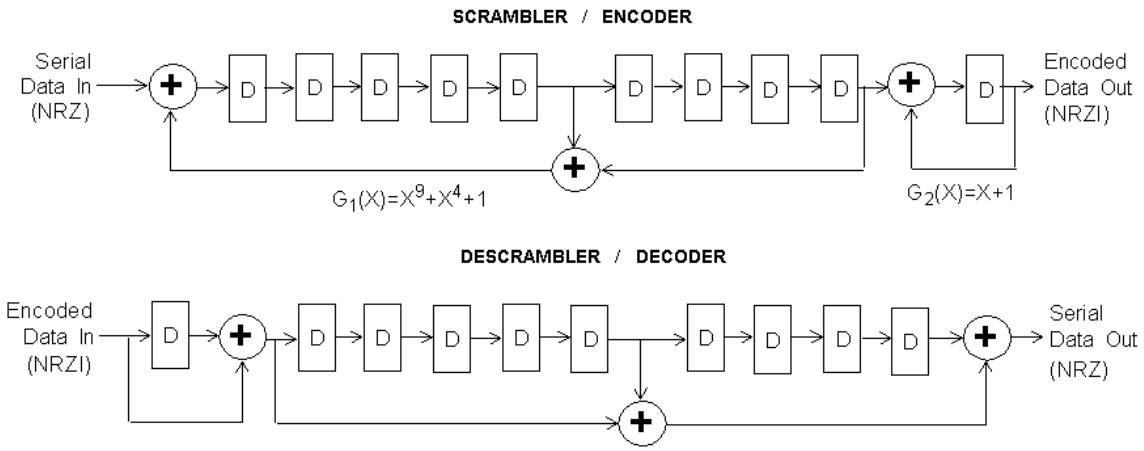

Fig. f: Structure of scrambler, NRZI encoder, descrambler and NRZI decoder for SDI

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