



CYPRESS

PRELIMINARY

Interfacing the HOTLink II™ Transceiver with the 3.3V National CLC001 Cable Driver for Digital Video

Introduction

The HOTLink II™ Transceiver is a point-to-point or point-to-multipoint communications building block allowing the transfer of data over high-speed serial links at signaling speeds ranging from 195 to 1500 MBaud. The device provides a selectable 8B/10B Encoder/Decoder and a Cypress Mode Multibyte Framer that may be used for DVB-ASI applications. The encoding, decoding and framing functions may be bypassed for use in SMPTE SDI applications.

Cable drivers are used in serial digital video systems to meet the 800mV signal amplitude requirements found in both the SMPTE 259M, 292M and DVB-ASI specifications. This application note explains how to interface the HOTLink II Transceiver to the National CLC001 Cable Driver for serial digital video communications over hundreds of meters of coaxial cable. All of the members of the HOTLink II video family, which includes the CYV15G0101DXB, CYV15G0201DXB, CYV15G0401DXB, CYV15G0402DXB and CYV15G0403DXB, are compatible with this National device.

Block Diagrams

Figure 1 and Figure 2 show the block diagram of the connection of CYV15G0101DXB (HOTLink II PHY), the CLC001 (National Cable Driver) and the CLC014 (National Adaptive Equalizer). Although a single-channel device is shown in these figures, the same format is applicable to any device in the HOTLink II family, including dual-channel and quad-channel devices.

Figure 1 shows the block diagram for a SMPTE system in which the HOTLink II device's 8B/10B Encoder, 10B/8B Decoder and Framer are disabled, and the SMPTE scrambling and framing functions are provided by an external Cypress solution.

Figure 2 shows the block diagram for a DVB-ASI system in which the 8B/10B Encoder, 10B/8B Decoder and Cypress Mode Multibyte Framer are enabled. The non-SMPTE "CYP" devices may also be used in DVB-ASI systems.

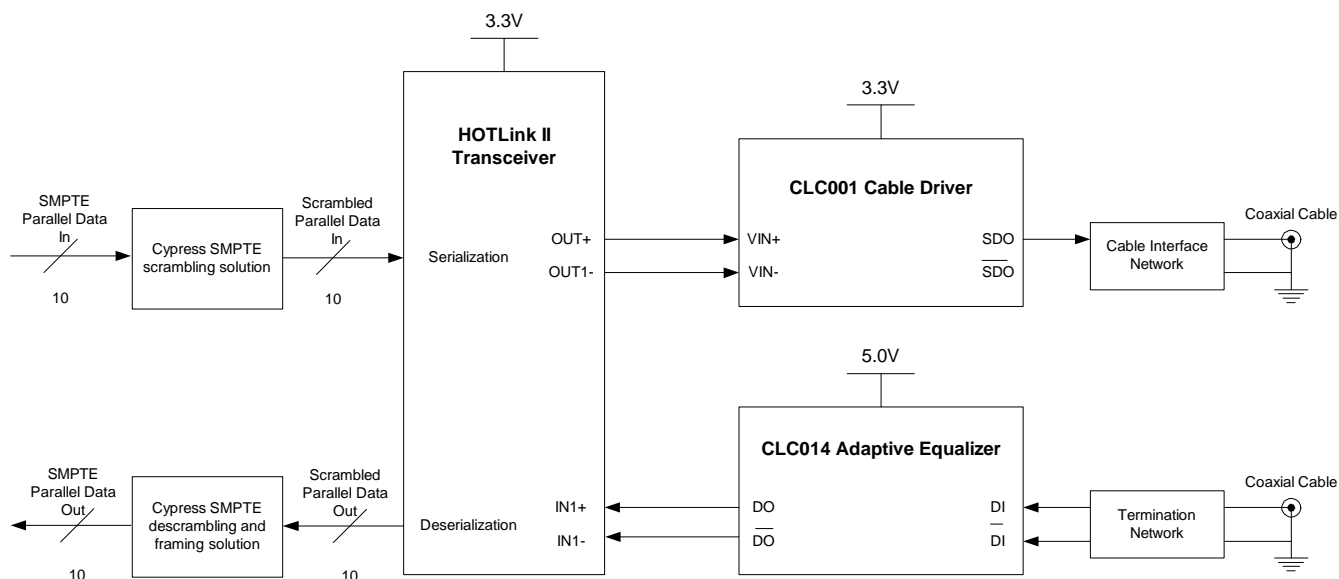


Figure 1. Typical Block Diagram of the Physical Layer in a SMPTE SDI Video System



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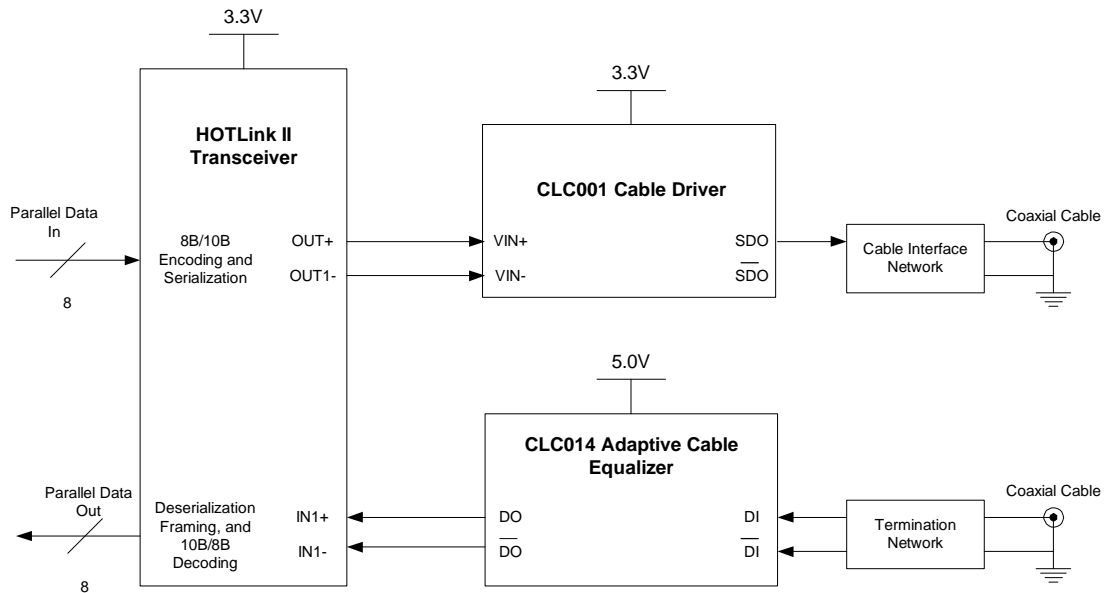


Figure 2. Typical Block Diagram of the Physical Layer in a DVB-ASI Video System

Schematic Diagram

Figure 3 shows the schematic connections between the HOTLink II device and the CLC001.

Transmitting Data to the Coaxial Cable

For SMPTE video, 10-bit parallel data is sent from upstream logic at a rate of 27 MHz for SD-SDI. The HOTLink II device serializes the data and sends it to the CLC001 Cable Driver at 270 Mb/s for SD-SDI. Cypress also offers solutions for implementing the SD-SDI scrambler.

For DVB-ASI video, 8-bit parallel data words are sent from upstream logic at a rate of 27 MHz. The HOTLink II 8B/10B encoder must be enabled to transmit the associated 10-bit code word with correct disparity for each 8-bit input character or special character.

In all cases, the CLC001 provides the appropriate 800mV $\pm 10\%$ amplitude swing at the signal outputs. Signals should be AC-coupled to the transmission line using a capacitor. This is shown in Figure 3.

Design Considerations for the Interface Between the HOTLink II Device and the CLC001

It is important to control trace impedances to minimize distortions caused by reflections. The following practices are recommended to ensure good signal integrity. The component names refer to those shown in Figure 3.

1. The traces connecting the HOTLink II outputs and cable driver inputs should have a uniform characteristic impedance of $Z_0 = 50\Omega$ or 75Ω .
2. R1 should be placed as close as possible to the VIN+/- inputs on the CLC001. $R1 = 2 Z_0$.
3. High speed traces should be curved to minimize impedance variations due to change of PCB trace width.
4. RREF should be $1.91k\Omega \pm 1\%$ to provide the appropriate output signal swing.

In addition to the recommendations listed here, National specifies other guidelines in their datasheets. These guidelines should also be considered when designing this system.



Interfacing the HOTLink II™ Transceiver with the 3.3V National CLC001 Cable Driver for Digital Video

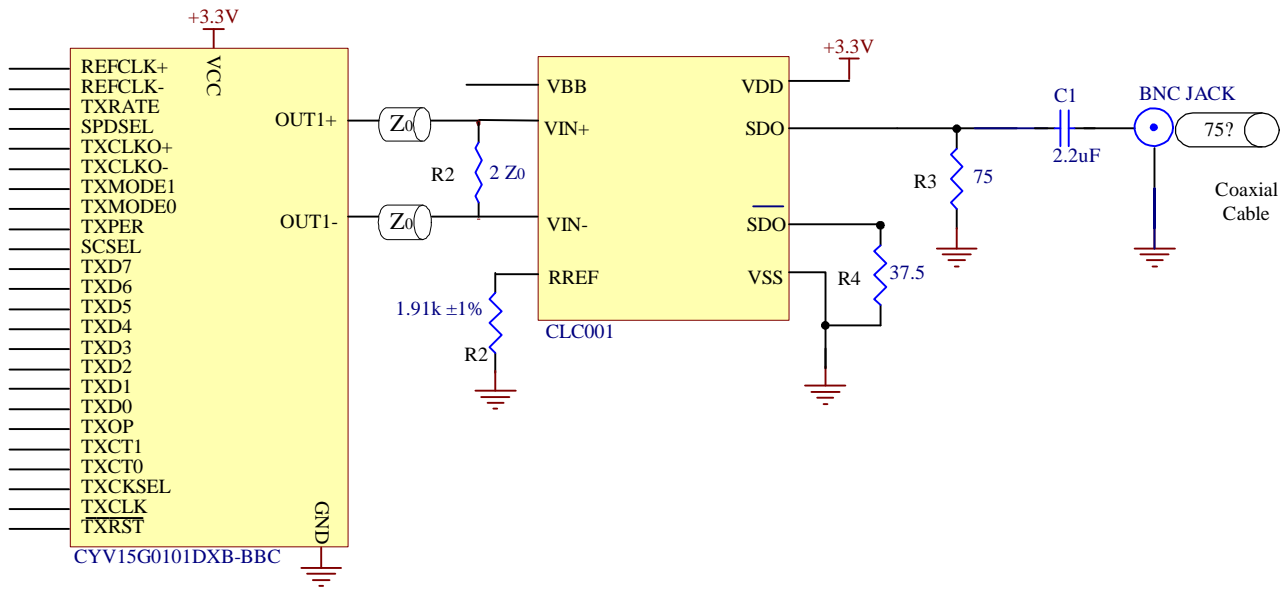


Figure 3. Schematic Diagram of the Connection of the Transmit Portion of the HOTLink II Transceiver with the CLC001 Cable Driver

Receiving Data from a Coaxial Cable

Serial data received from a coaxial cable is coupled to the CLC014 adaptive equalizer using an appropriate terminating and coupling network. Please see the application note entitled "Interfacing the HOTLink II Transceiver with the National 5.0 V CLC007 Cable Driver and the CLC014 Equalizer for Digital Video" for more details on the interface of the CLC014 with the HOTLink II device to receive serial data.

Conclusion

Cypress Semiconductor's HOTLink II family of video physical layer devices seamlessly interfaces with the National CLC001 Cable Driver. When interfaced correctly, the HOTLink II device and the Cable Driver provide a physical layer solution for a transmitter that is compliant with both the DVB-ASI and SMPTE SDI specifications.

References

1. CYP(V)15G0101DXB Single-Channel HOTLink II Transceiver, data sheet, Cypress Semiconductor, 2003.
2. CLC001 Serial Digital Cable Driver with Adjustable Outputs, data sheet, National Semiconductor, 2001.
3. Implement SMPTE 259M Using the CY7C9235/ CY7C9335, application note, Cypress Semiconductor, 1999.
4. Implementing DVB-ASI Serial Interfaces Using HOTLink, application note, Cypress Semiconductor, 2002.

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