# Interfacing the HOTLink II™ Transceiver with the National 5.0V CLC007 Cable Driver and the CLC014 Equalizer for Digital Video

## Introduction

The HOTLink II™ Transceiver is a point-to-point or point-to-multipoint communications building block allowing the transfer of data over high-speed serial links at signaling speeds ranging from 195 to 1500 MBaud. The device provides a selectable 8B/10B Encoder/Decoder and a Cypress Mode Multi-byte Framer that may be used for DVB-ASI applications. The encoding, decoding and framing functions may be bypassed for use in SMPTE SDI applications.

Cable drivers are used in serial digital video systems to meet the 800mV signal amplitude requirements found in the SMPTE 259M, 292M and DVB-ASI specifications. Adaptive equalizers are used to reverse the eye-closing effects of frequency-dependent attenuation of copper interconnects. This application note explains how to interface the HOTLink II Transceiver to National's CLC014 Adaptive Cable Equalizer and CLC007 Cable Driver for serial digital video communications over hundreds of meters of coaxial cable. All of the members of the HOTLink II video family, which include the CYV15G0101DXB, CYV15G0201DXB, CYV15G0401DXB, CYV15G0402DXB and CYV15G0403DXB, are compatible with these National devices.

## Block Diagrams

*Figure 1* and *Figure 2* show the block diagram of the connection of CYV15G0101DXB (HOTLink II PHY), the CLC007 (National Cable Driver) and the CLC014 (National Adaptive Equalizer). Although a single-channel device is shown in these figures, the same format is applicable to any device in the HOTLink II family, including dual-channel and quad-channel devices.

*Figure 1* shows the block diagram for a SMPTE system in which the HOTLink II device's 8B/10B Encoder, 10B/8B Decoder and Framer are disabled, and the SMPTE scrambling, descrambling and framing functions are provided by an external Cypress solution.

*Figure 2* shows the block diagram for a DVB-ASI system in which the 8B/10B Encoder, 10B/8B Decoder and Cypress Mode Multi-byte Framer are enabled. The non-SMPTE "CYP" devices may also be used in DVB-ASI systems.

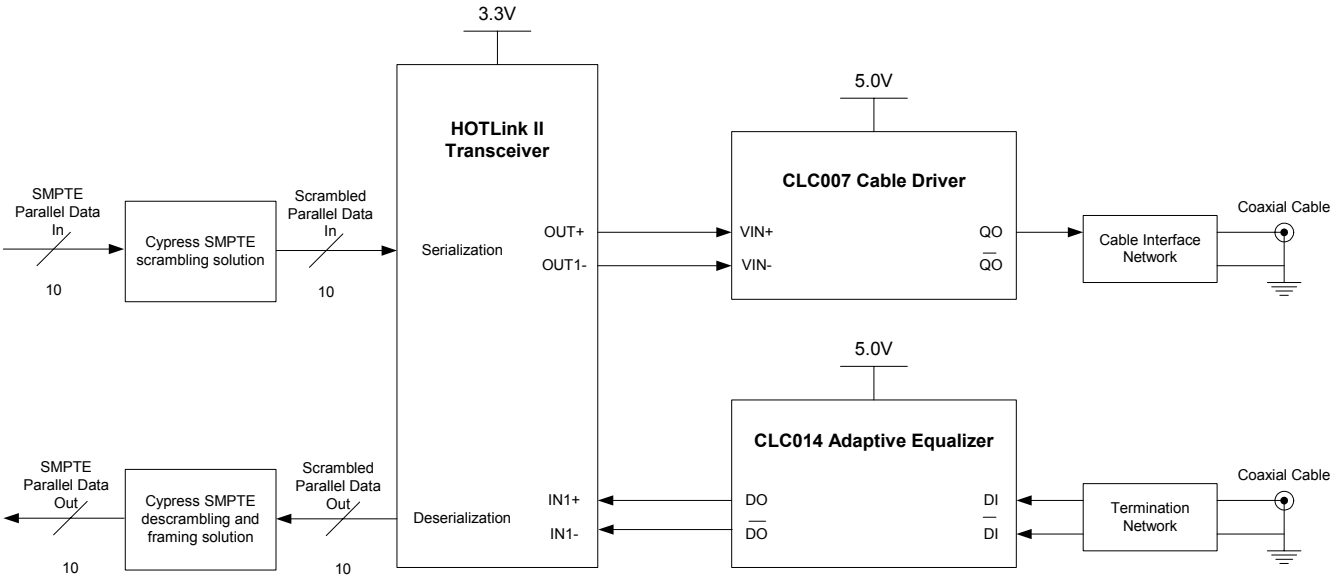


**Figure 1. Typical Block Diagram of the Physical Layer in a SMPTE SDI Video System**

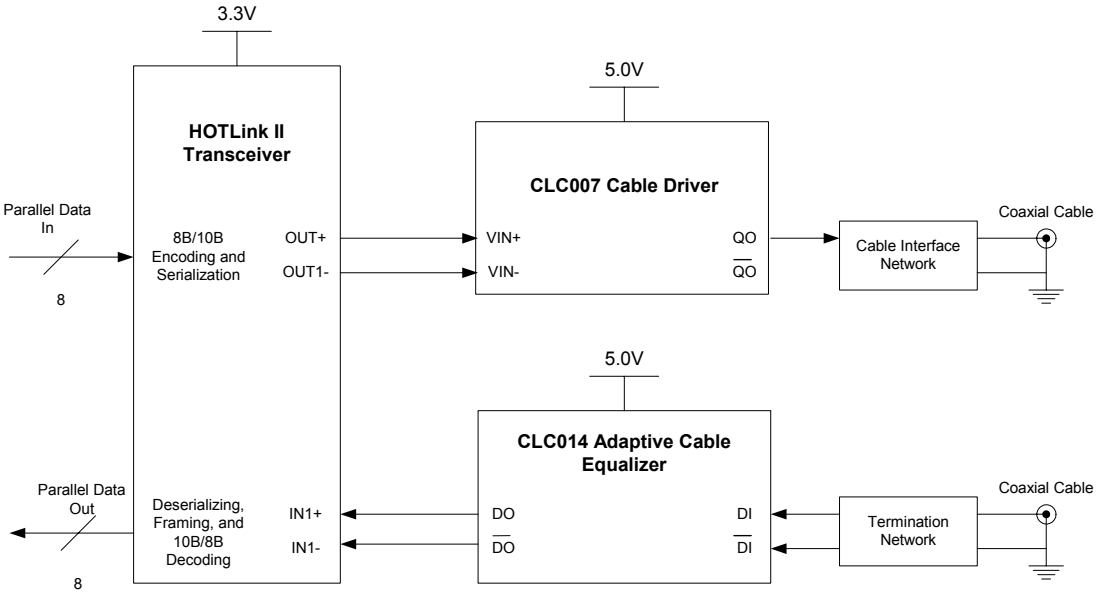


**Figure 2. Typical Block Diagram of the Physical Layer in a DVB-ASI Video System**

## Schematic Diagrams

*Figure 3* shows the schematic connections between the HOTLink II device and the CLC007 Cable Driver, and *Figure 4* shows the schematic connections between the HOTLink II device and the CLC014 Adaptive Cable Equalizer.

### Transmitting Data to the Coaxial Cable

For SMPTE video, 10-bit parallel words are sent from upstream logic at a rate of 27 MHz for SD-SDI. The HOTLink II device serializes the data and sends it to the CLC007 Cable Driver at 270 Mb/s for SD-SDI. Cypress also offers solutions for implementing the SD-SDI scrambler.

For DVB-ASI video, 8-bit parallel bytes are sent from upstream logic at a rate of 27 MHz. The HOTLink II 8B/10B encoder must be enabled to transmit the associated 10-bit code word with the correct disparity for each 8-bit input character or special character.

In all cases, the CLC007 provides the appropriate 800-mV amplitude swing at the signal outputs. Signals should be coupled to the transmission line using capacitors. This is shown in *Figure 3*.

### Design Considerations for the Interface Between the HOTLink II Device and the CLC007

It is important to control trace impedances to minimize distortions caused by reflections. The following practices are recommended to ensure good signal integrity. The component names refer to those shown in *Figure 3*.

1. The traces connecting the HOTLink II outputs and cable driver inputs should have a uniform characteristic impedance of 50Ω or 75Ω.
2. For $Z_0$=50Ω, R4=R5=51.1Ω. For $Z_0$=75Ω, R4=R5=75Ω.
3. High speed traces should be curved to minimize impedance variations due to change of PCB trace width.
4. R4-R7 and C4 should be as close as possible to the CLC007 VIN+/- inputs. C2 and C3 should be as close as possible to the OUT+/- outputs on the HOTLink II device.

In addition to the recommendations listed here, National specifies other guidelines in their datasheets. These guidelines should also be considered when designing this system.

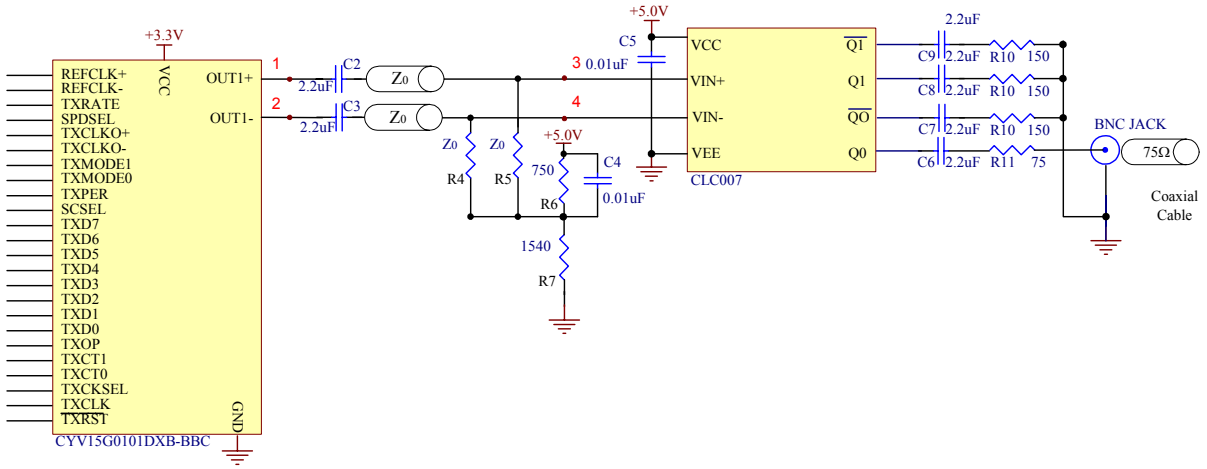


**Figure 3. Schematic Diagram of the Connection of the Transmit Portion of the HOTLink II Transceiver with the CLC007 Cable Driver**

### Receiving Data from a Coaxial Cable

Serial data received from a coaxial cable is coupled to the CLC014 adaptive equalizer using an appropriate terminating and coupling network. As with the cable driver, the adaptive equalizer should be coupled to the transmission line using capacitors. This is shown in *Figure 4*.

The equalizer opens the eye by reversing the effects of the frequency-dependent attenuation of the copper link. This equalized differential signal is then presented to the serial inputs of the HOTLink II device.

For SMPTE SD-SDI, the deserialized data is output onto the HOTLink II device's 10-bit receive bus, along with a recovered clock (RXCLK) operating at 27 MHz. The received parallel data is then delivered to a descrambler/framer. Cypress offers a descrambling and framing solution for SD-SDI.

For DVB-ASI systems, the received data is framed, decoded and placed on the HOTLink II device's 8-bit receive bus along with a 27 MHz recovered clock. The deserialized data can also be clocked out with the local reference clock using the optional Elasticity Buffer in the HOTLink II receiver. When the Elasticity Buffer is enabled, K28.5 framing characters will be inserted or deleted to/from the datastream to absorb the frequency difference between the two clock domains (recovered clock and reference clock). The framing is implemented using the Cypress Mode Multi-byte Framer, which frames on two instances of K28.5 having identical 10-bit boundaries in a space of 50 bits. This is optimized for DVB-ASI, which transmits two consecutive K28.5 characters between packets. The RXST[2:0] bus indicates the presence of valid data and framing characters. The upstream logic decodes the signal on this bus to remove K28.5 characters from the data stream. See the HOTLink II device's data sheet for the interpretation of the RXST[2:0] bus.

### Design Considerations for the Interface Between the HOTLink II Device and the CLC014 Adaptive Equalizer

At the high data rates used to transmit SMPTE SDI data, it is important to control the trace impedances to minimize distortions caused by reflections. The following practices are recommended to optimize performance of the adaptive equalizer. The component names refer to those shown in *Figure 4*.

1. The traces connecting the HOTLink II inputs and equalizer outputs should have a uniform characteristic impedance. *Figure 4* assumes $Z_0$=75Ω. For 75Ω traces, R12 should be 150Ω, and for 50Ω trances, R12 should be 100Ω.
2. High speed traces should be curved to minimize impedance changes.
3. C10, C11, R13 and R14 should be as close as possible to the D0/D0 outputs of the CLC014.
4. R12 should be as close as possible to the IN1± inputs on the HOTLink II transceiver.
5. The components at the input of the equalizer (C18, C19, R15-R18) should be as close as possible to the DI inputs on the CLC014.
6. Consult the CLC014 datasheet for the selection of the value of C13.

In addition to the recommendations listed here, National specifies other guidelines in the CLC014 data sheet. These guidelines should also be considered when designing this system.

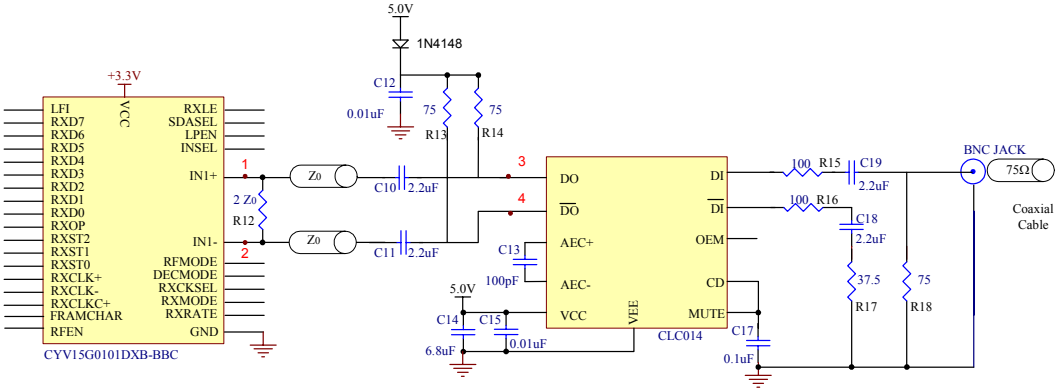


**Figure 4. Schematic Diagram of the Connection of the Receiver Portion of the HOTLink II Transceiver with the CLC014 Adaptive Cable Equalizer**

## Conclusion

Cypress Semiconductor's HOTLink II Family of Video Physical Layer Devices seamlessly interfaces with the National CLC007/CLC014 Cable Driver and Adaptive Equalizer chipset. When interfaced correctly, Cypress Semiconductor's HOTLink II transceiver, and National's CLC007/CLC014 Cable Driver and Adaptive Equalizer provide a DVB-ASI- and SMPTE SDI-compliant physical layer solution.

### References

1. *CYP(V)15G0101DXB Single-Channel HOTLink II Transceiver*, data sheet, Cypress Semiconductor, 2003.
2. *CLC007 Serial Digital Cable Driver with Dual Complementary Outputs*, data sheet, National Semiconductor, 1998.
3. *CLC014 Adaptive Cable Equalizer for High-Speed Data Recovery*, data sheet, National Semiconductor, 2003.
4. *Implement SMPTE 259M Using The CY7C9235/CY7C9335*, application note, Cypress Semiconductor,1999.
5. *Implementing DVB-ASI Serial Interfaces Using HOTLink®* application note, Cypress Semiconductor, 2002.



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