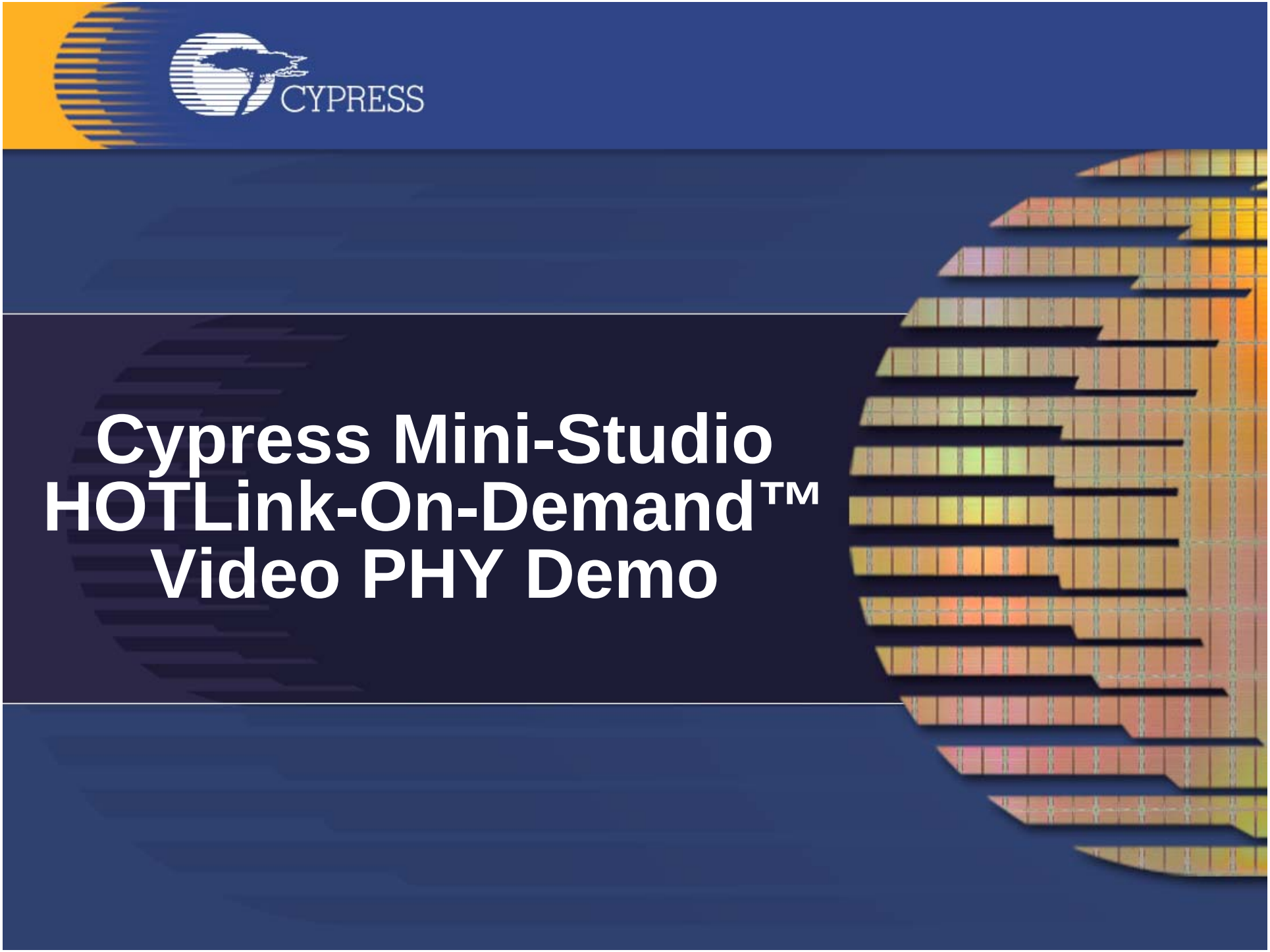

CYPRESS
Cypress Mini-Studio
HOTLink-On-Demand™
Video PHY Demo

Professional Video Market Trends

- **Worldwide transition to digital video through 2010**
- **Growing consumer demand for HDTV**
- **Multi-format equipment most sought-after**
- **Growth in modular products for migration**
- **Decentralized production/editing environment**

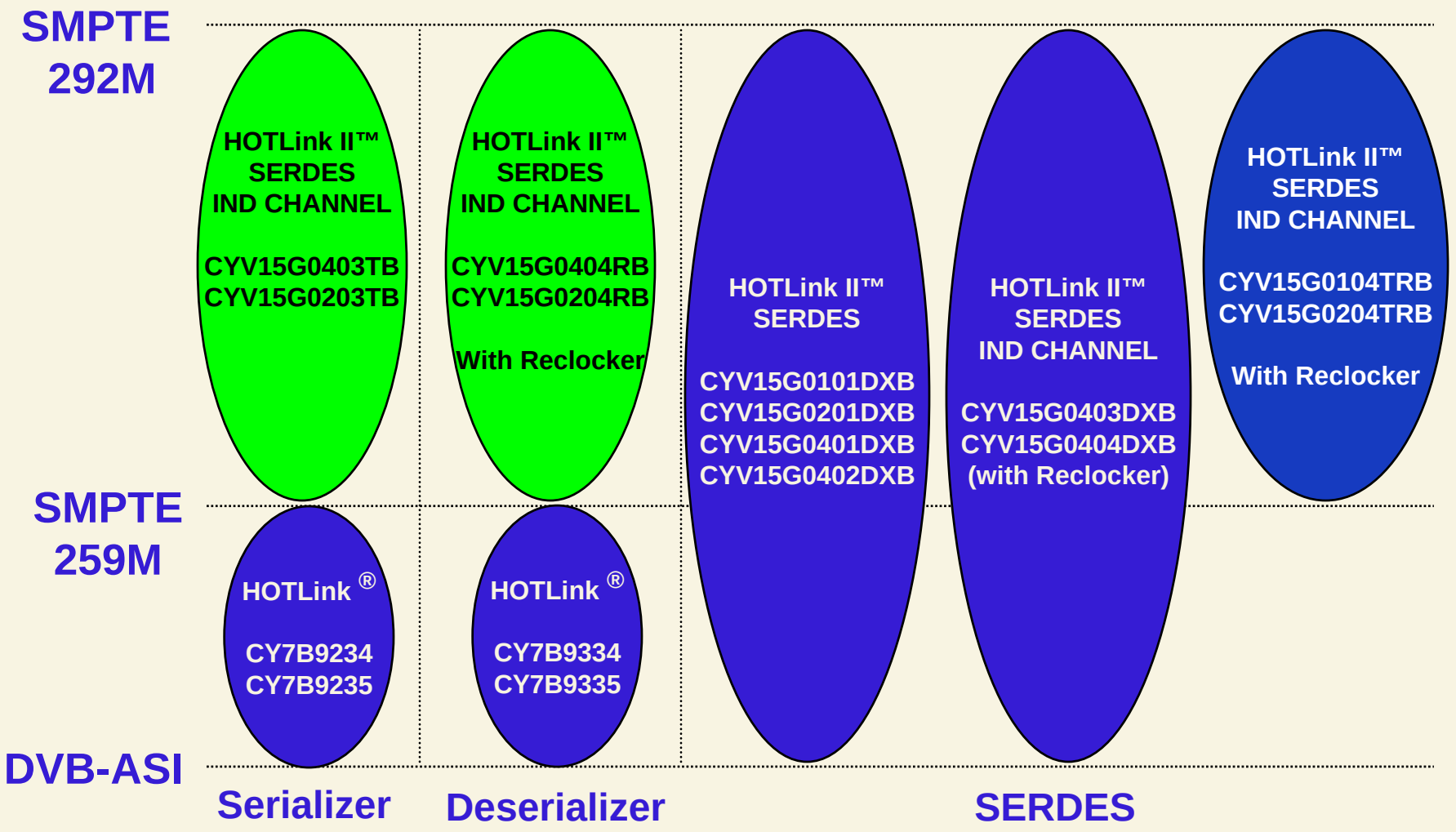
HOTLink-On-Demand™ Video PHY Benefits

- **Scalable and flexible Video PHY portfolio**
  - **Multi-channel support – Single,Dual, Quads**
  - **Multi-format support – Independent channel (SD/HD)**
  - **Multiple options – Transmit, Receive, Reclocker**

- **Board layout and ease of use – "No Assembly Required"**
  - **Integrated VCOs**
  - **Wide SMPTE jitter margin**
  - **No channel crosstalk**
  - **Failsafe clock**
  - **Single power rail**

"Our goal is to team with best-in-class video solution providers to ensure that our customers receive the highest quality and function at a reasonable price," said John Abt, president, AJA Video Systems. "The HOTLink II video transceiver enables us to do just that by providing enhanced levels of integration and proven performance required to support our KONA HD video capture cards as well as several of our video converter products."

HOTLink-On-Demand™ Video Portfolio

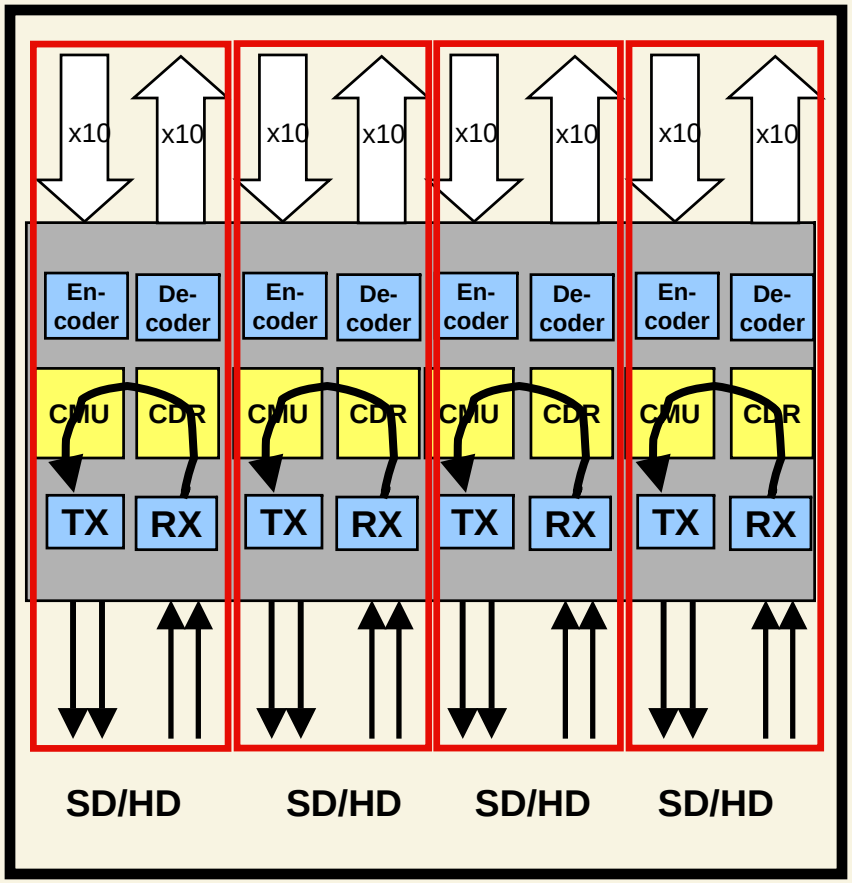


In Production

Samples

Singles, Duals, Quads available

Independent Channel Reclocking HOTLink II™ SERDES

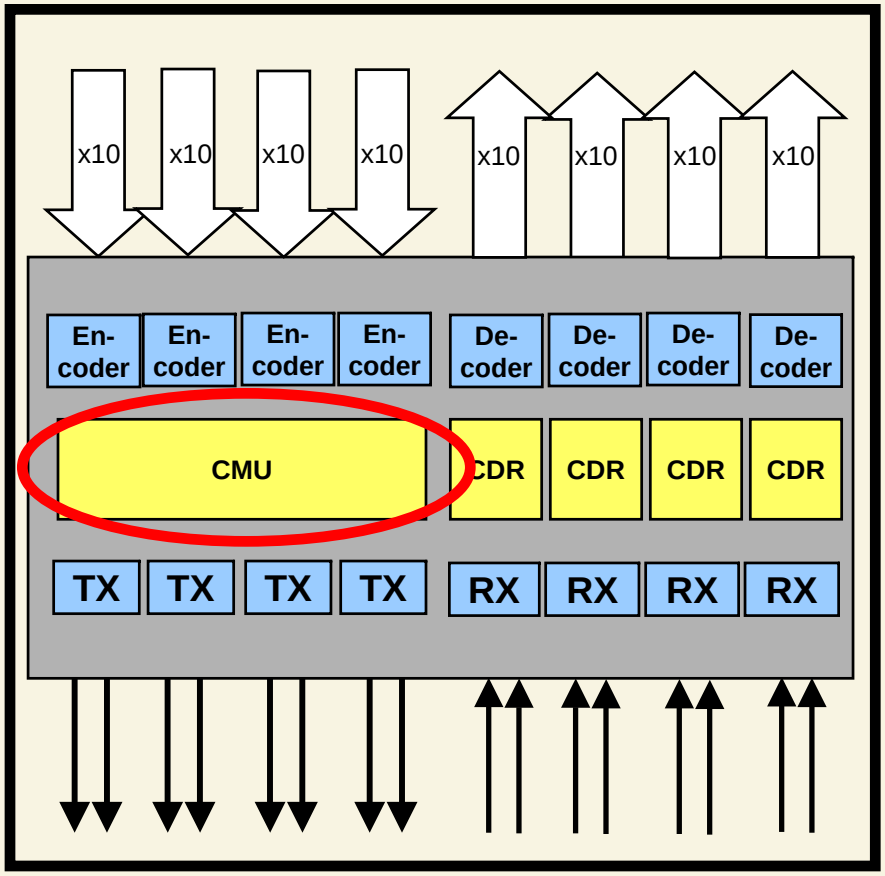


CYV15G0404DXB Block Diagram

- **Multi-format support per channel**
- **Reclocking function on each channel – "Serial In, Serial Out"**
- **Failsafe clock**
- **Integrated VCOs**
- **Single power rail**

Quad Channel HOTLink II™ SERDES Features

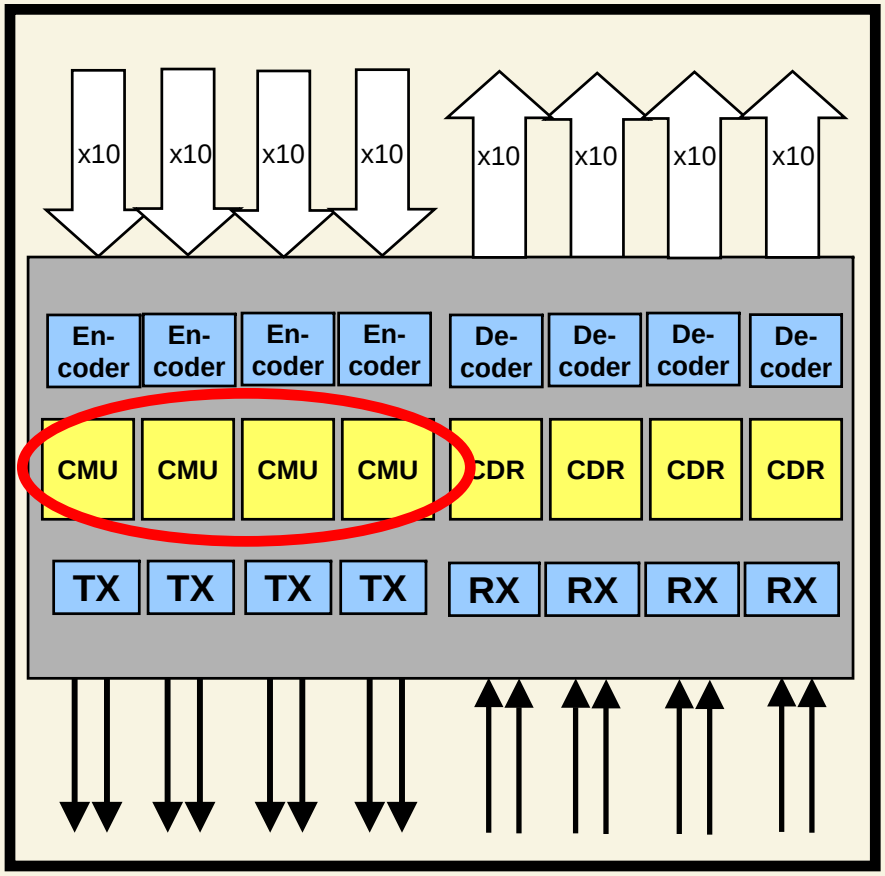
CYV15G0401DXB-BGC



- Quad channel operation
- 0.2 – 1.5 GBd/channel
- Selectable 8B/10B coding
- Compliant to DVB-ASI, SMPTE-259M, SMPTE-292M
- Selectable serial inputs
- Redundant serial outputs
- Built In Self Test (BIST)

Quad Independent Channel HOTLink II™ SERDES Features

CYV15G0403DXB-BGC



- Independent channel operation
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- Selectable 8B/10B coding
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- Selectable serial inputs
- Redundant serial outputs
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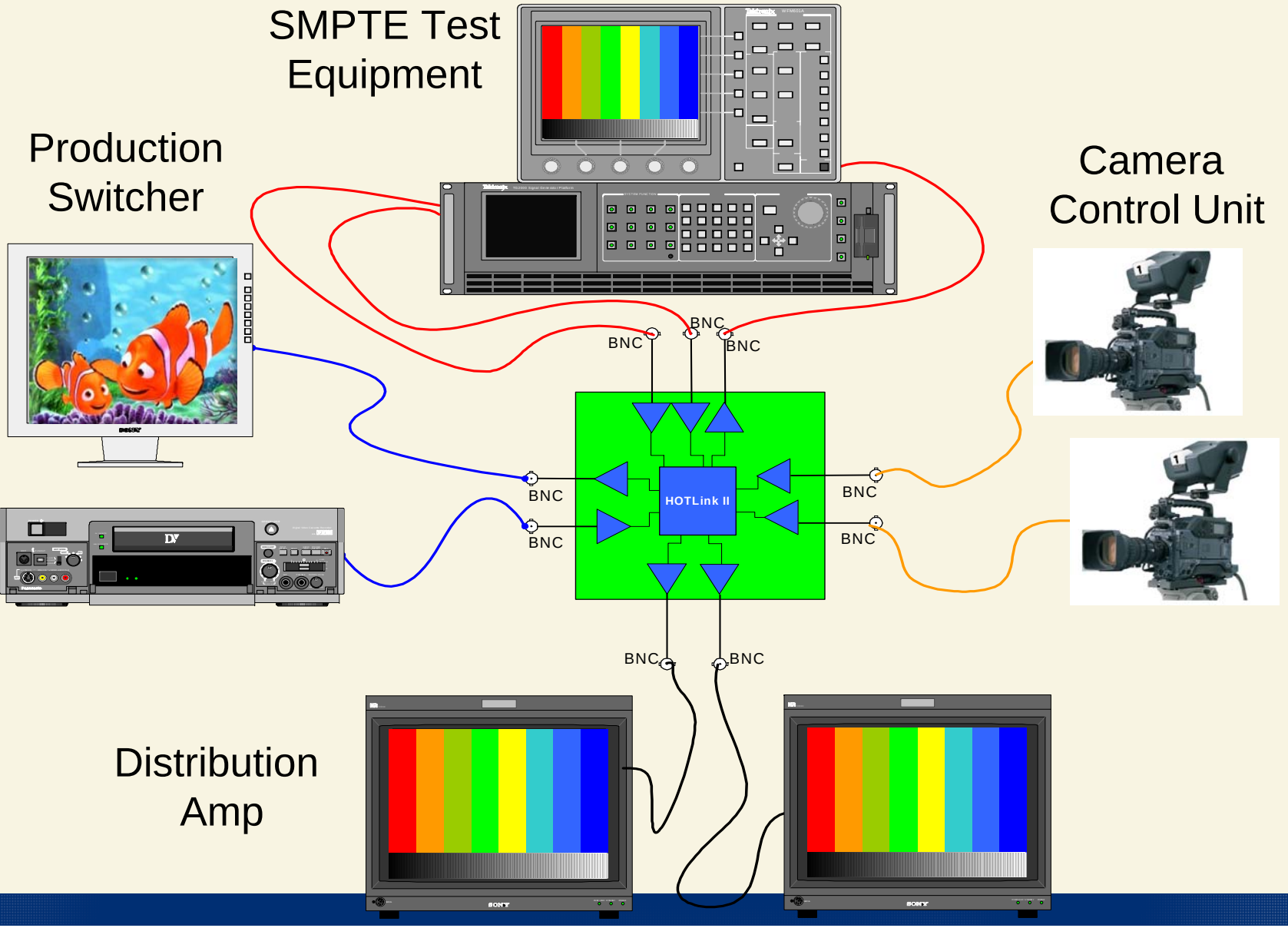
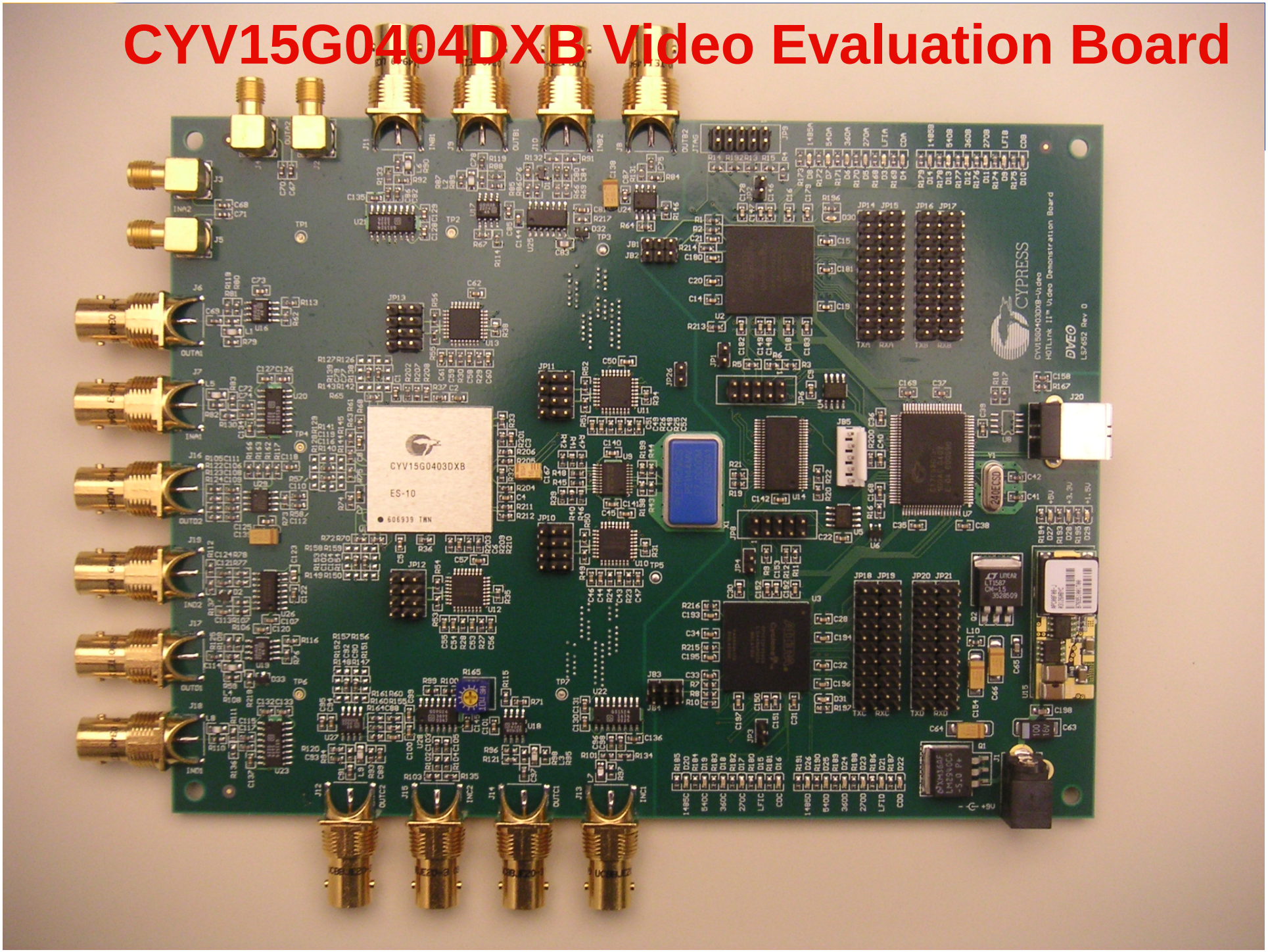
Cypress Mini-Studio Demo

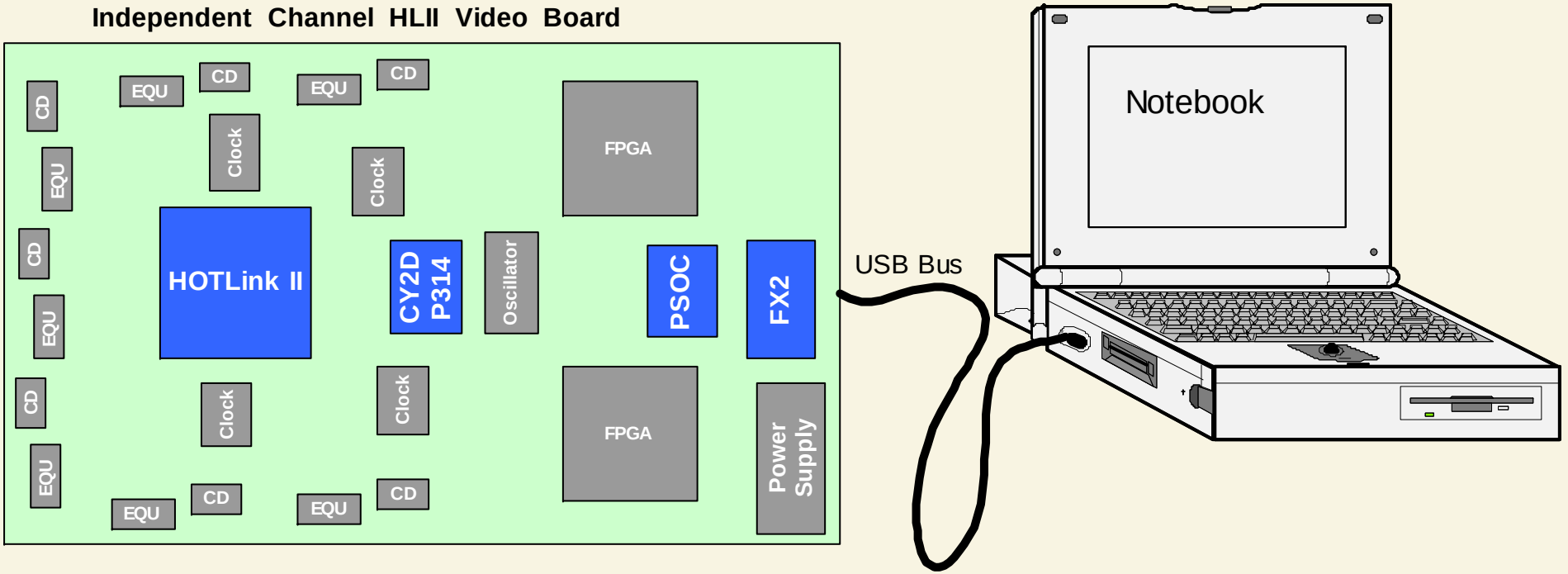


CYV15G0404DXB Video Evaluation Board

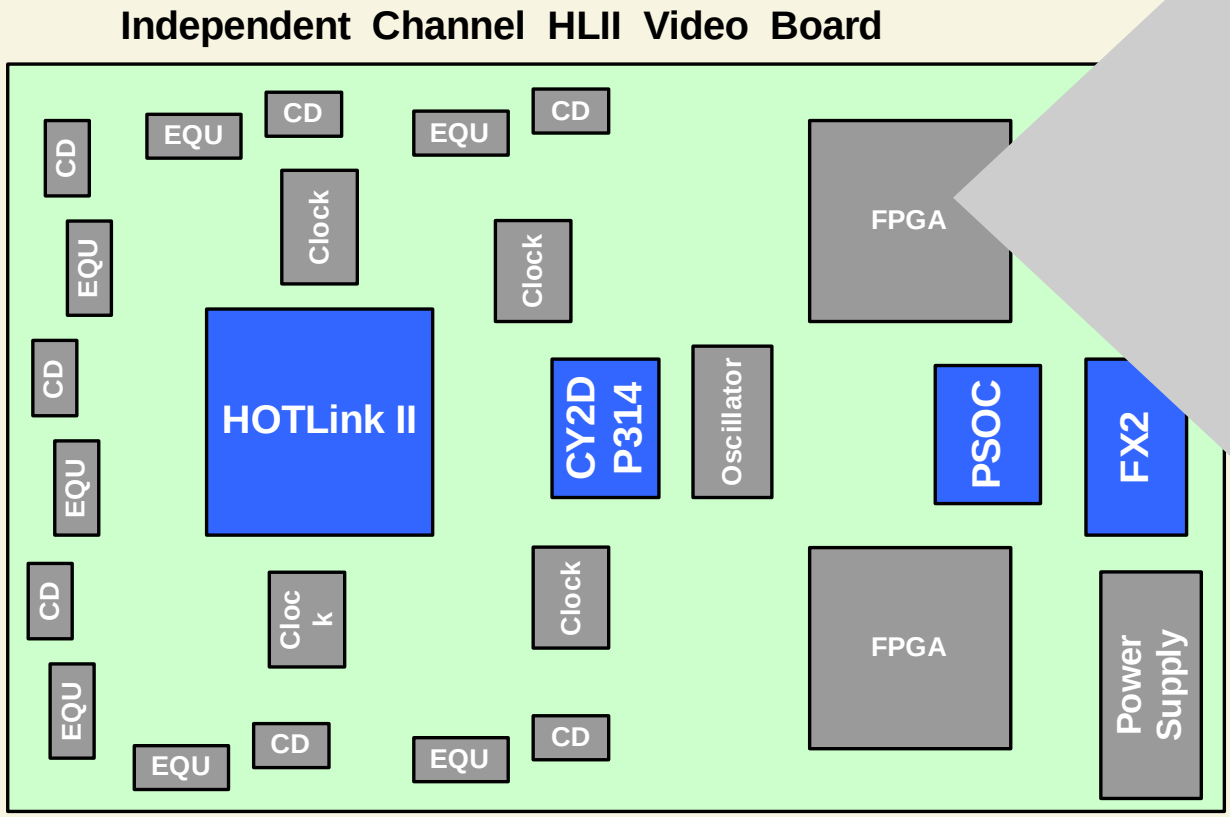


Board Configuration

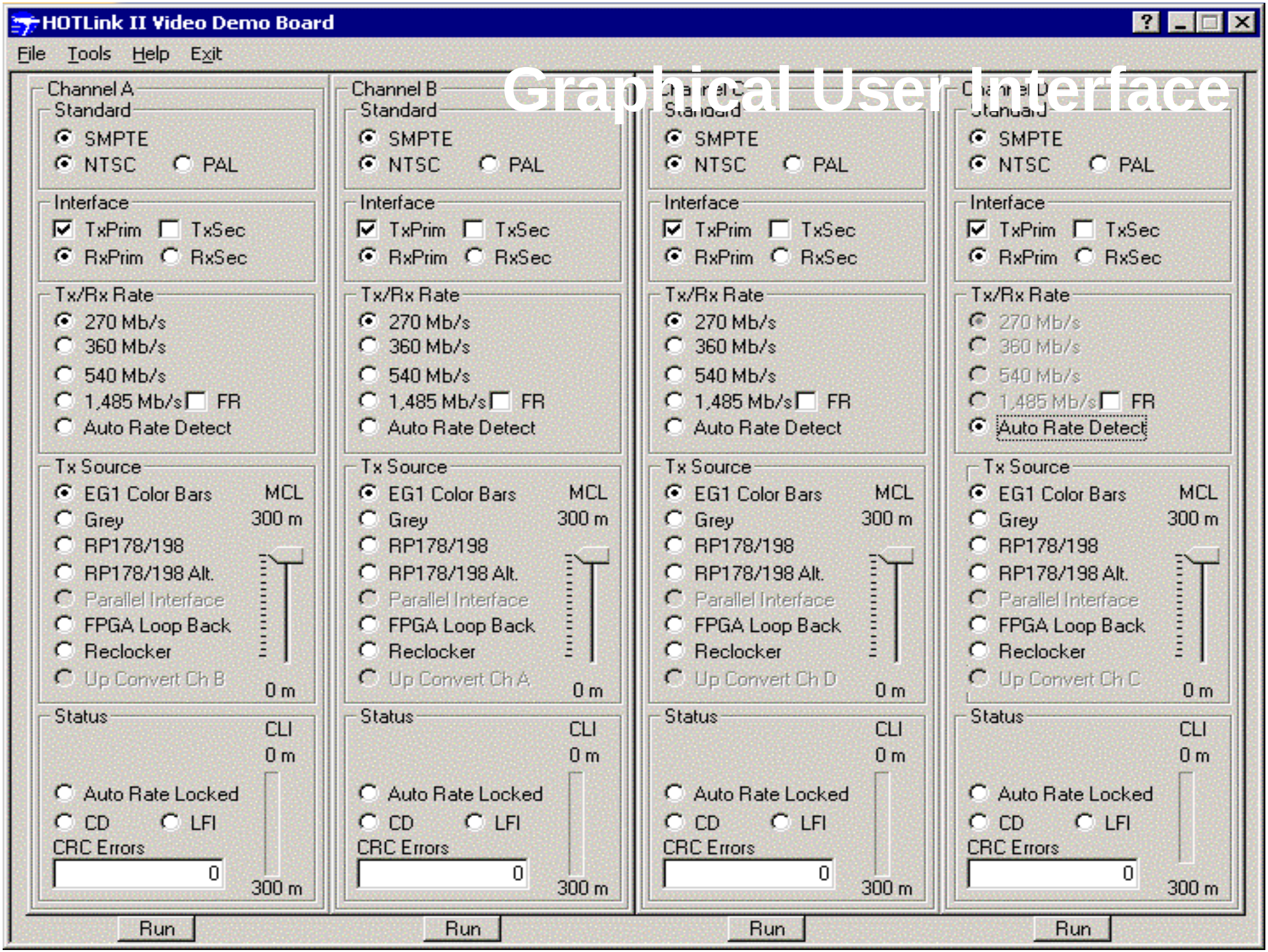
- Configure Board via USB FX2 device
- Configure HOTLink II using I2C via PSOC



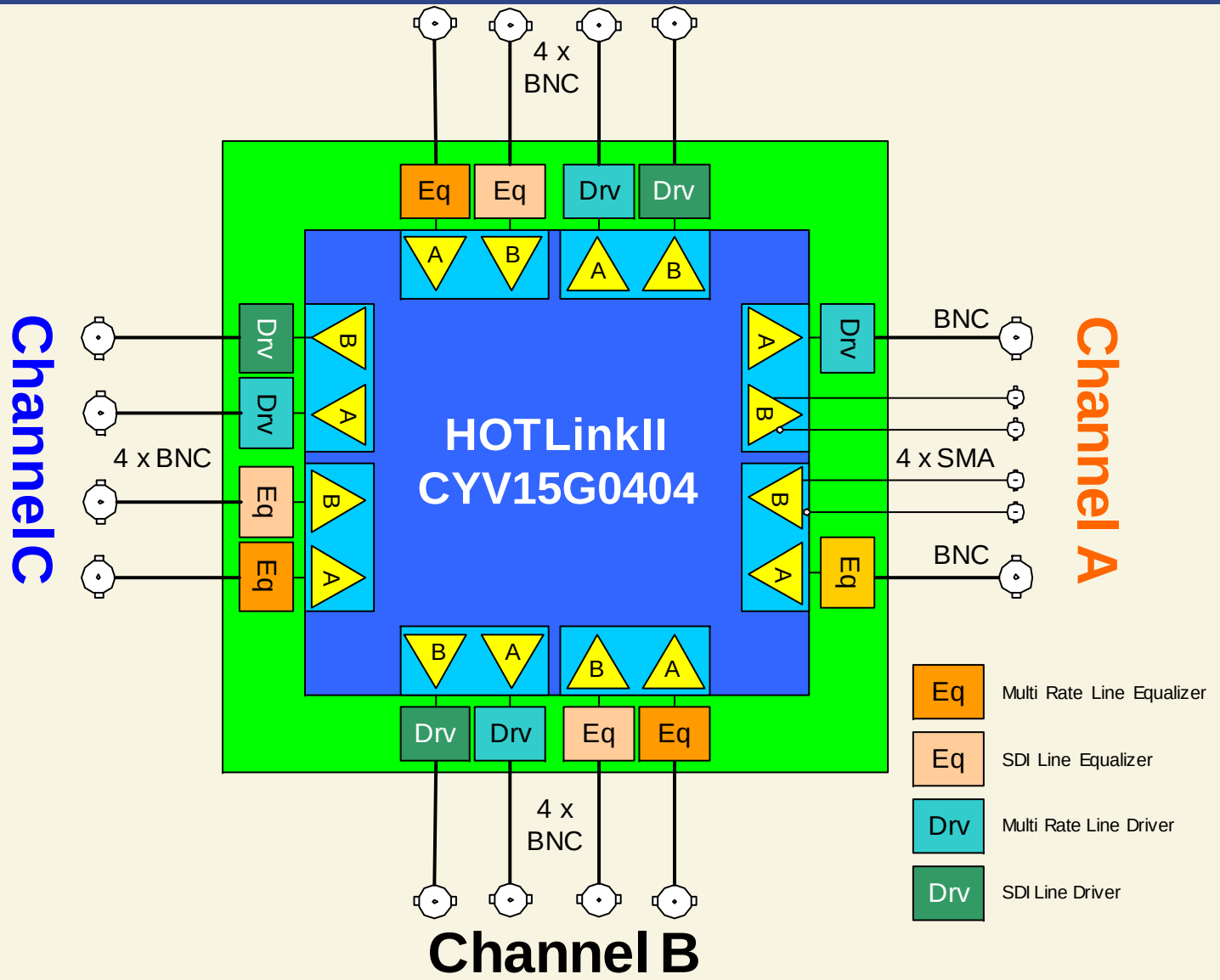
FPGA IP



SMPTE 259 Scrambler/NRZI Encoder	SMPTE 259 Decrambler/NRZI Decoder
SMPTE 292 Scrambler/NRZI Encoder	SMPTE 292 Decrambler/NRZI Decoder
SMPTE 292 EG1/ RP198/Grey Generator	SMPTE 259 EG1/ RP178/Grey Generator
SMPTE 292 CRC Checking	SMPTE 259 CRC Checking as per RP165
Auto rate-detection	SMPTE 259M-D and SMPTE 344M

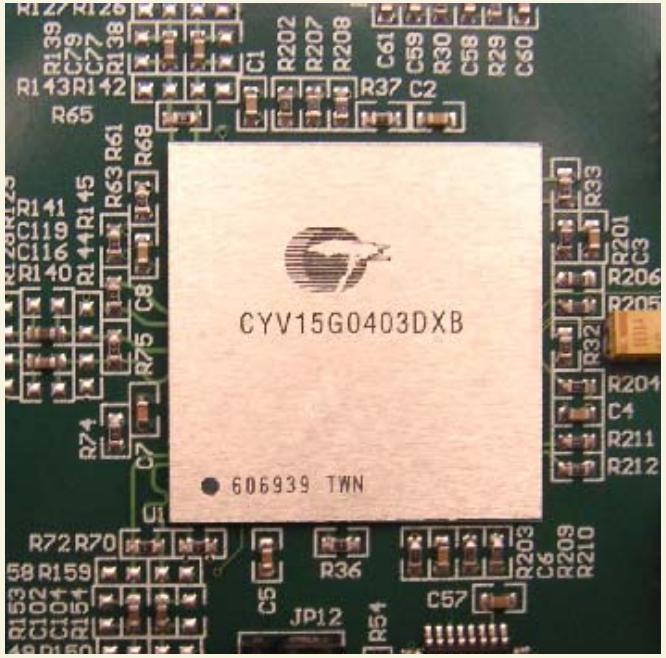

HOTLink II Video Demo Board
File Tools Help Exit
Graphical User Interface
Channel A
Channel B
Standard
SMPTE
NTSC PAL
Interface
TxPrim TxSec
RxPrim RxSec
Tx/Rx Rate
270 Mb/s
360 Mb/s
540 Mb/s
1,485 Mb/s FR
Auto Rate Detect
Tx Source
EG1 Color Bars
Grey
RP178/198
RP178/198 Alt.
Parallel Interface
FPGA Loop Back
Reclocker
Up Convert Ch B
Up Convert Ch A
Up Convert Ch D
Up Convert Ch C
MCL
300 m
0 m
Status
CLI
0 m
Auto Rate Locked
CD LFI
CRC Errors
0
300 m
Run

Video Board Model for Demo



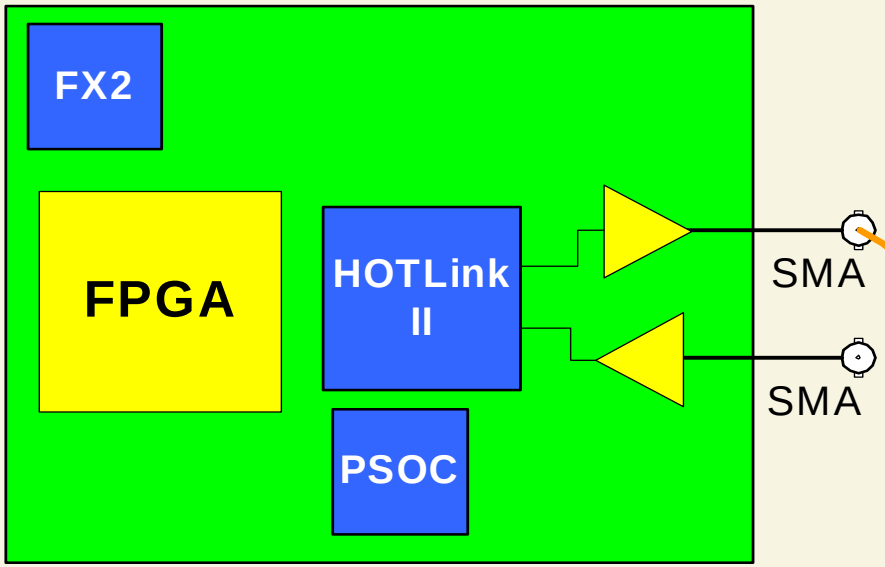
Cypress Video Features Checklist

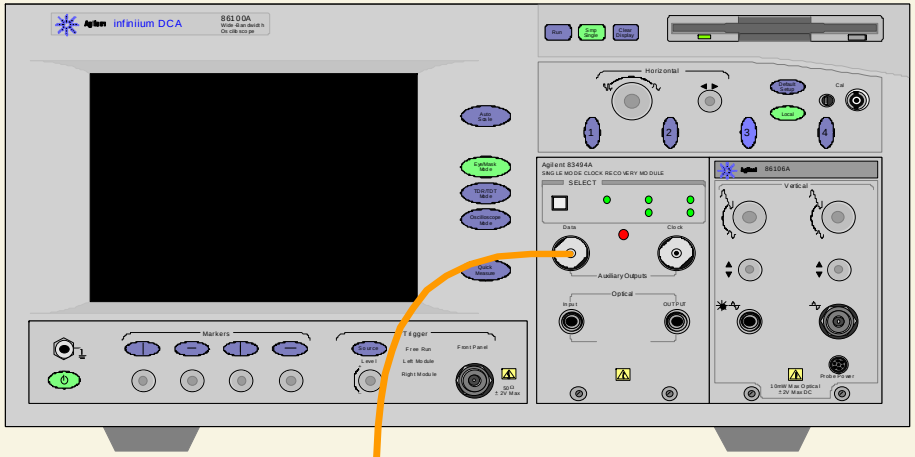
- Independent Channel Operation
- Broadcast Test Equipment Validated
- Integrated Transceiver Channels
- SMPTE Pathological Compliance
- High Ref Clock Input Tolerance
- Auto-Rate Detection
- Reclocker
- HD-SDI Support
- Selectable Inputs
- Interfaces to Common EQ/CD
- Per-Channel Power-Down
- SD-SDI Support
- Redundant Outputs
- SMPTE Jitter Compliance
- Low Power
- Cost Effective Solution
- Ease of Design



Channel A Demo

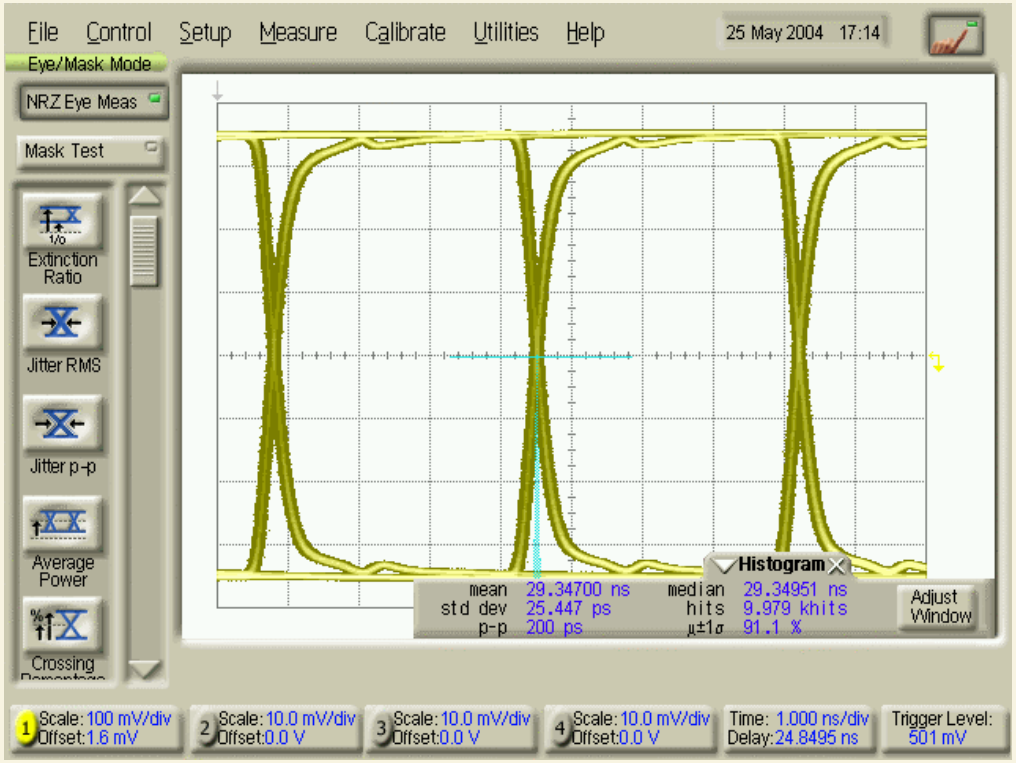
- ☑ Low Jitter
- ☑ 10-bit support (pin count)
- ☑ Cost Effective Solution
- ☑ Low Power





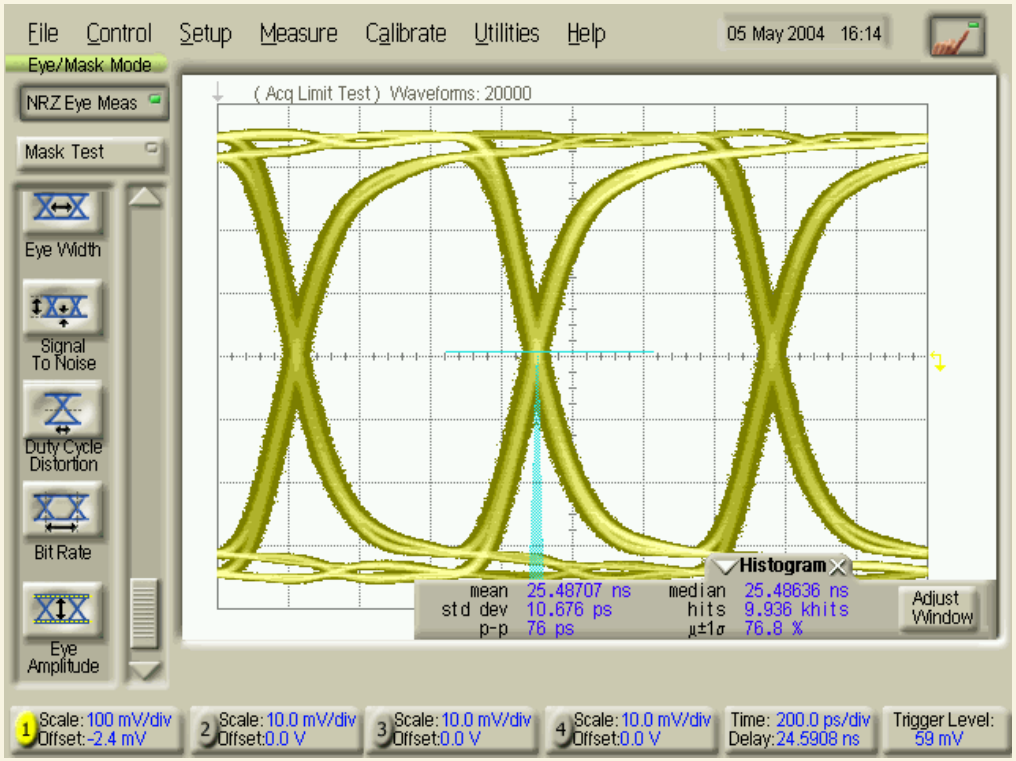
Cypress SD Transmit Jitter Generation Eye diagram

- SD Transmit Jitter Eye Diagram
- Broadband Histogram without SMPTE filter
- SMPTE Spec with Filter is .2UI or 740pS
- Histogram measurement is 200pS



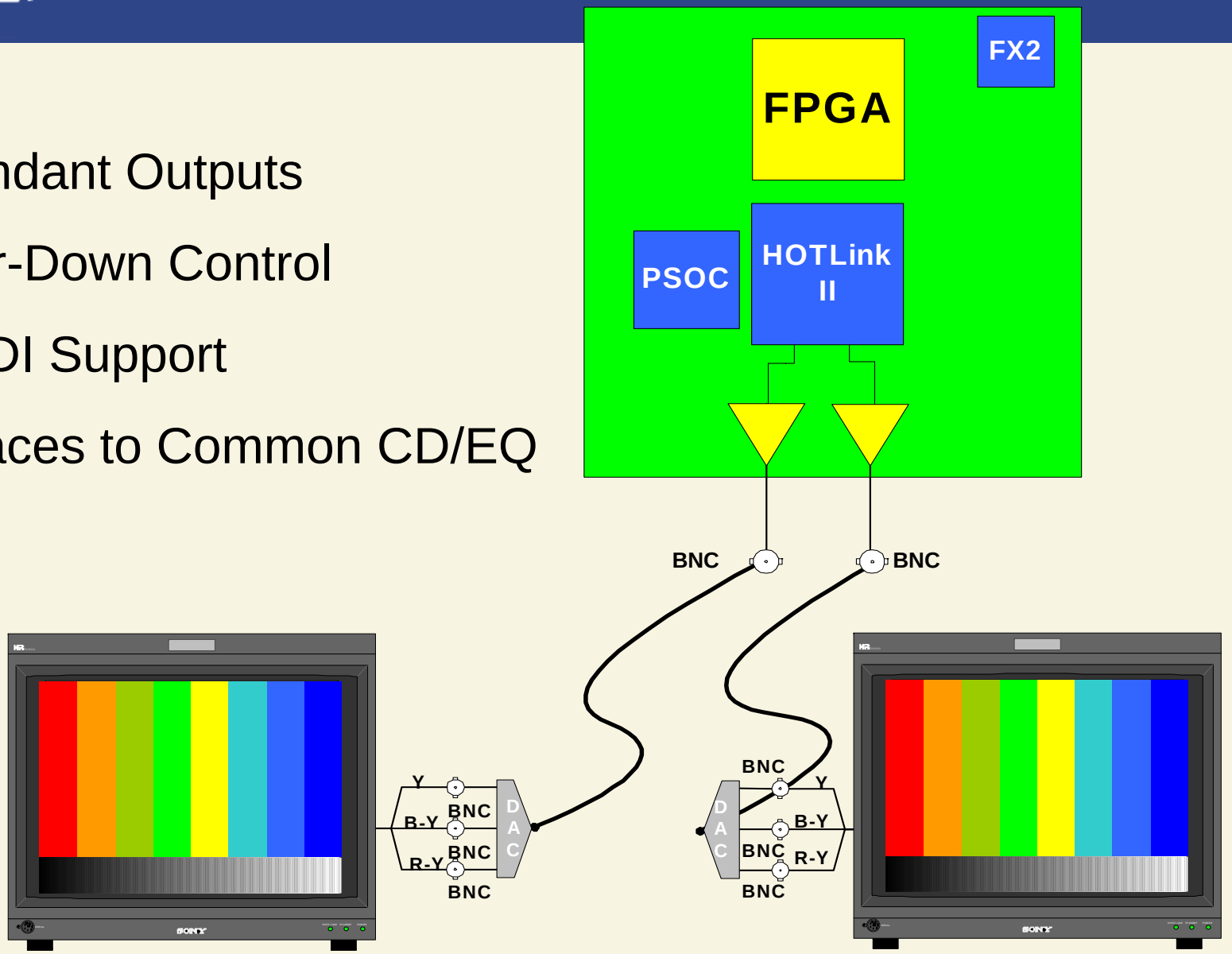
Cypress HD Transmit Jitter Generation Eye diagram

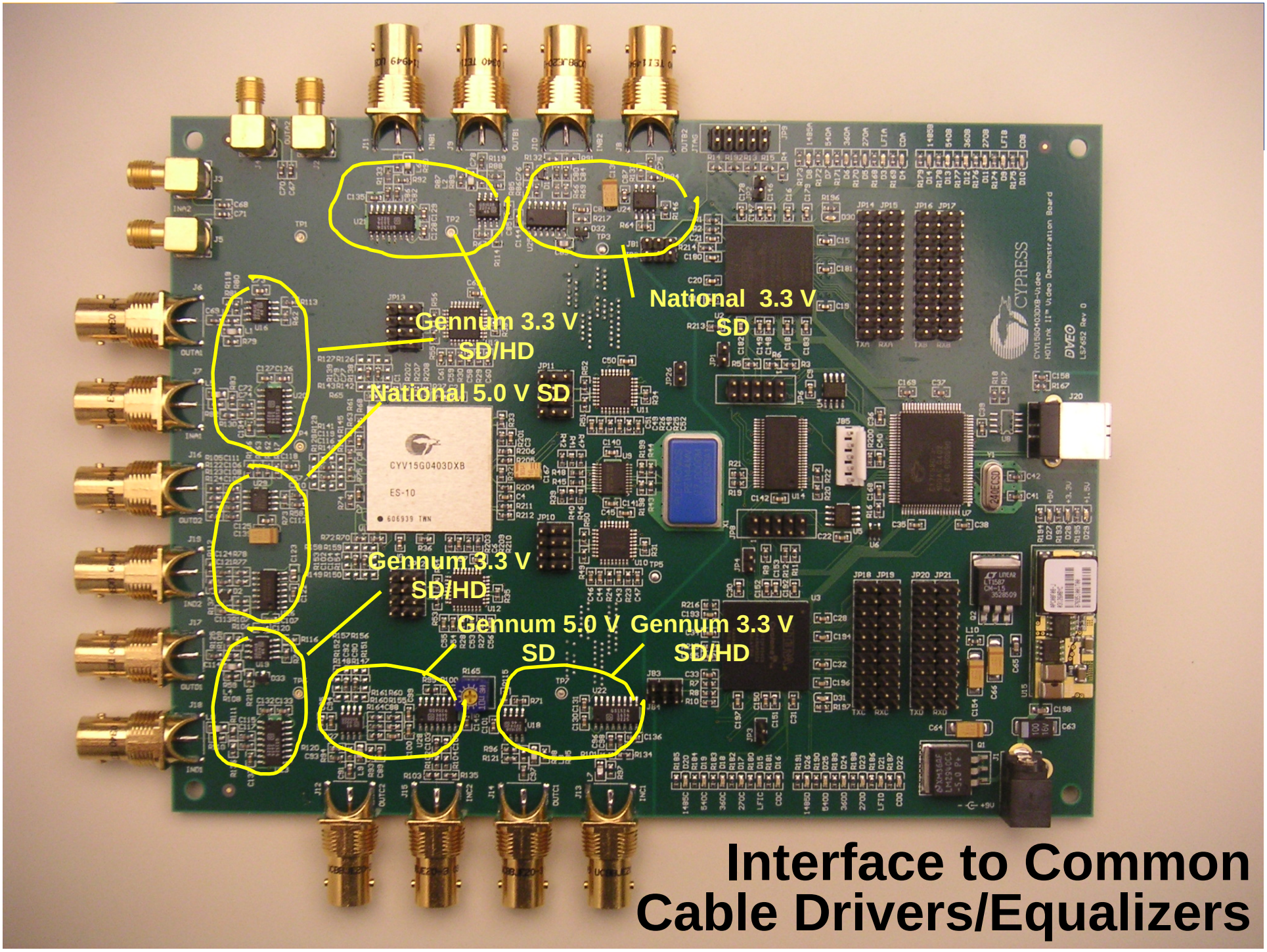
- HD Transmit Jitter Eye Diagram
- Broadband Histogram without SMPTE filter
- SMPTE Spec with Filter is .2UI or 135pS
- Histogram measurement is 76pS



Channel B Demo

- ☑Redundant Outputs
- ☑Power-Down Control
- ☑SD-SDI Support
- ☑Interfaces to Common CD/EQ

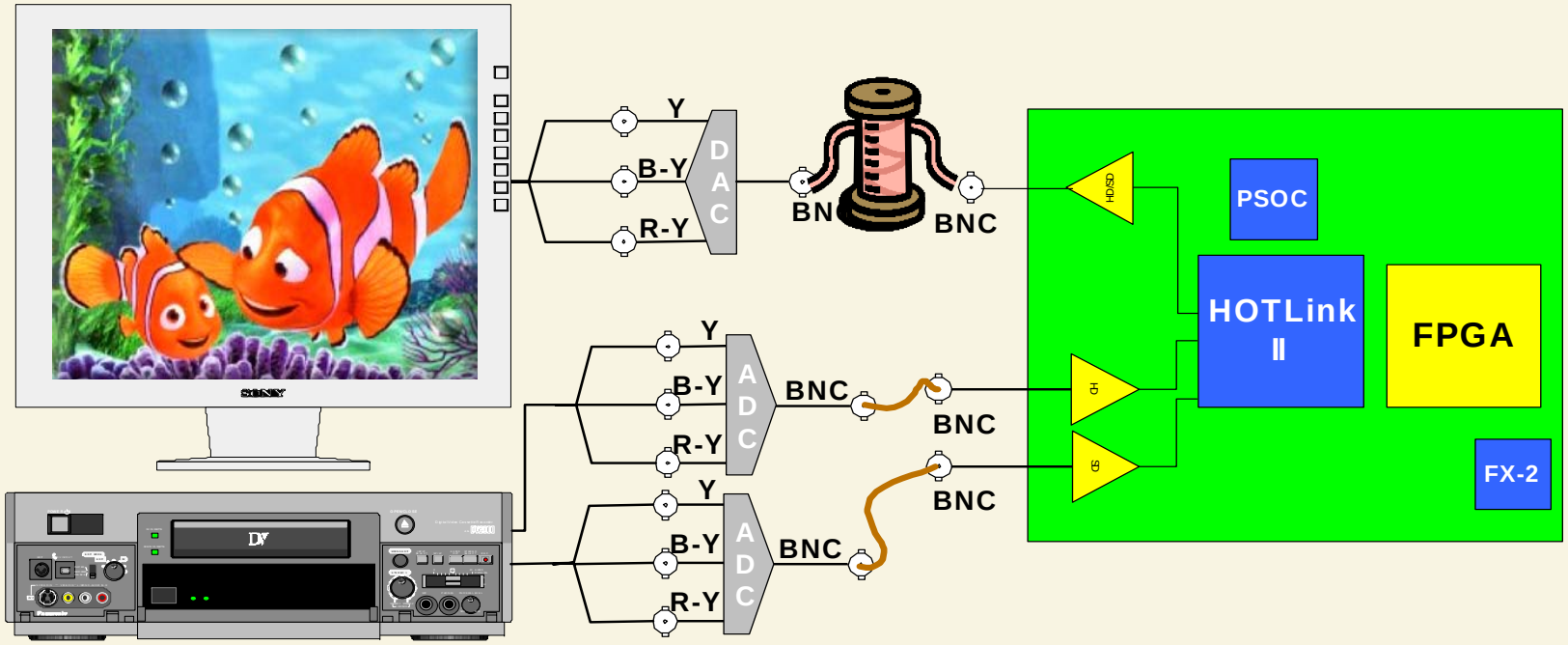




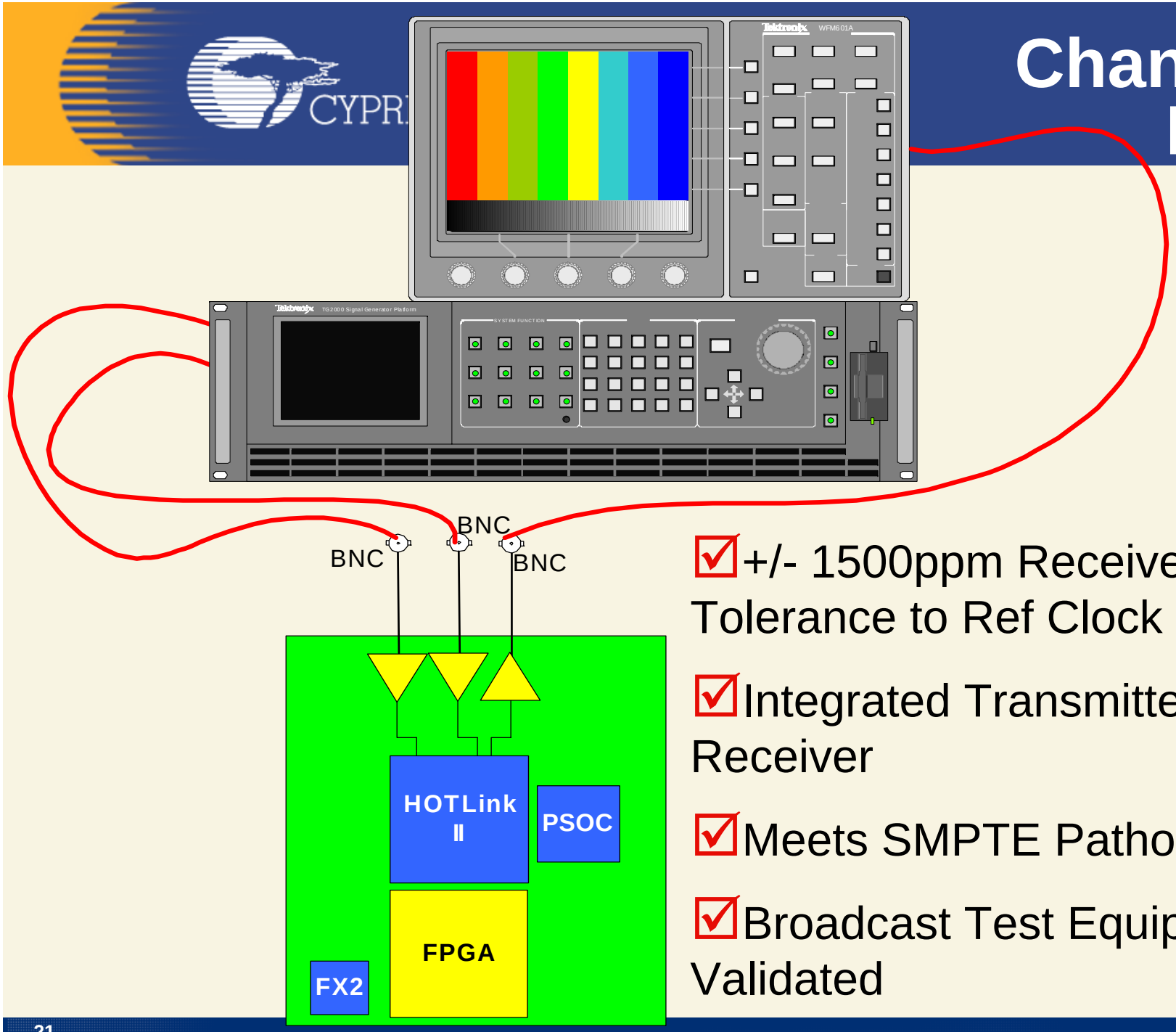
Interface to Common Cable Drivers/Equalizers

Channel C Demo

- ☑ HD-SDI Support
- ☑ SD-SDI Support
- ☑ Auto Rate-detection
- ☑ Reclocker
- ☑ Selectable Serial Inputs



Channel D Demo

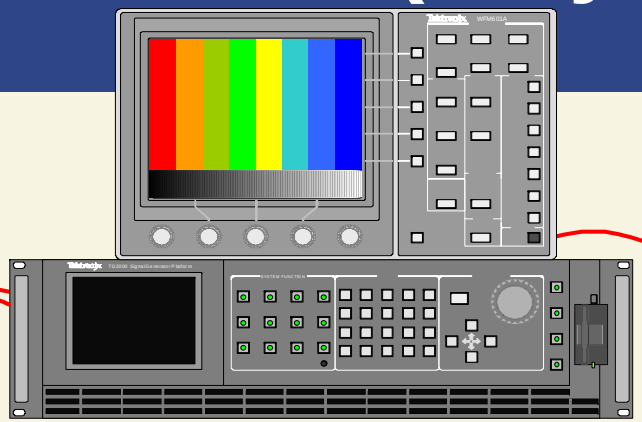


- ☑ +/- 1500ppm Receive Tolerance to Ref Clock
- ☑ Integrated Transmitter/ Receiver
- ☑ Meets SMPTE Pathologicals
- ☑ Broadcast Test Equipment Validated

Channel E(verything) Demo

Channel D (1.4835 Gbps):

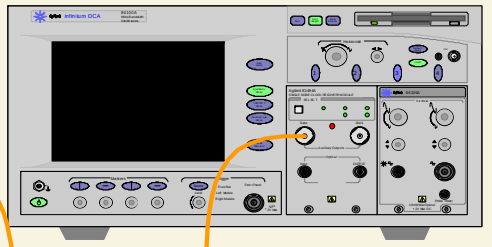
- 1500 ppm tolerance
- Pathological Compliance
- Broadcast test equipment validated

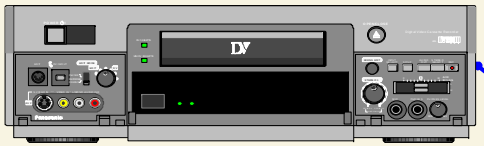


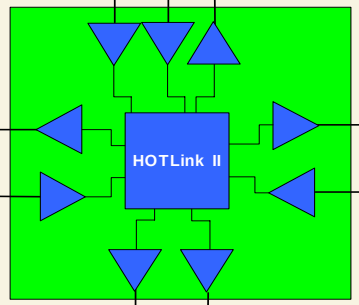
Channel A (1.485 Gbps):

-HD/SD Eye diagram

-Low Jitter



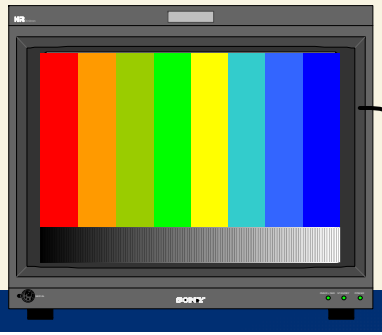


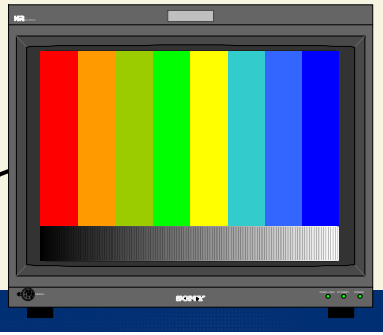


Channel C (1.485 Gbps and 270 Mbps):

-Selectable Inputs

- Auto rate-detect
- Reclocker
- HD support





Channel B (270 Mbps)

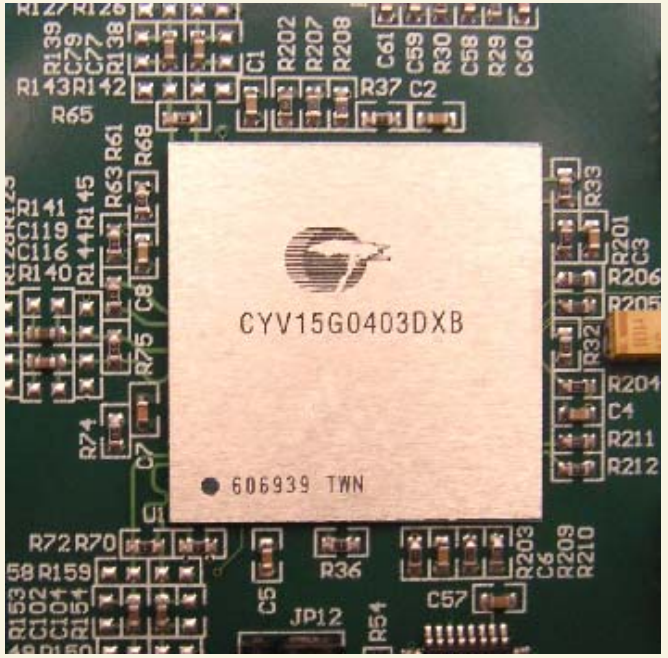
-Redundant Output

-SD support

-Power down control

Cypress Video Features Checklist

- Independent Channel Operation
- Broadcast Test Equipment Validated
- Integrated Transceiver Channels
- SMPTE Pathological Compliance
- High Ref Clock Input Tolerance
- Auto Rate-Detection
- Reclocker
- HD-SDI Support
- Selectable Inputs
- Interfaces to Common EQ/CD
- Per-Channel Power-Down
- SD-SDI Support
- Redundant Outputs
- SMPTE Jitter Compliance
- Low Power
- Cost Effective Solution
- Ease of Design



HOTLink-On-Demand Video Portfolio

Device	Device Function	Samples	Production
CYV15G0101DXB	1 Transceiver Channel	Now	Now
CYV15G0104TRB	1 Reclocking Deserializer + 1 Serializer	Now	Now
CYV15G0203TB	2 Independent Serializers	Now	October 2004
CYV15G0204RB	2 Independent Deserializing Reclockers	Now	October 2004
CYV15G0201DXB	2 Transceiver Channels	Now	Now
CYV15G0402DXB	4 Transceiver Channels (no DVB-ASI)	Now	Now
CYV15G0204TRB	2 Independent Reclocking Deserializers + 2 Independent Serializers	Now	Now
CYV15G0403TB	4 Independent Serializers	Now	October 2004
CYV15G0404RB	4 Independent Deserializing Reclockers	Now	October 2004
CYV15G0401DXB	4 Transceiver Channels	Now	Now
CYV15G0403DXB	4 Independent Transceiver Channels	Now	Now
CYV15G0404DXB	4 Independent Transceiver Channels w/ Reclocking Deserializers	Now	Now

Appendix

HOTLink-On-Demand Video Portfolio

Device	# Transmitters	# Receivers	Reclocker	8B/10B ENDEC	Independent Channels
CYV15G0101DXB	1	1		X	
CYV15G0104TRB	1	1	X		
CYV15G0203TB	2	0			X
CYV15G0204RB	0	2	X		X
CYV15G0201DXB	2	2		X	
CYV15G0402DXB	4	4			
CYV15G0204TRB	2	2	X		X
CYV15G0403TB	4	0			X
CYV15G0404RB	0	4	X		X
CYV15G0401DXB	4	4		X	
CYV15G0403DXB	4	4		X	X
CYV15G0404DXB	4	4	X	X	X

Part Number Decoder

What does “CYV15G0204TRB” mean?

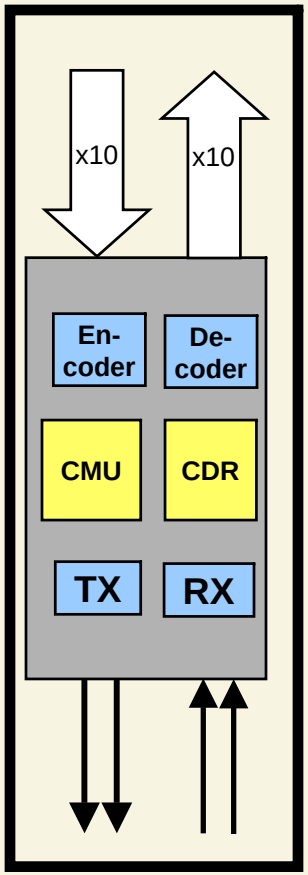
CY + V + 15G + 0x + 0x + xx + B

CY	V	15G	0x	0x	xx	B
Cypress Device	Video PHY	1.5Gbps Support	# of Channels	Device Function Rev	Device Integration	Silicon Rev

Device Function Rev:
01 – Original HOTLink II PHY
02 – Quad Port PHY only
03 – Independent Channel
04 – Independent Channel w/ Reclocking

Device Integration:
DX – Integrated Tx/Rx Channel
T – Transmit Only Channel
R – Receive Only Channel
TR – Independent Transmit and Receive Pairs

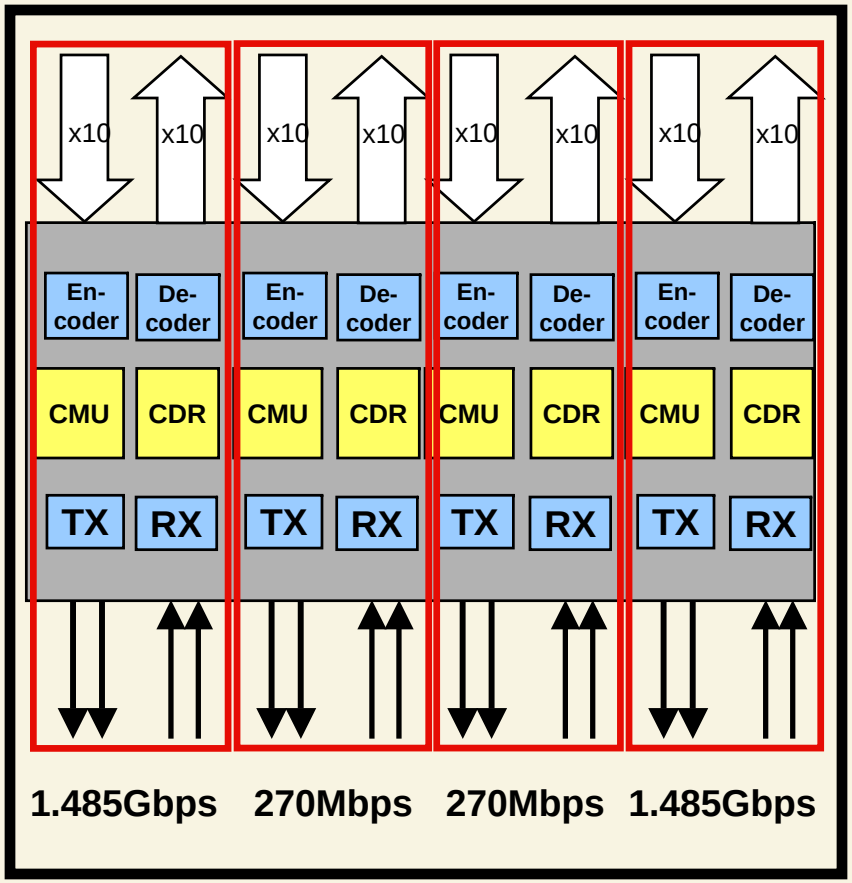
Original HOTLink II™ SERDES



x1 Block Diagram

- **4 Devices, 195Mbps-1.5Gbps**
- **Single, Dual, or Quad Channels**
- **Data rate locked across all channels**
- **Integrated Transmit & Receive Channels**
  - **3 Devices – 8B/10B ENDEC**
    - x1 – CYV15G0101DXB
    - x2 – CYV15G0201DXB
    - x4 – CYV15G0401DXB
  - **1 Device – no 8B/10B ENDEC**
    - x4 – CYV15G0402DXB

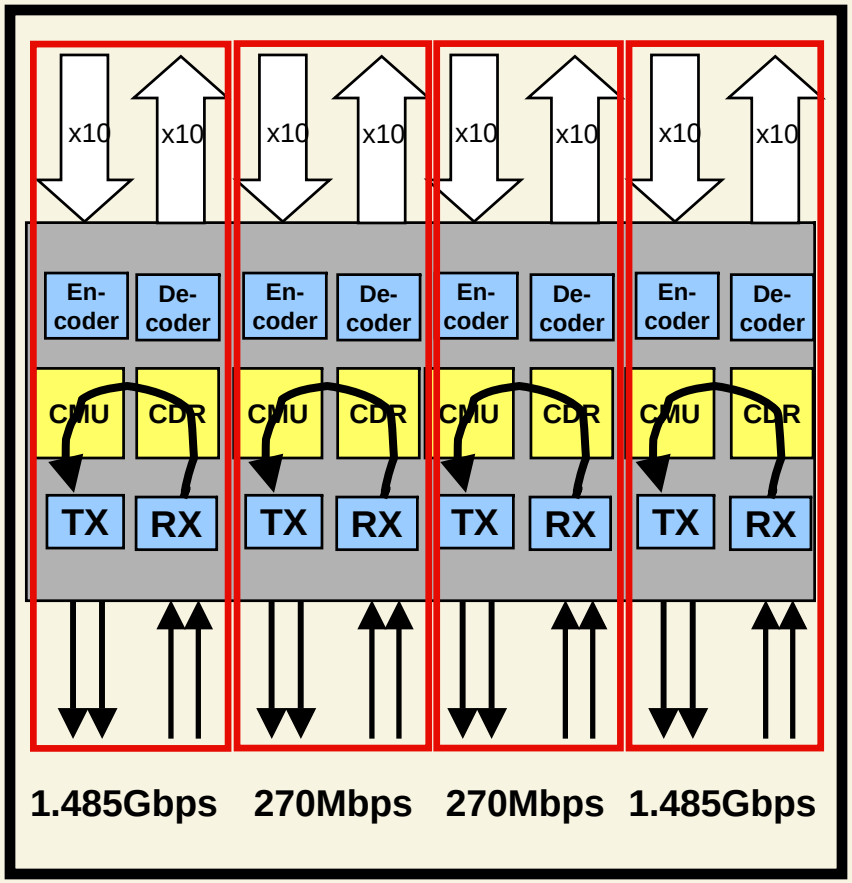
Independent Channel HOTLink II™ SERDES



CYV15G0403DXB Block Diagram

- **Four channels in single device**
- **Integrated Transmit & Receive on each channel**
- **Variable data rate across each channel**
- **Selectable 8B/10B ENDEC on each channel**

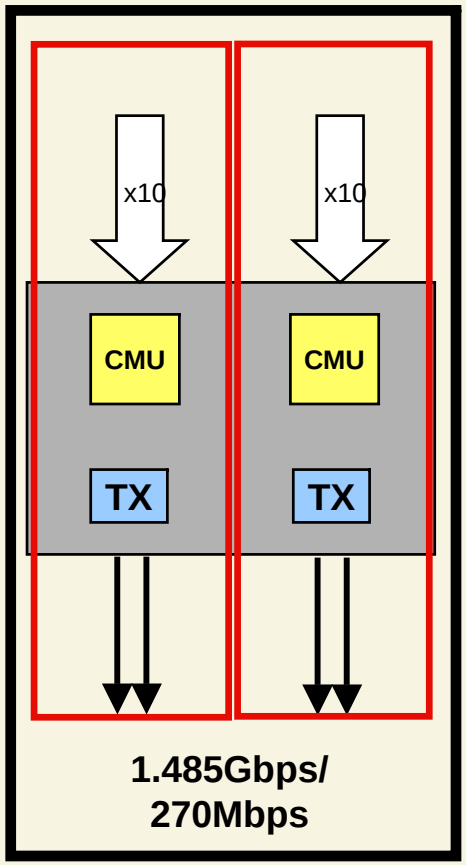
Independent Channel Reclocking HOTLink II™ SERDES



CYV15G0404DXB Block Diagram

- **Four channels in single device**
- **Integrated Transmit & Receive on each channel**
- **Variable data rate across each channel**
- **Selectable 8B/10B ENDEC on each channel**
- **Reclocking function on each channel – “Serial in, Serial Out”**

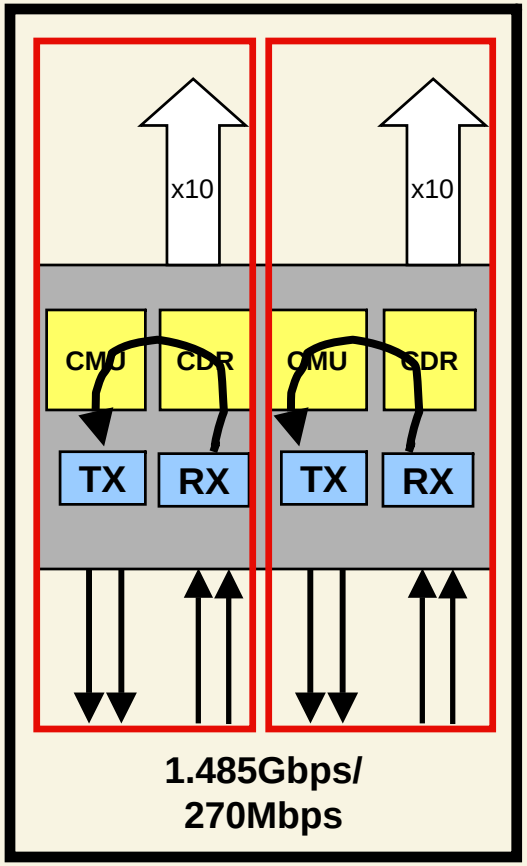
Independent Serializing HOTLink II™ PHY



x2 Block Diagram

- **Transmit-only Functionality**
- **Variable data rate across each channel**
- **Dual or Quad Channels**
  - x2 – CYV15G0203TB
  - x4 – CYV15G0403TB

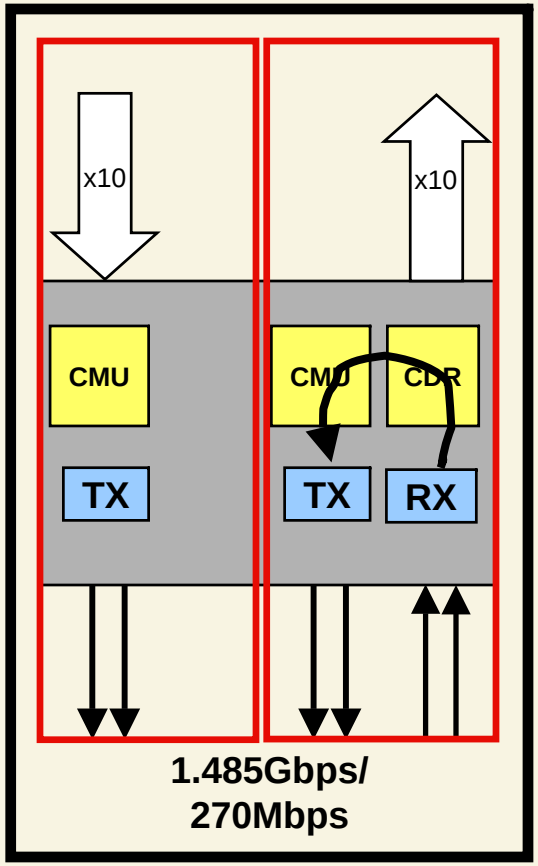
Independent Reclocking Deserializer HOTLink II™ PHY



x2 Block Diagram

- **Receive-only with Optional Reclocking Functionality**
- **Variable data rate across each channel**
- **Dual or Quad Channels**
  - x2 – CYV15G0204RB
  - x4 – CYV15G0404RB

Independent Serializer & Reclocking Deserializer HOTLink II™ PHY



x1 Pair Block Diagram

- **Transmit & Receive Pair operate independently**
- **Variable data rate across each function**
- **Single or Dual Pairs**
  - x1 – CYV15G0104TRB
  - x2 – CYV15G0204TRB