PRELIMINARY

Interfacing the HOTLink II™ Transceiver with the 3.3V Gennum GS1524 Equalizer and GS1528 Cable Driver for Digital Video

Introduction

The HOTLink II™ Transceiver is a point-to-point or point-to-multipoint communications building block allowing the transfer of data over high-speed serial links at signaling speeds ranging from 195 to 1500 MBaud. The device provides a selectable 8B/10B Encoder/Decoder and a Cypress Mode Multibyte Framer that may be used for DVB-ASI applications. The encoding, decoding and framing functions may be bypassed for SMPTE SDI transport.

Cable drivers are used in serial digital video systems to meet the 800mV signal amplitude requirements found in the SMPTE 259M, 292M and DVB-ASI specifications. Adaptive equalizers are used to reverse the eye-closing effects of frequency-dependent attenuation of copper interconnects. This application note explains how to interface the HOTLink II Transceiver to the Gennum GS1524 Adaptive Cable Equalizer and GS1528 Cable Driver for serial digital video applications over hundreds of meters of coaxial cable. All of the members of the HOTLink II video family, which includes the CYV15G0101DXB, CYV15G0201DXB, CYV15G0401-DXB, CYV15G0402DXB and CYV15G0403DXB, are compatible with Gennum's 3.3V cable driver and adaptive equalizer chipset.

The HOTLink II Video Evaluation Board uses the GS1524 and GS1528; the board was tested by transmitting SMPTE 259M data (SD-SDI) and DVB-ASI data over 300m of Belden 8281 coaxial cable. The results of these tests are discussed in the final section of this application note.

Block Diagrams

Figure 1 and *Figure 2* show the block diagram of the connection of CYV15G0101DXB (HOTLink II PHY), the GS1524 (Gennum adaptive equalizer) and the GS1528 (Gennum cable driver). Although a single-channel device is shown in these figures, the same format is applicable to any device in the HOTLink II family, including dual-channel and quad-channel devices.

Figure 1 shows the block diagram for a SMPTE system in which the HOTLink II device's 8B/10B Encoder, 10B/8B Decoder and Framer are disabled, and the SMPTE scrambling, descrambling and framing functions are provided by an external Cypress solution.

Figure 2 shows the block diagram for a DVB-ASI system in which the 8B/10B Encoder, 10B/8B Decoder and Cypress Mode Multi-byte Framer are enabled. The non-SMPTE "CYP" devices may also be used in DVB-ASI systems.

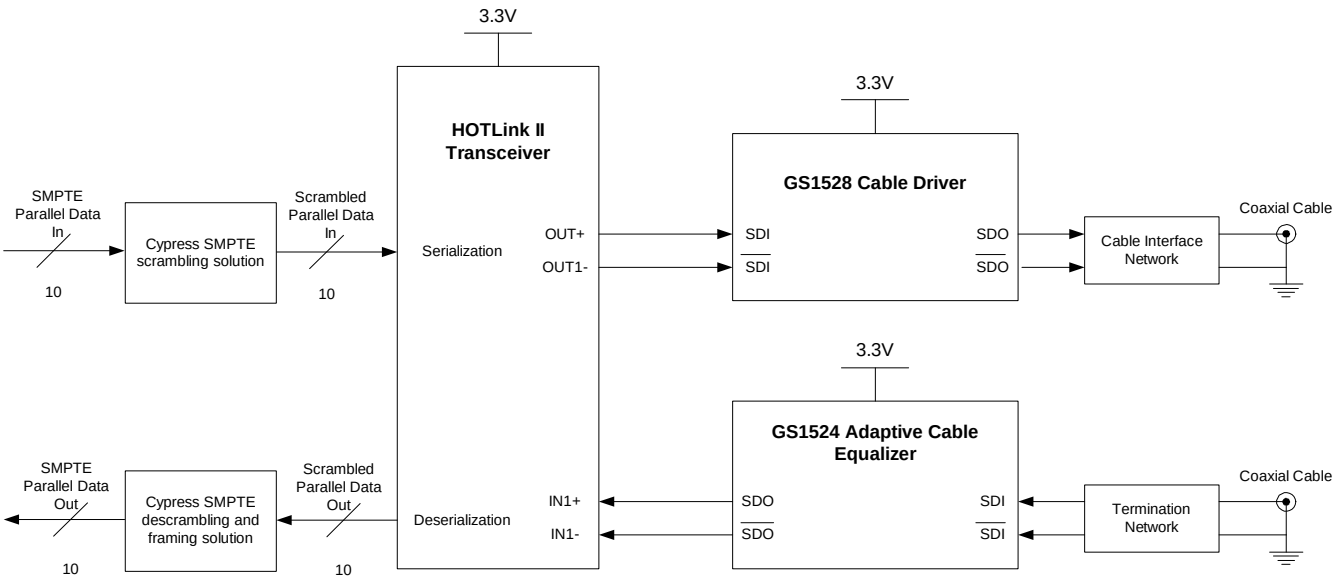

Figure 1. Typical Block Diagram of the Physical Layer in a SMPTE SDI Video System

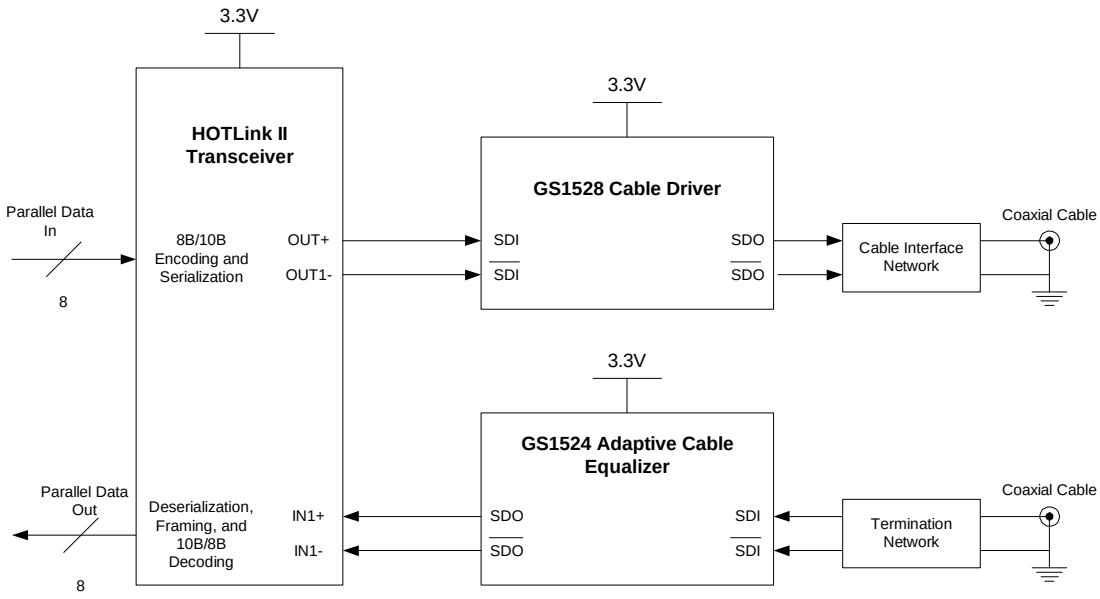

Figure 2. Typical Block Diagram of the Physical Layer in a DVB-ASI Video System

Schematic Diagrams

Figure 3 and *Figure 4* show the schematic connections between the HOTLink II device and the GS1524 and the GS1528. Because these are all 3.3V devices, they can be powered with a single supply.

Transmitting Data to the Coaxial Cable

For SMPTE video, 10-bit parallel data is sent from upstream logic. The HOTLink II device serializes the data and sends it to the GS1528 Cable Driver at bit rate 10 times that of the parallel word rate. Cypress also offers solutions for implementing the SD-SDI and HD-SDI scrambler for interface with the HOTLink II device.

For DVB-ASI video, 8-bit parallel data is sent from upstream logic at a rate of 27 MHz. The HOTLink II 8B/10B encoder must be enabled to transmit the associated 10-bit code word with correct disparity for each 8-bit input character or special character.

In all cases, the GS1528 provides the appropriate 800-mV amplitude swing at the signal outputs. Signals are coupled to the transmission line using capacitors. This is shown in *Figure 3*.

Design Considerations for the Interface Between the HOTLink II Device and the GS1528

At the high data rates used to transmit SMPTE 292M (HD-SDI) data, it is important to control the trace impedances to minimize distortions caused by reflections. The following practices are recommended to ensure signal integrity. The component names refer to those shown in *Figure 3*.

1. R2 should be placed as close as possible to the SDI inputs on the GS1528.
2. High speed traces should be curved to minimize impedance variations due to change of PCB trace width.

In addition to the recommendations listed here, Gennum specifies other guidelines in the GS1528 data sheet. The details provided by Gennum regarding board layout and the selection of R8, R10, L1, L2 and C5, C6 should also be considered when designing this system.

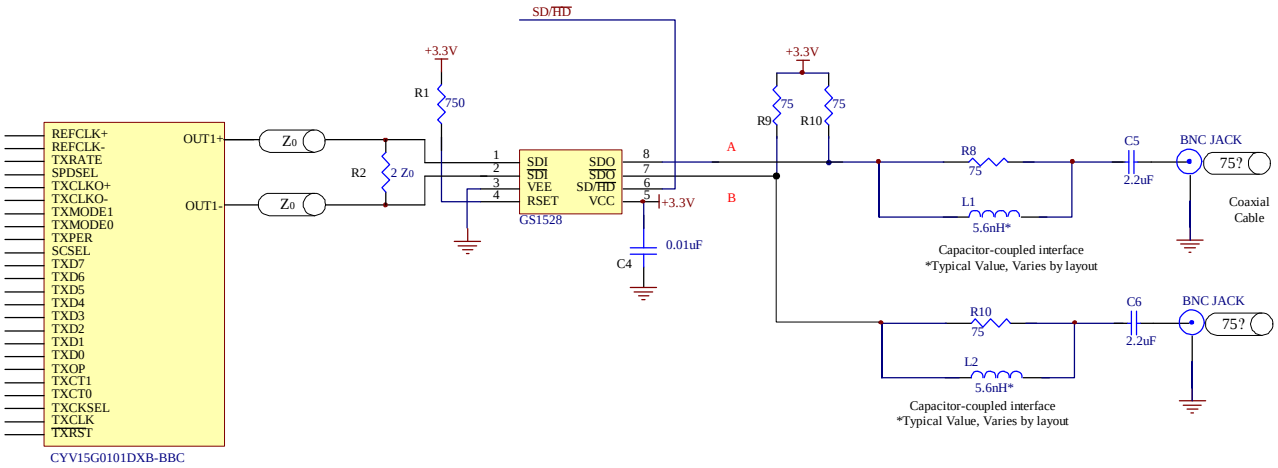

Figure 3. Schematic Diagram of the Connection of the Transmit Portion of the HOTLink II Transceiver with the GS1528 Cable Driver

Receiving Data from a Coaxial Cable

Serial data received from a coaxial cable is coupled to the GS1524 adaptive equalizer using an appropriate terminating and coupling network. As with the cable driver, the adaptive equalizer should be coupled to the transmission line using capacitors. This is shown in *Figure 4*.

The equalizer opens the eye by reversing the effects of the frequency-dependent attenuation of the copper link. This equalized differential signal is then presented to the serial inputs of the HOTLink II device.

For SMPTE SD-SDI and HD-SDI systems, the data is placed on the HOTLink II device's 10-bit receive bus, along with a recovered clock (RXCLK) operating at 27 MHz and 148.5 MHz (or 148.5/1.001 MHz), respectively. The received parallel data is then delivered to a descrambler/framer. Cypress offers a descrambling and framing solution for both SD-SDI and HD-SDI.

For DVB-ASI systems, the received data is framed, decoded and placed on the HOTLink II device's 8-bit receive bus along with a 27 MHz recovered clock. The deserialized data can also be clocked out with the local reference clock using the optional Elasticity Buffer in the HOTLink II receiver. When the Elasticity Buffer is enabled, K28.5 framing characters will be inserted or deleted to/from the datastream to absorb the frequency difference between the two clock domains (recovered clock and reference clock). The framing is implemented using the Cypress Mode Multibyte Framer, which frames on two instances of K28.5 having identical 10-bit boundaries in a space of 50 bits. This is optimized for DVB-ASI, which transmits two consecutive K28.5 characters between packets. The RXST[2:0] bus indicates the presence of valid data and framing characters. The upstream logic decodes the signal on this bus to remove K28.5 characters from the data stream. See the HOTLink II device's data sheet for the interpretation of the RXST[2:0] bus.

Design Considerations for the Interface Between the HOTLink II Device and the GS1524 Adaptive Equalizer

At the high data rates used to transmit SMPTE 292M (HD-SDI) data, it is important to control the trace impedances to minimize distortions caused by reflections. The following practices are recommended to optimize performance of the adaptive equalizer. The component names refer to those shown in *Figure 4*.

1. The traces connecting the HOTLink II inputs and equalizer outputs should have a uniform characteristic impedance of 50? or 75? . R18 should be twice the characteristic impedance of each line.
2. High speed traces are curved to minimize impedance changes.
3. The components C15-C16, R14-R16 and L2 should be as close as possible to the SDI inputs on the GS1524.

In addition to the recommendations listed here, Gennum specifies other guidelines in the GS1524 data sheet. The details provided by Gennum regarding board layout and the selection of R13, R14, R15, C15, C16 and L2 should also be considered when designing this system. Also, please refer to the schematics for the HOTLink II Video Evaluation board found in the *HOTLink II Video Evaluation Board User's Guide*.

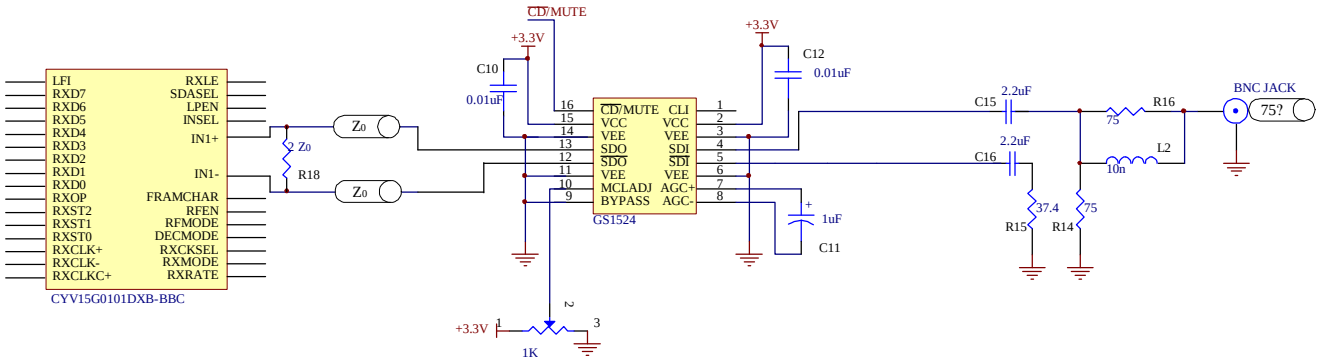

Figure 4. Schematic Diagram of the Connection of the Receiver Portion of the HOTLink II Transceiver with the GS1524 Adaptive Cable Equalizer

HOTLink II Video Evaluation Board Tests

The HOTLink II Video Evaluation Board supports digital video transmission at SD-SDI and DVB-ASI rates. The following tests were run to evaluate the board's performance for SMPTE 259M and DVB-ASI.

SMPTE SD-SDI pathological tests

The HOTLink II Video Evaluation board provides a test suite to check the serial pathological patterns defined in SMPTE EG-34. The first pathological condition could happen as often as once per scan line, so it was tested on each scan line. The two other pathological conditions typically occur on no more than one scan line per frame, so an occurrence rate of five lines per frame was tested for each of the pathological conditions as a stressing condition. Data was tested at the SD-SDI rate of 270 Mb/s. The setup is shown in *Figure 5*.

Pathological Serial Loopback Test 1: Runlength Test

The first pathological condition tests the run-length limit of the SMPTE scrambler. The scrambler is run-length limited to 44 consecutive bits of the same parity. In this test, every scan line contains a series of 44 bits without a transition. This data was driven over 300m of Belden 8281 coaxial cable for 1 hour, 45 minutes without a single bit error. A screen shot showing the Bit Error Rate (BER) and the elapsed time of the test is shown in *Figure 6*.

Pathological Serial Loopback Test 2: Equalizer Test

The second pathological condition tests the equalizer. Under the conditions specified in EG 34, the scrambler can output a scan line consisting of a repeating pattern of 19 bits of one parity followed by 1 bit of the opposite parity (19 1's followed by a 0, or 19 0's followed by a 1). In this test, five lines per frame consisted of this pathological condition. The data was driven over 300m of Belden 8281 coaxial cable for 1 hour, 45 minutes without a single bit error.

Pathological Serial Loopback Test 3: PLL Test

The third pathological condition tests the clock recovery Phase Locked Loop of the serial receiver, located in the CYV15G0101DXB. Under the conditions specified in EG 34, the scrambler can output a scan line consisting of a repeating pattern of 20 bits of one parity followed by 20 bits of the opposite parity (20 highs followed by 20 lows). This pattern is used to test the performance of the CDR PLL and its ability to maintain lock for long periods of data with a low transition density. The data was driven over 300m of Belden 8281 coaxial cable for 1 hour, 45 minutes without a single bit error.

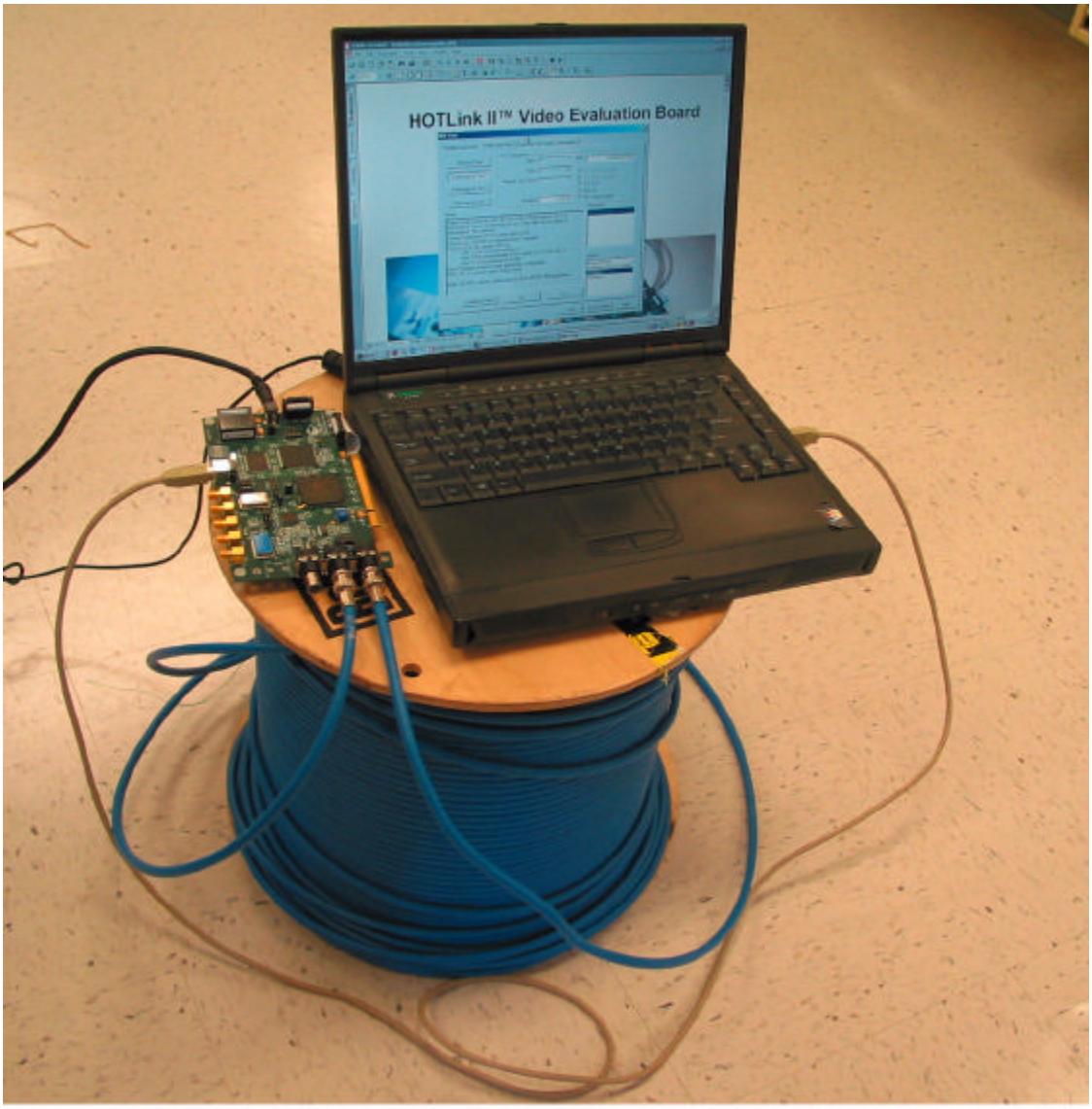

Figure 5. HOTLink II Video Evaluation Board Driving 300 m of Belden 8281 Cable

DVB-ASI Link Tests

In this test, two HOTLink II Video Evaluation Boards were used to test the functionality of a DVB-ASI link. A Linear Systems DVB Master board[1] was used to transmit and test DVB-ASI data. The HOTLink II video evaluation boards were placed in DVB-ASI Parallel Loopback mode, and the data was transmitted over 300m of Belden 8281 cable. The signaling rate was 270 Mbaud, of which 150 Mb/s consisted of actual data packets. The rest of the bandwidth was taken up by K28.5 framing and stuffing characters.The test was run for 90 minutes, and over that time the link had no errors. The set-up is show in *Figure 7*.

Note:
1. See <http://www.linsys.ca/products/hardware/DVB%20Full%20Duplex.htm>.

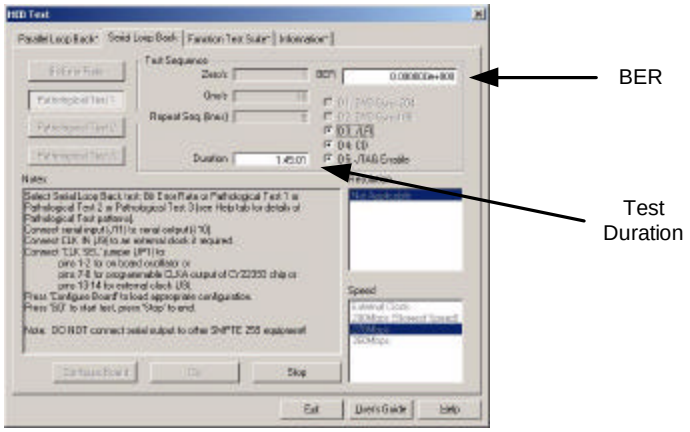

Figure 6. User Interface Showing Results of Run-Length Pathological Test

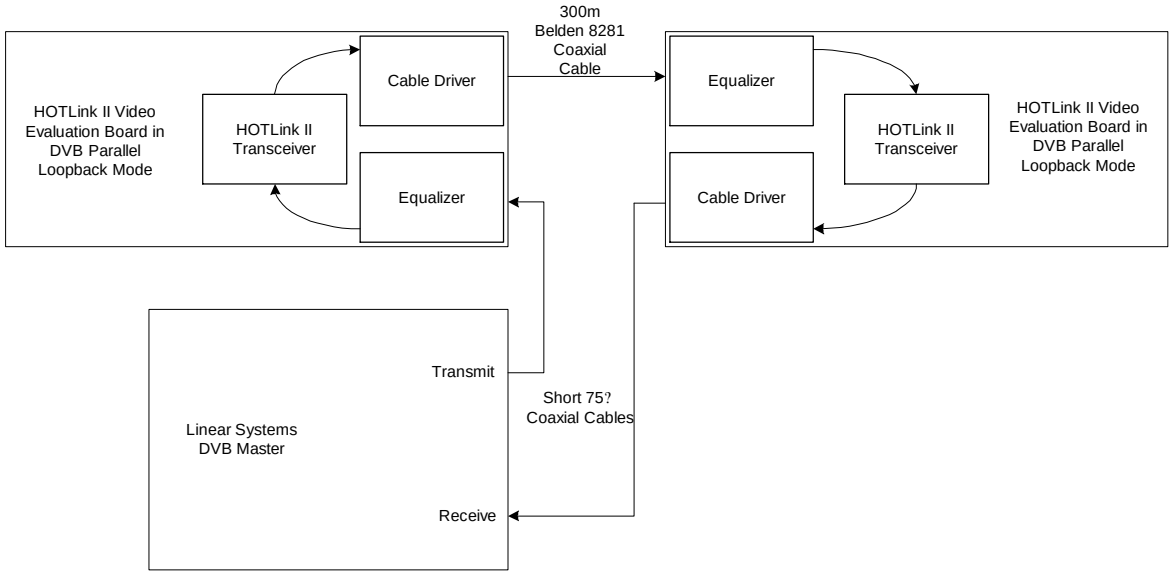

Figure 7. DVB-ASI Link Test

Conclusion

Cypress Semiconductor's HOTLink II family of video physical layer devices is able to interface with the Gennum GS1524/GS1528 Cable Driver and Adaptive Equalizer chipset. This interface was shown to work while driving SMPTE EG 34 pathological signals over 300 m of Belden 8281 coaxial cable. This interface was also tested for a DVB-ASI application using 300m of Belden 8281 cable. Therefore, the HOTLink II device, which can interface to the Gennum Cable Driver and Equalizer, is a proven solution for SMPTE SDI and DVB-ASI serial digital video links over copper.

References

1. *CYP(V)15G0101DXB Single-Channel HOTLink II Transceiver*, data sheet, Cypress Semiconductor, 2003.
2. *GS1528 HD-LINX™ II Multi-Rate SDI Dual Slew-Rate Cable Driver*, data sheet, Gennum Corporation, 2002.
3. *GS1524 HD-LINX™ II Multi-Rate SDI Adaptive Cable Equalizer*, data sheet, Gennum Corporation, 2003.
4. *Implement SMPTE 259M Using the CY7C9235/ CY7C9335*, application note, Cypress Semiconductor,1999.
5. Implementing DVB-ASI Serial Interfaces Using HOTLink? application note, Cypress Semiconductor, 2002
6. *EG 34-1999 Pathological Conditions in Serial Digital Video Systems*, SMPTE Engineering Guideline, Society of Motion Picture and Television Engineers, 1999

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