CW25-NAV

NAVSYNC

Contents

Figure and Table Contents

List of Figures

List of Tables

Revision History of Version 2.0

Revision	Date	Released By	Note
2	7/11/2003	Calum Dalmeny	New version reflecting size and pinout changes
3	10/11/2003	Calum Dalmeny	Add improved footprint and dimension diagrams
4	23/02/04	Calum Dalmeny	Add updated graphics and logo's.
5	10/11/04	Calum Dalmeny	Updated Specifictions

Table 1 Revision History

Other Documentation

The following additional documentation may be of use in understanding this document.

Document	By	Note
RF25IC Data Sheet	Navsync	
BB25IC Data Sheet	Navsync	
CW25 User Manual	Navsync	

Table 2 Additional Documentation List

1 INTRODUCTION

The CW25-NAV is a small size GPS OEM module that has been specifically designed for use in weak signal GPS environments and for rapid integration into host systems, while maintaining all the features of a standard GPS solution, such as high accuracy.

Normal GPS systems cannot track satellites below -175 dBW (-145 dBm) however the CW25-NAV can track down a further 10 dB resulting in tracking down to -185 dBW (-155 dBm). This makes it possible to track the person, asset or vehicle as they enter buildings, move under dense vegetation, or drive through dense urban canyons. The CW25-ULS GPS model can also acquire the satellites in these locations when using Network Assistance techniques, or pre-loaded information. In order to obtain this level of performance the CW25-NAV uses an innovative GPS engine built into its BB25IC, which enables the system to search in parallel 12288 time/frequency bins. Not only does this enable better sensitivity but also makes for very rapid acquisition of the satellites. At outdoor signal levels the time taken to obtain a 'hot' position fix is under 2 seconds.

With a size of just over an inch square (25 x 27 mm) and provided as a tape and reel component, the CW25-NAV is specifically designed to be integrated with Communications devices such as GSM, CDMA, UMTS modems or any other communications medium. The CW25-TIM is optimised for the output of time/ frequency information. Another aid to integration is the ability to store users' software code in the CW25-NAV, reducing the need for external memory and processors.

Key Features of the CW25-NAV include:

- Enables indoor use
  - -173 dBW acquisition and -185 dBW tracking
- Rapid Time To Fix
  - <2 second outdoors
- Standalone CW25-NAV module
  - No GPS knowledge required for hardware integration
- 25 mm x 27 mm x 4.2 mm

This document, the **CW25-NAV Data Sheet**, provides information on the **Hardware Elements of the CW25-NAV.**

Key information includes:

- System Block Diagram
- Maximum Ratings
- Physical Characteristics
  - CW25-NAV Dimensions, castellation information
  - Solder Pad and placement information
- Signal Descriptions
- Special Features
- Application Information
  - Power supply modes
  - RF connections
  - Grounding
  - Battery Back-up
  - Over Voltage and Reverse Polarity
  - LED's

The specifications in the following sections refer to the standard software builds of the CW25-NAV. The performance and specification of the CW-25NAV can be modified with the use of customized software builds.

2 SPECIFICATION

2.1 Performance

CW25-NAV GPS RECEIVER SPECIFICATIONS[1]

Physical	Module dimensions	25mm (D) x 27mm (W) x 4.2mm (H)
	Supply voltages	3V3 (Digital I/O), 3V3 (RF), 1V8 (Core option), 3V (Standby Battery)
	Operating Temp Range	0 to 70°C (standard) -40°C to 85°C (available as options)
	Storage Temp Range	-55 to 125°C
	Humidity	5% to 95% non-condensing
	Max Velocity / Altitude	515ms^{-1} / 18,000m (increased rating version available subject to export license)
	Max Acceleration / Jerk	4g / 1gs^{-1} (sustained for less than 5 seconds)
Sensitivity	Acquisition/Tracking	173dBW / -185dBW
	Stand Alone (Outdoor)	Cold: <60s Warm: <45s Hot: <2s Re-acquisition: <0.5s (90%confidence)
Accuracy	Position: Outdoor / Indoor	<5m rms / <50m rms
	Velocity	<0.05ms-1
	Latency	<200ms
	Raw Measurement Accuracy	Pseudorange <0.3m rms, Carrier phase <5mm rms
	Tracking	Code and carrier coherent
Power	1 fix per second	0.22W typically (1)
	Sleep/Standby Current	5mA/1µA
Interfaces	Serial	3 ports, CMOS levels; USB v1.1
	Multi function I/O	1PPS and Frequency Output Event Counter/Timer Input 4 x GPIO (multi-function) 2 x LED Status Drive I2C, External Clock (on special build)
	Protocols	NMEA 0183, Proprietary ASCII and binary message formats
	1pps Timing Output	30ns rms accuracy, <5ns resolution User selectable pulse width
	Event Input	30ns rms accuracy, <10ns resolution
	Frequency Output	10Hz to 10MHz
	Receiver Type	12 parallel channel x 32 taps up to 32 point FFT. Channels, taps and FFT can be switched off to minimise power or simulate simpler designs.
General	Processor	ARM 966E-S on a 0.18µ process at up to 120MHz.
	User Memory	64K loaded from 24K on module EEPROM or external EEPROM.

Table 3 CW25-NAV Specification

Footnotes

This value is based on a software build which has all peripherals powered. For applications where power consumption is an issue some of these may be turned off to provide a saving in this area.

2.2 Recommended Ratings

Symbol	Parameter	Min	Max	Units
RF_3V3	RF Supply Voltage	+2.9	+3.5	Volts
DIG_3V3	Digital Supply Voltage	+2.9	+3.5	Volts
DIG_1V8	Digital Supply Voltage	+1.71	+1.89	Volts
VBATT	Battery Backup Voltage	+2.7	+3.5	Volts
ANT_SUPPLY	Antenna Supply Voltage	+3.0	+12	Volts

Table 4 Absolute Maximum Ratings

2.3 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
RF_3V3	RF Supply Voltage	-0.3	+6.5	Volts
DIG_1V8	Digital Supply Voltage	-0.3	+2.0	Volts
DIG_3V3	Digital Supply Voltage	-0.3	+3.7	Volts
VBATT	Battery Backup Voltage	-0.5	+7.0	Volts
ANT_SUPPLY	Antenna Supply Voltage	-15	+15	Volts
DIG_SIG_IN	Any Digital Input Signal	-0.3	+5.5	Volts
RF_IN	RF Input	-15	+15	Volts
TSTORE	Storage temperature	-55	+150	°C
TBIAS	Temperature under bias	-40	+100	°C
IOUT	Digital Signal Output Current	-6	+6	mA

Table 5 Absolute Maximum Ratings

2.4 Block Diagram

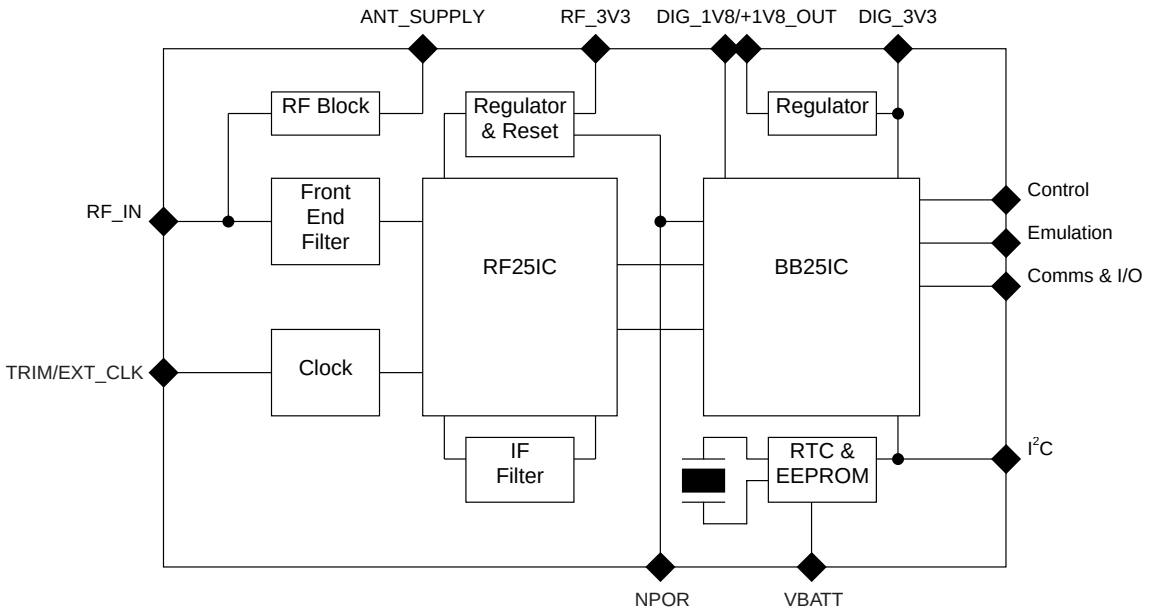

Figure 1 CW25-NAV Block Diagram

3 PHYSICAL CHARACTERISTICS

The CW25-NAV is a multi-chip module built on an FR4 fibreglass PCB. All digital and power connections to the CW25-NAV are via castellations on the 25 x 27 mm PCB. The RF connection is via castellations or an RF connector. The general arrangement of the CW25-NAV is shown in the diagram below. Dimensions in mm (inches/1000).

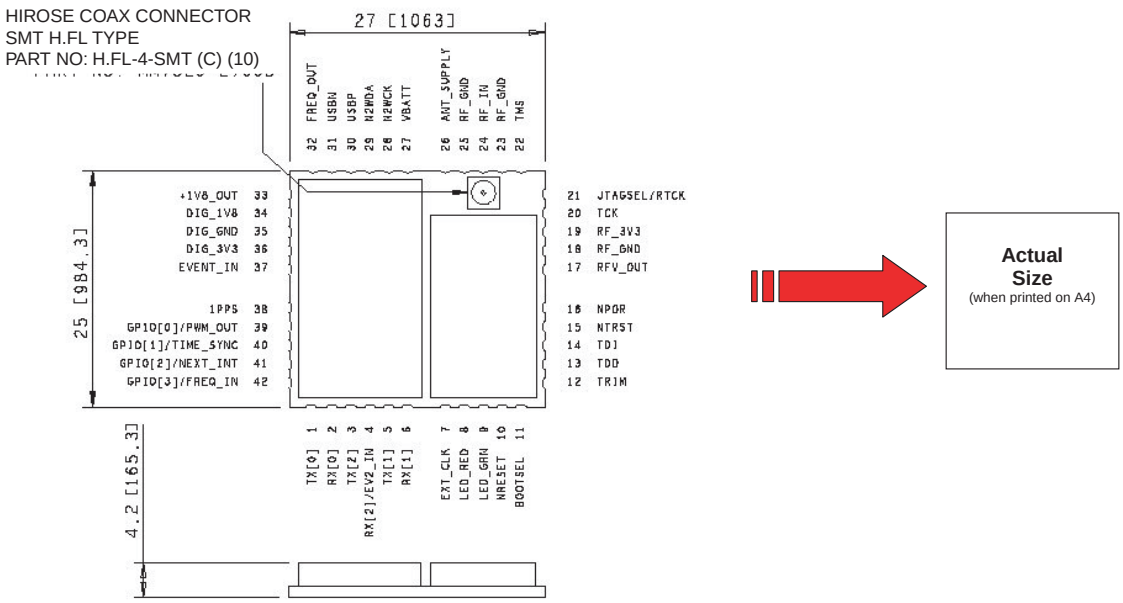

Figure 2 CW25-NAV Form and Size

3.1 Physical Interface Details

The interface to the CW25-NAV is via 1mm castellations on a 2mm pitch. There are 42 connections in all. There is also an RF connector for connecting to the GPS antenna. The details of the interface connections are given below.

Pin	Function	Pin	Function	Pin	Function
1	TX[0]	15	NTRST	29	N2WDA
2	RX[0]	16	NPOR	30	USBP
3	TX[2]	17	RFV_OUT	31	USBN
4	RX[2]/EV2_IN	18	RF_GND	32	FREQ_OUT
5	TX[1]	19	RF_3V3	33	+1V8_OUT
6	RX[1]	20	TCK	34	DIG_1V8
7	EXT_CLK	21	JTAGSEL/RTCK	35	DIG_GND
8	LED_RED	22	TMS	36	DIG_3V3
9	LED_GRN	23	RF_GND	37	EVENT_IN
10	NRESET	24	RF_IN	38	1PPS
11	BOOTSEL	25	RF_GND	39	GPIO[0]/PWM_OUT
12	TRIM	26	ANT_SUPPLY	40	GPIO[1]/TIME_SYNC
13	TDO	27	VBATT	41	GPIO[2]/NEXT_INT
14	TDI	28	N2WCK	42	GPIO[3]/FREQ_IN

Table 6 CW25-NAV Signal List

3.2 CW25-NAV Dimensions

The figure below provides the dimensions of the positioning of the CW25-NAV castellations. Dimensions in mm (inches/1000).

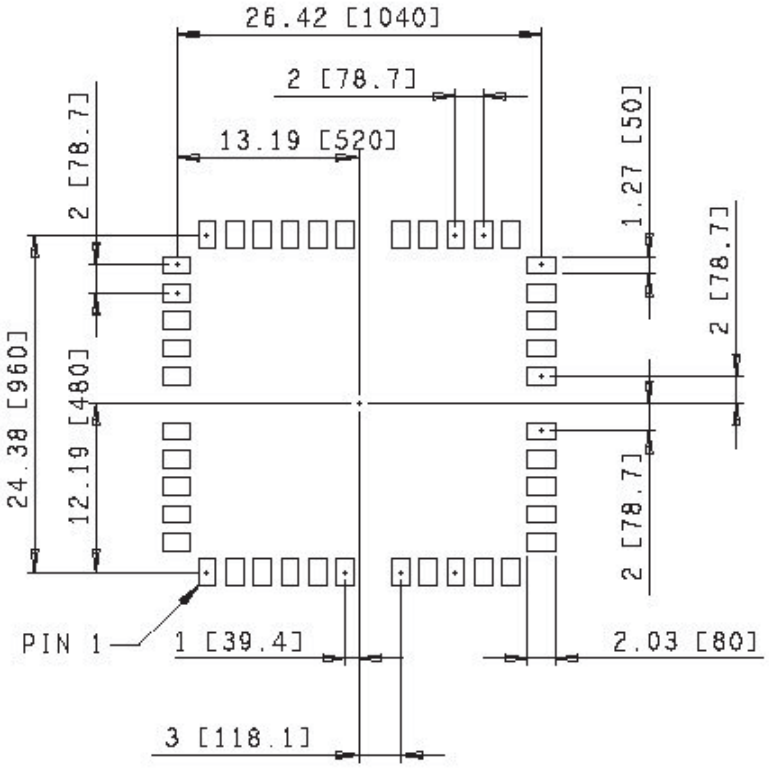

Figure 3 CW25-NAV Dimensions

3.3 Solder Pad Size and Placement

It is recommended that the footprint of the solder pad under each castellation be 2mm x 1mm, centred on the nominal centre point of the radius of the castellation. The castellations are gold plated and so are lead free. Note that if the RF_IN connector is being used, there should not be a pad or solder resist under the RF_IN castellation. If the RF_IN castellation is to be used, the pad should be shortened by 0.5mm underneath the CW25-NAV and standard RF design practices must be observed. The diagram below shows the placement of the pads under the castellations.

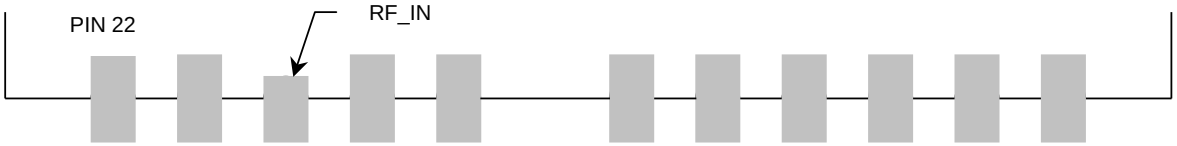

Figure 4 Solder Pad Size and Placement

4 SIGNAL DESCRIPTION

The signals on the CW25-NAV are described in the table below.

4.1 Power Signals

RF_3V3	**Type: Power**	**Direction: Input**	**Pin: 19**
	The RF supply input. This 3.3V ± 10% input supplies the 2.9V LDO regulator in the RF section of the CW25-NAV. It is important that this supply is well filtered with no more that 50mV peak to peak noise with respect to RF_GND.		
RF_GND	**Type: Power**	**Direction: Input/Output**	**Pins: 18, 23, 25**
	The RF input ground. This is the return path for the RF_3V3 supply and the ground for the antenna feed. The RF_GND must be tied to the DIG_GND externally to the CW25-NAV.		
RFV_OUT	**Type: Power**	**Direction: Output**	**Pin: 17**
	The output from the LDO regulator that is powered by the RF_3V3 signal. This supplies the power to the RF subsystem of the CW25-NAV. This may also be used to power external RF components but care must be taken not to inject noise onto this signal. No more than an additional 30mA may be taken from this signal by external circuitry. ANT_SUPPLY		
Type: Power	**Direction: Input**	**Pin: 26**	
	The antenna supply voltage. This may be used to supply power to the RF_IN signal, for use by an active antenna. The maximum voltage should not exceed ±15V and the current should be limited to 50mA.		
DIG_3V3	**Type: Power**	**Direction: Input**	**Pin: 36**
	The digital supply input. This 3.3V ± 10% input supplies the I/O ring of the BB25IC chip and the LDO regulator in the digital section of the CW25-NAV. It is important that this supply is well filtered with no more that 50mV peak to peak noise with respect to DIG_GND.		
DIG_1V8	**Type: Power**	**Direction: Input**	**Pin: 34**
	The 1.8V ± 5% digital core supply for the BB25IC. This is normally connected directly to the +1V8_OUT signal. However, if an external 1.8V ± 52% is available, a lower overall system power consumption may be achieved by using an external supply.		
+1V8_OUT	**Type: Power**	**Direction: Output**	**Pin: 33**
	The 1.8V output from the LDO regulator that is powered by the DIG_3V3 signal. Normally, this is connected to the DIG_1V8 signal. This may also be used to power external logic but care must be taken not to inject noise onto this signal. No more than an additional 50mA may be taken from this signal by external logic.		
DIG_GND	**Type: Power**	**Direction: Input/Output**	**Pin: 35**
	The digital ground. This is the return path for the DIG_3V3 supply and the ground reference for all the digital I/O. The DIG_GND must be tied to the RF_GND externally to the CW25-NAV.		

4 SIGNAL DESCRIPTION continued

4.1 Power Signals cont'd

VBATT	Type: Power	Direction: Input/Output	Pin: 27
	The battery backup supply. The CW25-NAV has an on board Real Time Clock (RTC). This is powered from the VBATT signal. A supply of typically 3v (greater than 2.5V and less than DIG_3V3) should be applied to this signal. This signal can be left floating if not required. The input has a blocking diode and so rechargeable batteries will need an external charging circuit. Typically, a 1K resister in series with this signal and the external battery will provide an easy method of measuring the current consumption from VBATT during test.		

4.2 RF Signals

RF_IN	Type: RF	Direction: Input	Pin: 24
	The RF input signal. This attaches to the GPS antenna. Standard RF design rules must be used when tracking to this signal. This signal has an RF blocked connection to the ANT_SUPPLY signal. This is the same signal presented on the RF connector on the CW25-NAV. Only one antenna connection should be made. If the RF connector is to be used, then there should be no connection, even an unconnected pad, to this castellation.		

TRIM	Type: RF	Direction: Input	Pin: 12
	This signal trims the output frequency of the VCTCXO. This signal is normally left open. When floating, this signal is biased to the control voltage of the VCTCXO. Any noise injected into this signal will severely compromise the performance of the CW25-NAV. This signal should only be used in conjunction with specific application notes.		

EXT_CLK	Type: RF	Direction: Input	Pin: 7
	This signal normally has no internal connection in the CW25-NAV. In special builds of the CW25-NAV that are not fitted with an internal VCTCXO, this input is the external clock input. The external clock is a 9MHz to 26MHz clipped sign wave input with an amplitude between 1V and 3V peak to peak. The return path for this signal is RF_GND.		

4.3 Emulation/Test Signals

TDI	Type: Test	Direction: Input	Pin: 14
	The Test Data In signal. This is the standard JTAG test data input. The signal return path is DIG_GND.		

TDO	Type: Test	Direction: Output	Pin: 13
	The Test Data Out signal. This is the standard JTAG test data output. The signal return path is DIG_GND.		

4.3 Power Signals cont'd

TCK	**Type: Test**	**Direction: Input**	**Pin: 20**
	The Test Clock signal. This is the standard JTAG test clock input. The signal return path is DIG_GND.		

TMS	**Type: Test**	**Direction: Input**	**Pin: 22**
	The Test Mode Select signal. This is the standard JTAG test mode input. The signal return path is DIG_GND.		

JTAGSEL/RTCK	**Type: Test**	**Direction: Input/Output**	**Pin: 21**
	This is a dual function signal. When the NPOR signal is asserted (low), this signal is an input and selects the function of the JTAG interface. When high, JTAG emulation into the embedded ARM9 processor is selected. When low, the BB25IC chip boundary scan mode is selected. The value on this signal is latched when NPOR de-asserts (goes high). When NPOR is de-asserted (high) and the JTAG emulation mode has been latched, this signal provides the return clock to the ARM Multi-ICE. Because the ARM9 functions off a single clock domain, the TCK has to be internally synchronised in the ARM9. This can cause a variable length delay in the validity of the TDO signal. The RTCK is a synchronised version of the TCK signal. The Multi-ICE uses the RTCK output signal to indicate when the TDO signal is valid. The signal return path is DIG_GND.		

NTRST	**Type: Test**	**Direction: Input**	**Pin: 15**
	The Test Reset signal. This is the active low JTAG test reset signal. The signal return path is DIG_GND.		

4.4 Control Signals

NPOR	**Type: Control**	**Direction: Input/Output**	**Pin: 16**
	The Power On Reset signal. This active low, open collector signal is the master reset for the CW25-NAV. The CW25-NAV can be held in reset by asserting this signal. The signal can be used to reset external circuitry, but care must be taken to ensure no DC current is drawn from this signal as the internal pull-up resistor value is 100K.		

NRESET	**Type: Control**	**Direction: Input/Output**	**Pin: 10**
	The system reset signal. This active low, open collector signal is generated by the BB25IC chip in response to the assertion of the NPOR. It may also be driven to reset the ARM9 processor in the BB25IC without completely re-initialising the chip.		

BOOTSEL	**Type: Control**	**Direction: Input**	**Pin: 11**
	The boot select signal. The BB25IC has four boot up modes, but only two are supported by the CW25-NAV. This signal is sampled when the NPOR is de-asserted. If the BOOTSEL signal is high or left floating, then the CW25-NAV boots from its on-chip FLASH memory. If the BOOTSEL signal is pulled low, the CW25-NAV boots from its on-chip ROM.		

4.5 I/O Signals

TX[0]	**Type: I/O**	**Direction: Output**	**Pin: 1**
The transmit signal for UART 0. This is a standard UART output signal. The signal return path is DIG_GND.			
TX[1]	**Type: I/O**	**Direction: Output**	**Pin: 5**
The transmit signal for UART 1. This is a standard UART output signal. The signal return path is DIG_GND.			
TX[2]	**Type: I/O**	**Direction: Output**	**Pin: 3**
The transmit signal for UART 2. This is a standard UART output signal. The signal return path is DIG_GND.			
RX[0]	**Type: I/O**	**Direction: Input**	**Pin: 2**
The receive signal for UART 0. This is a standard UART input signal. The signal return path is DIG_GND.			
RX[1]	**Type: I/O**	**Direction: Input**	**Pin: 6**
The receive signal for UART 1. This is a standard UART input signal. The signal return path is DIG_GND.			
RX[2]/EV2_IN	**Type: I/O**	**Direction: Input**	**Pin: 4**
This is a dual mode signal. Normally, this is the receive signal for UART 2, a standard UART receive signal. Under software control, it can also be used as general purpose I/O or to detect events. It can be used to detect the timing of the leading edge of the start bit of the incoming data stream. The signal return path is DIG_GND.			
FREQ_OUT	**Type: I/O**	**Direction: Input/Output**	**Pin: 32**
The frequency output signal. This is a complex signal which under software can provide any of either an NCO generated output frequency, a PWM signal, a GPS aligned EPOCH pulse or general purpose I/O signal. The signal return path is DIG_GND.			
1PPS	**Type: I/O**	**Direction: Input/Output**	**Pin: 38**
The 1 pulse per second signal. This is normally a 1 pulse aligned with GPS time, but can under software control also provide general purpose I/O or an additional even input. The pulse width of the 1PPS is software selectable with a default of 100µs. The signal return path is DIG_GND.			
EVENT_IN	**Type: I/O**	**Direction: Input/Output**	**Pin: 37**
The event input signal. This is normally an event timer or counter. Events are timed against GPS time. Under software control, this input can be used as an external 48MHz input for the USB interface or this input can also be used for general purpose I/O. The signal return path is DIG_GND.Figure 6 Grounding			

N2WCK	**Type: I/O**	**Direction: Input/Output**	**Pin: 28**
	The Navsync 2 Wire Clock signal. This is the open collector I2C compatible clock signal for the 2 wire serial interface. The signal return path is DIG_GND.		
N2WDA	**Type: I/O**	**Direction: Input/Output**	**Pin: 29**
	The Navsync 2 Wire Data signal. This is the open collector I2C compatible data signal for the 2 wire serial interface. The signal return path is DIG_GND.		
USBP	**Type: I/O**	**Direction: Input/Output**	**Pin: 30**
	The positive USB signal. The signal return path is DIG_GND.		
USBN	**Type: I/O**	**Direction: Input/Output**	**Pin: 31**
	The negative USB signal. The signal return path is DIG_GND.		
LED_RED	**Type: I/O**	**Direction: Output**	**Pin: 8**
	This is a dual function signal. Normally this signal is used to drive a red LED. Standard software builds use this signal to indicate GPS status. In special software builds, this signal can be used as GPIO. This signal has a 3.3V CMOS drive. A series limiting resistor is required to limit output current to ±5mA. The signal return path is DIG_GND.		
LED_GRN	**Type: I/O**	**Direction: Output**	**Pin: 9**
	This is a dual function signal. Normally this signal is used to drive a green LED. Standard software builds use this signal to indicate GPS status. In special software builds, this signal can be used as GPIO. This signal has a 3.3V CMOS drive. A series limiting resistor is required to limit output current to ±5mA. The signal return path is DIG_GND.		
GPIO[0]/PWM	**Type: I/O**	**Direction: Input/Output**	**Pin: 39**
	The GPIO[0] signal. Primarily for general purpose I/O, this signal can also be programmed to provide either a frequency, PWM or EPOCH output. It can also be configured to form and external RC oscillator in combination with GPIO[3]. The signal return path is DIG_GND.		
GPIO[1]/TIME_SYNC	**Type: I/ODirection: Input/Output**		**Pin: 40**
	The GPIO[1] signal. Primarily for general purpose I/O, this signal can also be programmed to provide either an additional PPS output or a time synchronisation input to the GPS engine in the BB25IC chip. The synchronisation pulse can be provided from an external source or can be generated by the on-board RTC. When generated by the onboard RTC, the synchronisation signal can be observed on this pin signal. The signal return path is DIG_GND.		
GPIO[2]/NEXT_INT	**Type: I/O**	**Direction: Input/Output**	**Pin: 41**
	The GPIO[2] signal. Primarily for general purpose I/O, this signal can also be programmed to provide an interrupt event from an active low external input. The signal return path is DIG_GND.		

4.5 I/O Signals cont'd

GPIO[3]/FREQ_IN	Type: I/O	Direction: Input/Output	Pin: 42
	The GPIO[3] signal. Primarily for general purpose I/O, this signal can also be programmed to provide a frequency counter input. The frequency counter input has a Schmitt trigger and if used with GPIO[0] can be configured to form a temperature controlled oscillator. The signal return path is DIG_GND.		

5 SPECIAL FEATURES

While most of the features on the CW25-NAV are just a subset of the capabilities of the BB25IC and so are described in the BB25IC Data Sheet and the BB25IC User Manual, there are some additional features buried in the CW25-NAV that need specific explanation, especially if use is to be made of them by user application code.

5.1 Power on Reset

The power on reset for the CW25-NAV is generated on-board by the regulator in the RF section from the RF_3V3 signal. The RF_3V3 signal must be applied to the CW25-NAV at the same time as the DIG_3V3, if the on-board power on reset is to be used. If an external source of reset is to be applied to the NPOR signal after both the RF_3V3 and the DIG_3V3 signals are valid, this restriction does not apply.

5.2 Time Transfer

In order to aid time transfer between fixes during which the CW25-NAV has been unable to maintain an accurate perception of time (eg. in deep sleep or powered down states), the on-board RTC can be set to provide a signal derived from the 32.768Hz crystal.

5.3 CW25-NAV Embedded Identification

The hardware version number is hard coded onto the CW25-NAV; firmware also contains a version number allowing for easy identification of the hardware and software version in embedded applications.

5.4 CW25 Build Options

There are 3 versions of the CW25 available:

CW25-NAV: This is the general navigation version of the receiver, as described in this datasheet.

CW25-ULS: This version of the CW25 includes Network Assistance, which allows the receiver to be sent ephemeris data from a base-station (such as the CW55) over a communications link, which allow the receiver to acquire initial positional lock in harsh environments, down to signal levels of -155dBm.
See CW25-ULS Datasheet for more Details.

CW25-TIM: This version of the CW25 has position-hold software included, which allows for very stable output frequency control for timing applications. See CW25-TIM Datasheet for more Details.

5.5 User Commands

The CW25-NAV can accept a number of specific user commands that can be used to set receiver parameters such as UART baud rate and message subset. NCO frequency, 1 pps initialization etc. These commands are defined in detail within the CW25 User Manual and the set values are stored in Non-Volatile Memory (NVM) within the CW25-NAV receiver.

6 APPLICATION HINTS

The following are a list of application hints that may help in implementing system based on the CW25-NAV.

6.1 Power Supply

The power supply requirements of the CW25-NAV can all be provided from a single 3.3V supply. To simplify system integration on-board regulators provide the correct voltage levels for the RF and oscillator (2.9V or 3.0V) and low voltage digital core (1.8V). In power sensitive applications it is recommended that the DIG_1V8 supply is provided from a high efficiency external 1.8V source e.g. switch mode power supply, rather than the on-board linear regulator.

If the source impedance of the power supply to the CW25-NAV is high due to long tracks, filtering or other causes, local decoupling of the supply signals may be necessary. Care should be taken to ensure that the maximum supply ripple at the pins of the CW25-NAV is 50mV peak to peak.

6.2 RF Connection

The RF connection to the CW25-NAV can be done in two ways. The preferred method is to use standard microstrip design techniques to track from the antenna element to the RF_IN castellation,. This also allows the systems integrator the option of designing in external connectors suitable for the application. The user can easily fit an externally mounted MCX, SMA or similar connector, provided it is placed adjacent to the RF_IN castellation. If the tracking guidelines given below are followed, the impedance match will be acceptable. The diagram below shows how this could be achieved. In this diagram, the centre via of the RF connector is presumed to be plated through with a minimal pad top and bottom. The PCB material is assumed to be 1.6mm thick FR4 with a dielectric constant of 4.3. Two situations are considered; one with no ground plane and one with a ground plane on the bottom of the board, underneath the RF connector. In both cases there is no inner layer tracking under the RF connector.

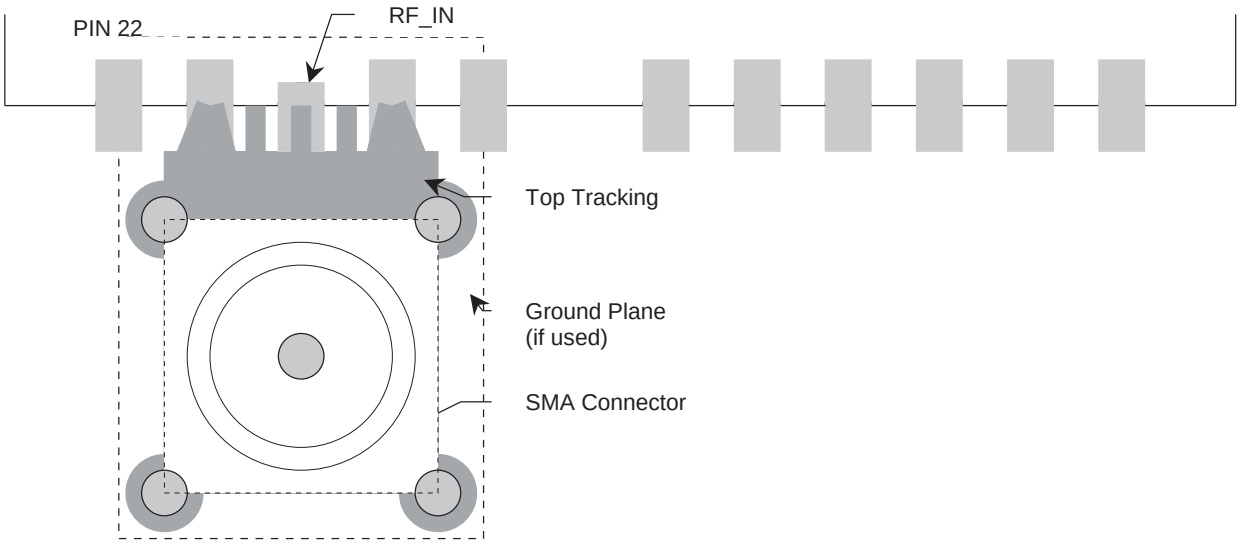

Figure 5 — RF Tracking Example

The widths of the RF_IN track and the associated gaps are given in the table below.

Scenario	**Track Width** (1/1000 Inch)	**Gap Width** (1/1000 Inch)
Without ground plane	37	6
	56	8
With ground plane	32	6
	43	8

Table 7 RF Track & Gap Widths

Alternatively, the user can attach the antenna to the Hirose H.FL-R-SMT using a flying lead fitted with a suitable plug.

6.3 Grounding

In connecting the CW25-NAV into a host system, good grounding practices should be observed. Specifically, ground currents from the rest of the system hosting the CW25-NAV should not pass through the ground connections to the CW25-NAV. This is most easily ensured by using a single point attachment for the ground. There must also be a good connection between the RF_GND and the DIG_GND signals. Whilst there is not a specific need to put a ground plane under the CW25-NAV, high energy signals should not be tracked under the CW25-NAV. It is however recommended that a ground plane be used under the CW25-NAV. In this case, the following would be an example of the pattern that may be used

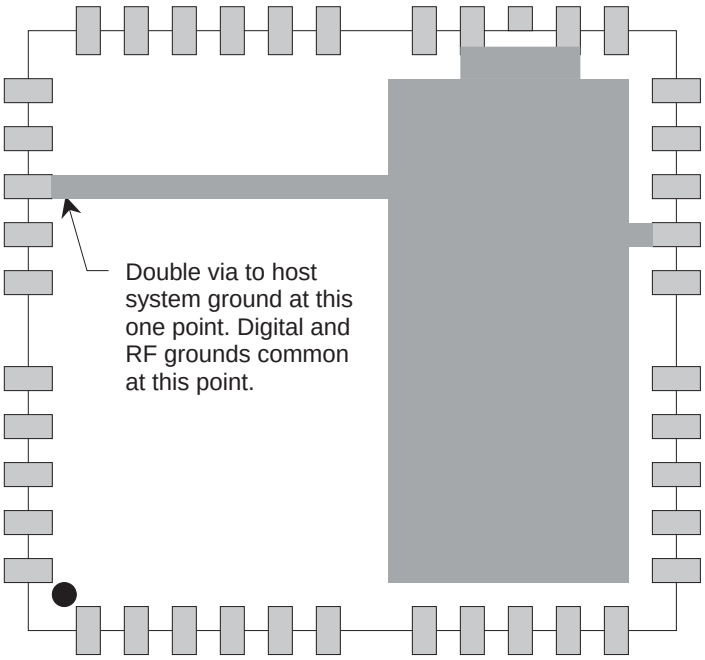

Figure 6 — Grounding the CW25-NAV with a Ground Plane

7 Battery Backup

The CW25-NAV has an on-board real time clock (RTC). This is used to store date and time information whilst the CW25-NAV is powered down. Having a valid date and time speeds the time to first fix (TTFF), allowing the CW25-NAV to meet its quoted TTFF specification. The CW25-NAV relies on an external power source to power the RTC (VBATT) when the DIG_3V3 is not present. If the user application does not require the warm or hot fix performance, or the required information is provided by network assistance, there is no need to provide the VBATT signal. The VBATT signal must be greater than 2.6V and less than DIG_3V3 + 0.6V. Typically, a 3V lithium primary cell or a high capacity "supercap" will be used. The CW25-NAV has an internal blocking diode, so if a "supercap" or rechargeable battery is used, an external charging circuit will be required.

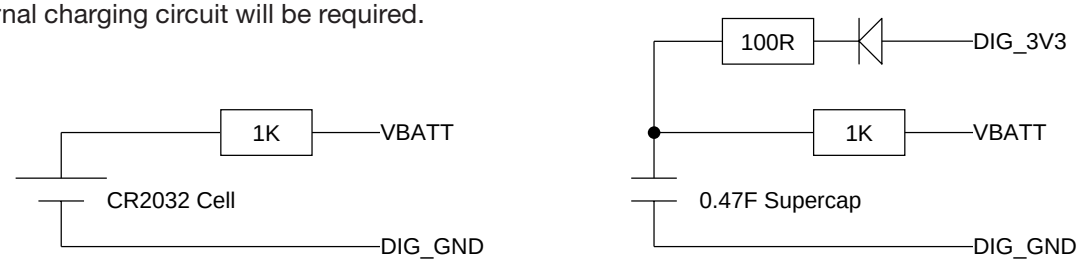

Figure 7 — Typical VBATT Supplies

The 1K resistor is recommended at it limits current in the VBATT circuit and provides an easy way to measure the current in the VBATT signal. The 100R limits the inrush current into the "supercap".

7.1 Over Voltage & Reverse Polarity Protection

The CW25-NAV contains no over voltage or reverse polarity protection. The CW25-NAV should be handled as a CMOS component, with full antistatic handling precautions. Any fault condition that results in the maximum limits being exceeded may irreparably damage the CW25-NAV.

7.2 LEDs

There are two connections on the CW25-NAV specifically intended to drive status LEDs. The LED_RED and LED_GRN signals should be connected, via suitable current limiting resistors, to the anodes of low current LEDs whose cathodes are connected to DIG_GND. The outputs are standard 3.3V CMOS and the current drawn should be limited to 5mA per output. Using a 270 ohm resistor provides a suitable current limit. If appropriately coloured LEDs are attached to these signals, other documentation (eg. user manuals) that refers to these status LEDs will be correct. If LEDs are not required, these signals can be left open. These signals may be connected to other logic if required.

7.3 Reset Generation

The power on reset for the CW25-NAV is generated on-board. It is generated by the regulator for the RF section. This signal is an active low, open collector signal and is presented on the NPOR castellation. If it is desired to extend the power on reset signal or provide a manual reset for the CW25-NAV, this signal can be driven from an open collector source at any time. The nPOR signal of the BB25IC, to which the NPOR castellation is connected, has a Schmitt trigger input. This means that there are no constraints on the rise time of the NPOR signal.

There is a second reset signal on the CW25-NAV, the NRESET signal. NRESET is also an active low open collector signal. This signal is generated by the BB25IC in response to the NPOR signal. It can also be generated under software control. Asserting the NRESET signal from an external open collector source will reset the ARM9 in the BB25IC without resetting the whole chip. Generally, this signal will be left open.

7.4 Boot Options

The CW25-NAV has two boot modes. These are selected by the state of the BOOTSEL signal when the NPOR signal goes inactive (high). Normally, BOOTSEL is left open so that a pull-up bias in the BB25IC will keep that signal high. When BOOTSEL is high, the CW25-NAV boots from the FLASH that is internal to the BB25IC. If BOOTSEL is tied low, the CW25-NAV boots from the ROM internal to the BB25IC. This ROM has a boot loader that polls the serial ports and I2C bus for boot code. This mode of operation requires special user handling and should only be used in conjunction with specific application notes.

CW25-NAV

NAVSYNC Ltd. World Headquarters

Bay 143
Shannon Industrial Estate
Shannon, Co. Clare, Ireland
Phone: +353 61 475 666
E-mail: sales@navsync.com

In North America

2111 Comprehensive Drive
Aurora, IL 60505, USA
Phone: 630.851.4722, ext. 4109
E-mail: northamerica@navsync.com

www.navsync.com