PRELIMINARY

HD-SDI and SD-SDI SMPTE Jitter Performance of the Independent Channel HOTLink II™ Transceiver in a System

Table of Contents

1. Introduction

The HOTLink II™ family of physical layer (PHY) devices is a point-to-point or point-to-multipoint communications building block that provides serialization, deserialization, optional 8B/10B encoding/decoding and framing functions. It can transport serial data at rates from 195 Mbps to 1.5 Gbps per channel and is compliant to digital video standards such as SMPTE 259M, SMPTE 292M and DVB-ASI.

The Society of Motion Picture and Television Engineers (SMPTE) is a professional organization that develops interface and protocol standards for the professional video industry. Two such standards are SMPTE 259M(SD-SDI) and SMPTE 292M(HD-SDI).

The HOTLink II family of video devices are compliant to both SMPTE 292M and SMPTE 259M requirements. This includes intrinsic jitter requirements specified in SMPTE 259M and SMPTE 292M. The purpose of this application note is to present the results of SMPTE SD-SDI and HD-SDI jitter generation and jitter tolerance. The testing was done on a Multi-format Serial Digital Interface system using the Quad Independent Channel HOTLink II Video Board. The HOTLink II Independent Channel Video Board is a full-fledged serial digital video reference platform that incorporates HOTLink II interfaces to industry-standard cable drivers and equalizers. Upstream processing of the pre-encoded video data and the decoded video data is performed using on-board FPGAs. The board also has a flexible clocking architecture with automatic rate-detection that allows the board to be able to pass video traffic in multiple formats. The measurements were performed using industry-standard test equipment that generates and monitors/measures the SDI Video data as per SMPTE recommendations. The equipment also has the capability to modulate jitter which was used for measuring jitter tolerance. All measurements shown in this application note are typical measurements taken under typical power supply voltage and room temperature unless explicitly stated otherwise. Although, the measurements were performed on the HOTLink II CYV15G0404DXB device, the data on this application note can be applied for any device in the HOTLink II Video Family of Transceivers. For more information on the board, refer to the user's guide of the board available in the Cypress Internet website (http://www.cypress.com) or call Cypress Applications support at 1-408-943-2821.

2. Jitter Generation of HOTLink II Transceivers

Jitter generation is defined as intrinsic jitter present at the output port of a device in the absence of applied input jitter.

2.1 Reclocked Output Jitter of HOTLink II Transceiver with Gennum 3.3V Cable Driver and Equalizer

This section will cover the output jitter of HOTLink II transceiver (CYV15G0404DXB) when the data recovered by the clock and data recovery unit of the device is retransmitted through the serial output buffers (RECLKENx = HIGH).

Note that in this mode, the output jitter is dependent upon the intrinsic jitter present in the serial input data and the characteristics of the internal PLLs of the HOTLink II Transceiver. The jitter contributed due to the cable driver and equalizer is also included in the jitter measured. The intrinsic power supply noise and the noise generated due to switching of different devices in the board also contribute to the measured jitter. The jitter present in the reference clock will not affect the reclocked output jitter of the HOTLink II transceiver in reclocker mode.

Jitter generation testing was performed on Quad Independent Channel HOTLink II Transceivers using standard test equipment used by the video industry. Both Timing Jitter as well as Alignment Jitter were measured. The equipment used for the testing described in this section is as follows:

1. Tektronix WFM700M - SD/HD SDI Waveform monitor.
2. Tektronix TG2000 - SD/HD SDI Pattern generator.
3. HOTLink II CYV15G0404DXB Video Board.
4. Two 75Ω Coaxial cables.
5. Wall power supply - 9V DC Output

A block diagram of the test set-up is shown in *Figure 1*. The actual test set-up is illustrated in *Figure 2*. The Tektronix TG2000 is used to generate 75% SMPTE color bars at both the SD-SDI and HD-SDI data rates. Before performing the measurement, the data generator's (TG2000) intrinsic output jitter was measured (See *Table 1* and *Table 2* for SMPTE 259M and SMPTE 292M color bar measurements, respectively). The TG2000 module called DVG1 is used for SD-SDI data generation. The TG2000 module called HDVG1 is used for HD-SDI data generation. The SDI data from the TG2000 generator is fed to the primary serial input (INx1 of any channel of HOTLink II CYV15G0404DXB Video Board). The video board is configured through the GUI to perform reclocking in the selected channel. The SDI data passes through Gennum GS1524 Equalizer after which it is fed to the HOTLink II Serial Inputs. The clock and data are recovered by the CDR unit embedded in the HOTLink II Transceiver. The

reclocked data is retransmitted to the serial output of the same channel. The serial output is fed to the WFM700 Waveform monitor through the GS1528 Cable Driver.

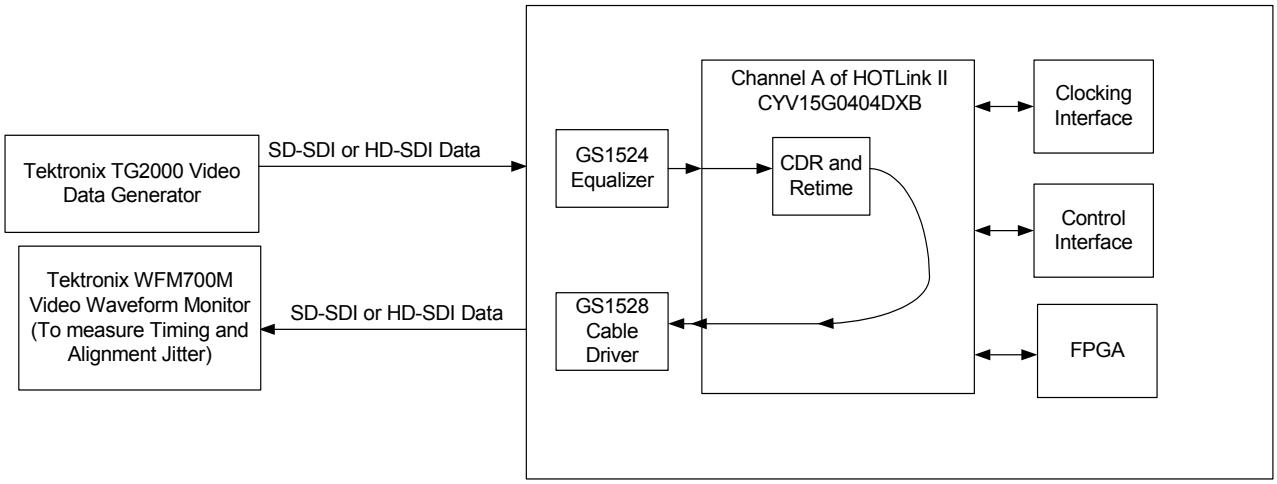


Figure 1. Block Diagram of Test Set-up to measure HD-SDI and SD-SDI Reclocked Output Timing and Alignment jitter

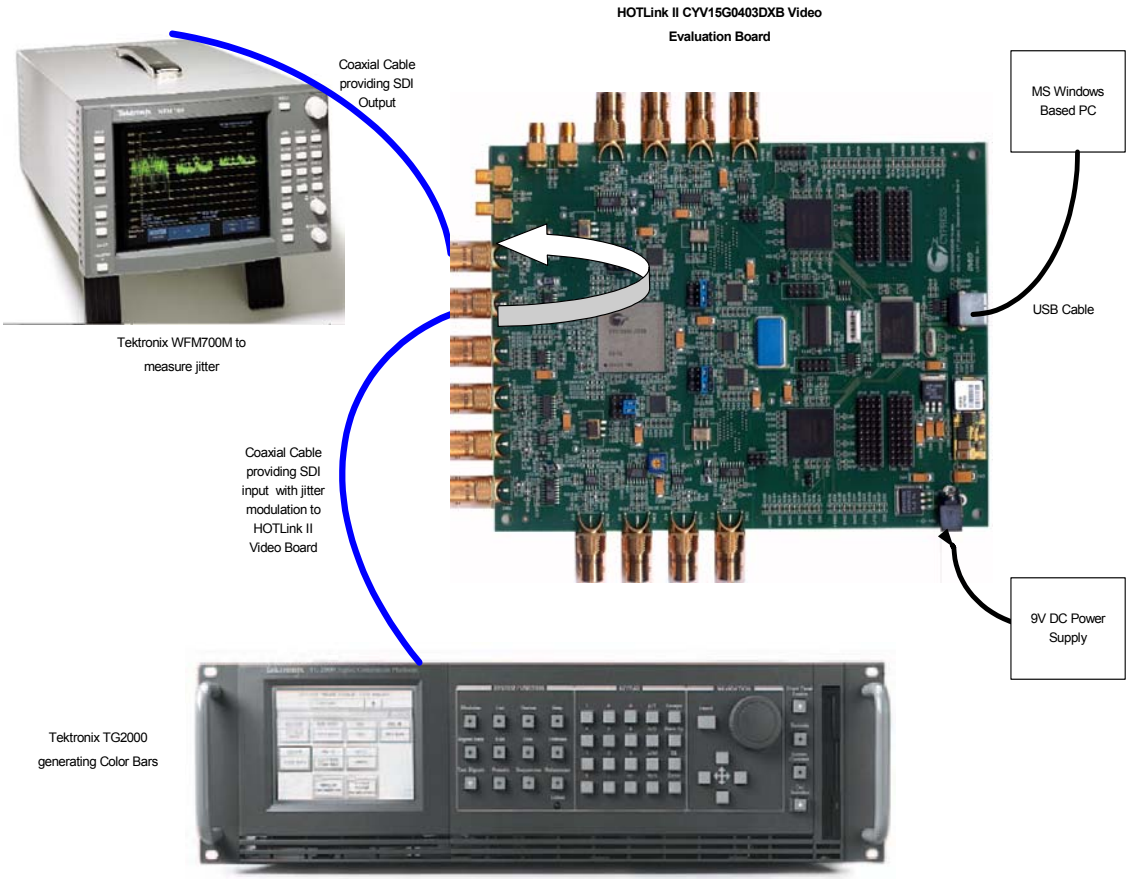


Figure 2. Pictorial Test Setup to measure SD-SDI and HD-SDI Timing and Alignment jitter

2.1.1 SD Reclocked Output (SMPTE 259M Color Bars)

The output jitter measured for SMPTE 259M Color Bar Data (SD-SDI) using the method described in Section 2.1 is shown in *Table 1* and illustrated in *Figure 3*. The results show that even with the presence of input jitter, the HOTLink II reclocker output jitter meets the SMPTE Timing Jitter and Alignment Jitter specs for SD-SDI with sufficient margin.

Table 1. Reclocked Output jitter of HOTLink II SDI Reclocker for SD-SDI Color Bar including Gennum 3.3V Cable Driver and Equalizer

Parameter	Jitter measured at HOTLink II Outputs by WFM700M (UI)	SMPTE SPEC (UI)	TG2000 Data Generator Intrinsic Jitter measured by WFM700M (UI)	Margin to Spec including equipment noise floor (UI)	Margin to Spec including equipment noise floor (%)
SMPTE 259M - SD Timing Jitter	0.098	0.2	0.088	0.102	51%
SMPTE 259M - SD Alignment Jitter	0.098	0.2	0.088	0.102	51%

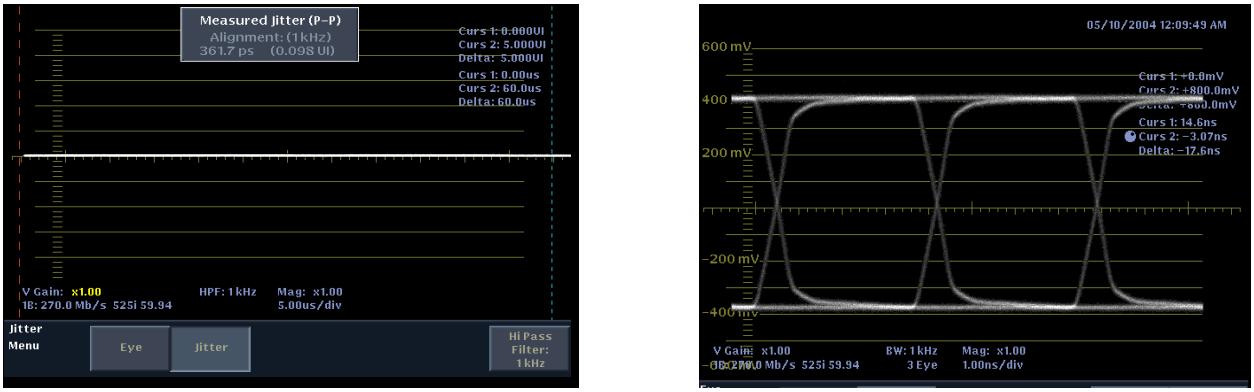


Figure 3. SD reclocked output alignment jitter

2.1.2 HD Reclocked Output Jitter (SMPTE 292M Color Bars)

The output jitter measured for SMPTE 292M Color Bar Data (HD-SDI) using the method described in Section 2.1 is shown in *Table 2* and illustrated in *Figure 4*. The results show that even with the presence of input jitter, the HOTLink II reclocker output jitter meets the SMPTE Timing Jitter and Alignment Jitter specs for HD-SDI with margin.

Table 2. Reclocked Output jitter of HOTLink II Reclocker for HD-SDI Color Bar including Gennum 3.3V Cable Driver and Equalizer

Parameter	Jitter measured at HOTLink II Outputs by WFM700M (UI)	SMPTE SPEC (UI)	TG2000 Data Generator Intrinsic Jitter measured by WFM700M (UI)	Margin to Spec including equipment noise floor (UI)	Margin to Spec even including equipment noise floor (%)
SMPTE 292M - HD Timing Jitter	0.225	1	0.156	0.775	77.5%
SMPTE 292M - HD Alignment Jitter	0.176	0.2	0.107	0.024	12%

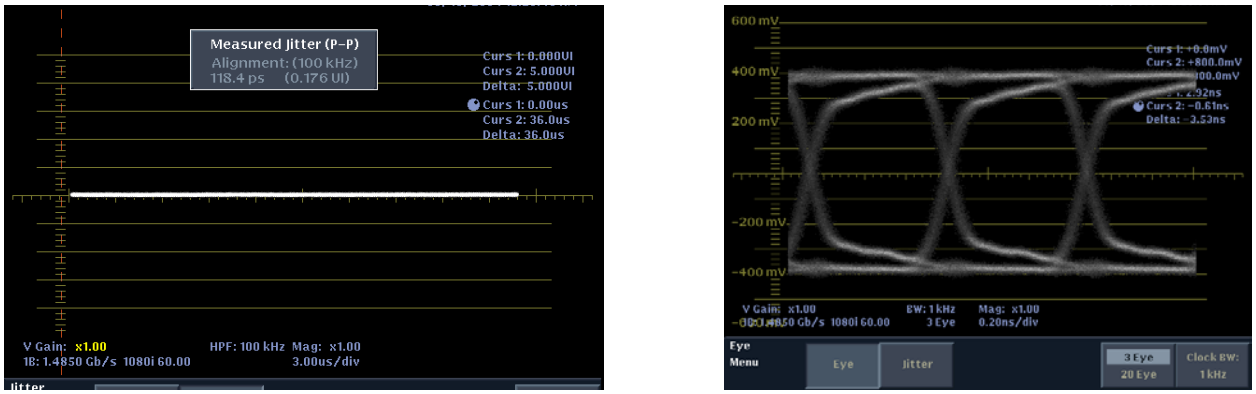


Figure 4. HD reclocked output alignment jitter

2.2 Reclocked Output Jitter of HOTLink II Reclocker alone

The reclocked output jitter directly from the HOTLink II serial outputs (without a cable driver at the outputs and without an equalizer at the inputs) can be measured using the CYV15G0404DXB Evaluation board. This board is a dedicated board that can be used to evaluate HOTLink II CYV15G0404DXB devices alone without any interfacing devices like FPGAs, Equalizers or Cable Drivers.

The equipment used for the testing described in this section is as follows:

1. Agilent 86100A Widebandwidth Oscilloscope
2. Agilent 8133A pulse generator
3. 3.3V Power supply
4. 50Ω Coaxial cables

The test set-up to measure jitter using this method is shown in *Figure 5*. One channel of the CYV15G0404DXB evaluation board is configured to generate BIST (Built-In Self Test) output data at either SD-SDI or HD-SDI rates. The output from this channel is fed as the input to the channel under test. The channel under test is configured to operate in reclocker mode (RECLKENx = HIGH). The reclocked serial output data is fed to the inputs of the wide bandwidth oscilloscope to generate an eye-diagram. The reference clock for both channels are provided from an external clock generator (Agilent 8133A). The jitter measured using this method represents broadband jitter (all jitter frequencies) without any jitter filters recommended by SMPTE. Applying jitter filters to this measurement will give same or better jitter numbers.

2.2.1 SMPTE 259M (SD-SDI)

The eye-diagram and jitter results obtained using the above mentioned method at SD-SDI datarate (270 Mbps) are shown in *Figure 6*. The jitter histogram shows that the reclocked output jitter measured for approximately 10000 hits is around 133ps p-p (**0.035UI**).

2.2.2 SMPTE 292M (HD-SDI)

The eye-diagram and jitter results obtained using the above mentioned at HD-SDI datarate (1485 Mbps) method is shown in *Figure 7*. The jitter histogram shows that the output jitter measured for approximately 10000 hits is around 107ps p-p (**0.158UI**).

2.3 Total Output Jitter including Gennum's 3.3V Cable Driver Outputs and on-board Reference Clock

The transmit output jitter of the Quad Independent Channel HOTLink II Video Board's entire transmit path is covered in this section. The total output jitter is measured at the outputs of the Cable Driver in the Video Board. The total jitter comprises the HOTLink II output intrinsic jitter, Cable Driver intrinsic jitter and a portion of the Reference Clock jitter. For SD-SDI Jitter Measurements, the 27 MHz reference clock is provided from the on-board programmable clock. For HD-SDI jitter measurements, the 74.25 MHz reference clock is provided by the on-board crystal oscillator, since the intrinsic jitter of the programmable clock is quite high at 74.25 MHz clock frequency.

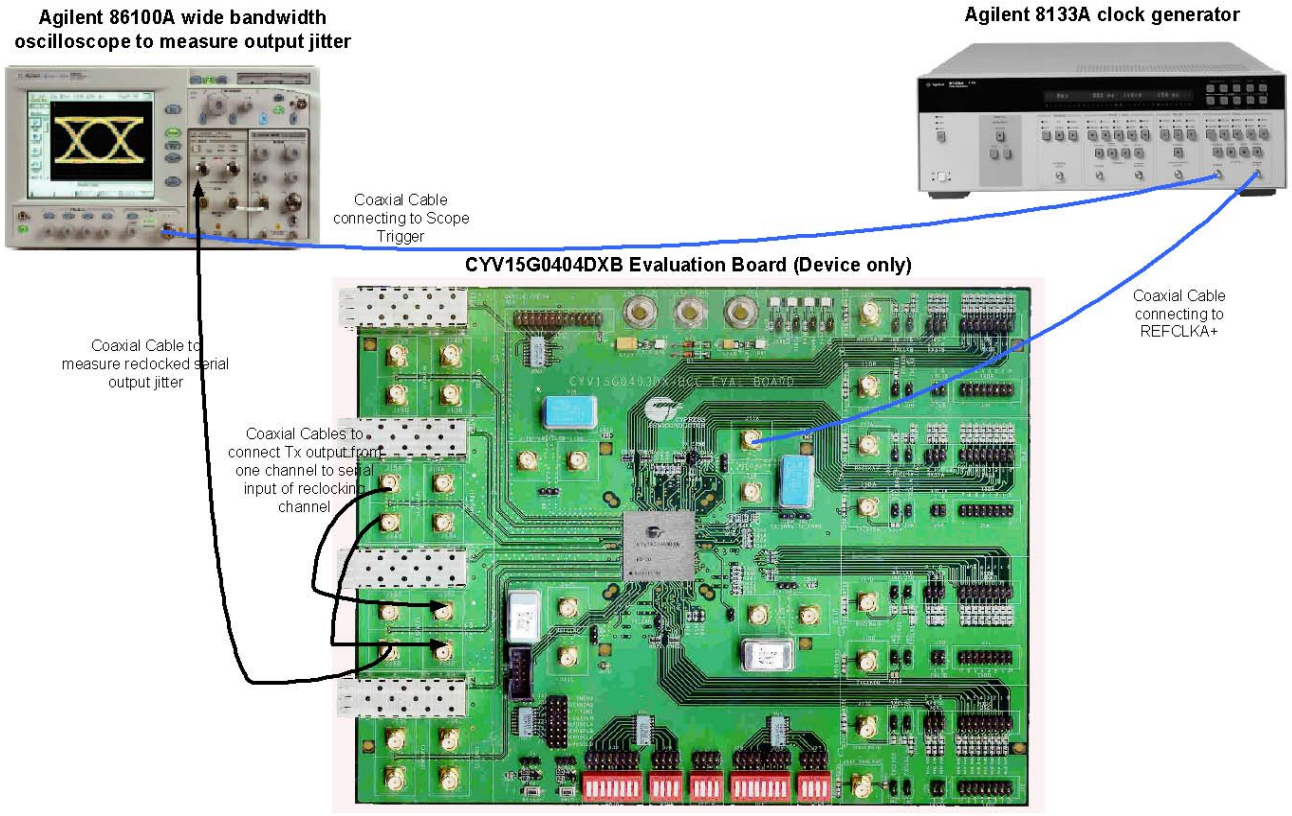


Figure 5. Test set-up to perform reclocked output jitter measurements on the HOTLink II Device alone

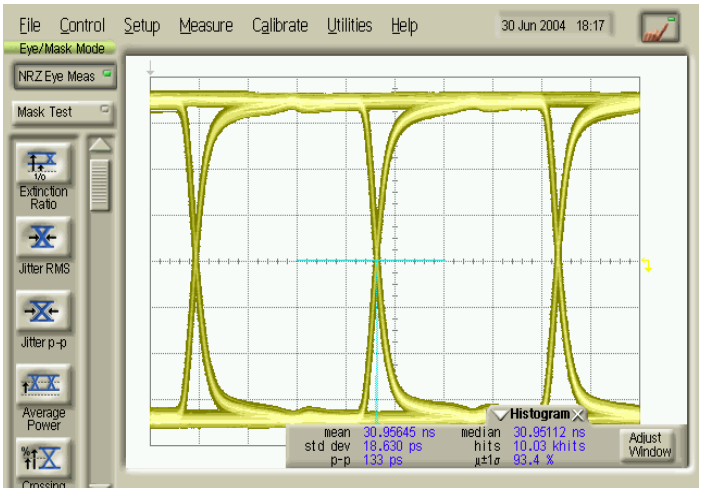


Figure 6. SD-SDI reclocked output jitter eye-diagram from the HOTLink II Device serial outputs

Test set-up to perform Total Output Jitter Generation Measurements using the Quad Independent Channel HOTLink II Video Board

Jitter generation testing was performed on Quad Independent Channel HOTLink II Video Board that incorporates a Gennum 3.3V Cable Driver using industry standard test equipment. Both Timing Jitter as well as Alignment Jitter were measured. The equipment used for the testing described in this section is as follows:

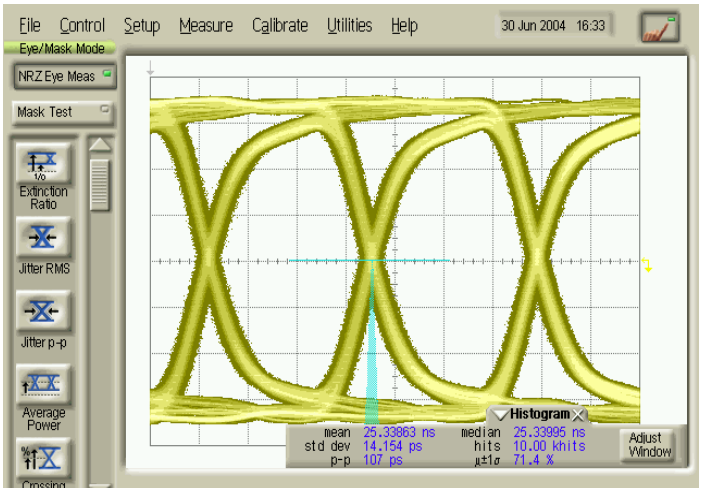


Figure 7. HD-SDI reclocked output jitter eye-diagram from the HOTLink II Device serial outputs

1. Tektronix WFM700M - SD/HD SDI Waveform monitor.
2. HOTLink II CYV15G0404DXB Video Evaluation Board
3. Computer with USB Cable to Configure HOTLink II Video Evaluation Board
4. Appropriate Coaxial cables
5. Wall power supply - 9V DC Output

The block diagram of the test set-up is shown in *Figure 8*. The test set-up is shown in *Figure 9*. The results are shown in *Table 3* and *Table 4*.

The HOTLink II Video Evaluation Board is configured to generate, scramble and serialize SDI Color Bar data. The Serial Outputs from the HOTLink II device are input into the Gennum GS1528 3.3V Cable Driver. The data output from the cable driver is analyzed by the WFM700, and the timing and alignment jitter are measured. This jitter is dependent upon the jitter input into the REFCLK, the jitter generated by HOTLink II Transmitter, the jitter generated by the Cable Driver and also power supply noise.

2.3.1 SMPTE 259M Color Bars

The output jitter measured for SMPTE 259M Color Bar Data (SD-SDI) using the method described in Section 2.3 is shown in *Table 3* and illustrated in *Figure 10*. The results show that the combined output jitter of the Quad Independent Channel HOTLink II Video Board transmit path including the reference clock and cable driver meets the SMPTE Timing Jitter and Alignment Jitter specs for SD-SDI with sufficient margin.

2.3.2 SMPTE 259M SDI Checkfield

The output jitter measured for SMPTE 259M SDI Checkfield Data (SD-SDI RP178) using the method described in Section 2.3 is shown in *Table 4*. The results show that the combined output jitter of the Quad Independent Channel HOTLink II Video Board transmit path including the reference clock and cable driver meets the SMPTE Timing Jitter and Alignment Jitter specs for SD-SDI with sufficient margin.

2.3.3 SMPTE 292M Color Bars

The total output jitter of the HOTLink II transmitter combined with a HD Cable Driver for SMPTE 292M Color Bars is covered in this section.

The output jitter measured for SMPTE 292M Color Bar Data (HD-SDI) using the method described in Section 2.3 is shown in *Table 5* and illustrated in *Figure 11*. The results show that the combined output jitter of the Quad Independent Channel HOTLink II Video Board transmit path including the reference clock and cable driver meets the SMPTE Timing Jitter and Alignment Jitter specs for HD-SDI with sufficient margin.

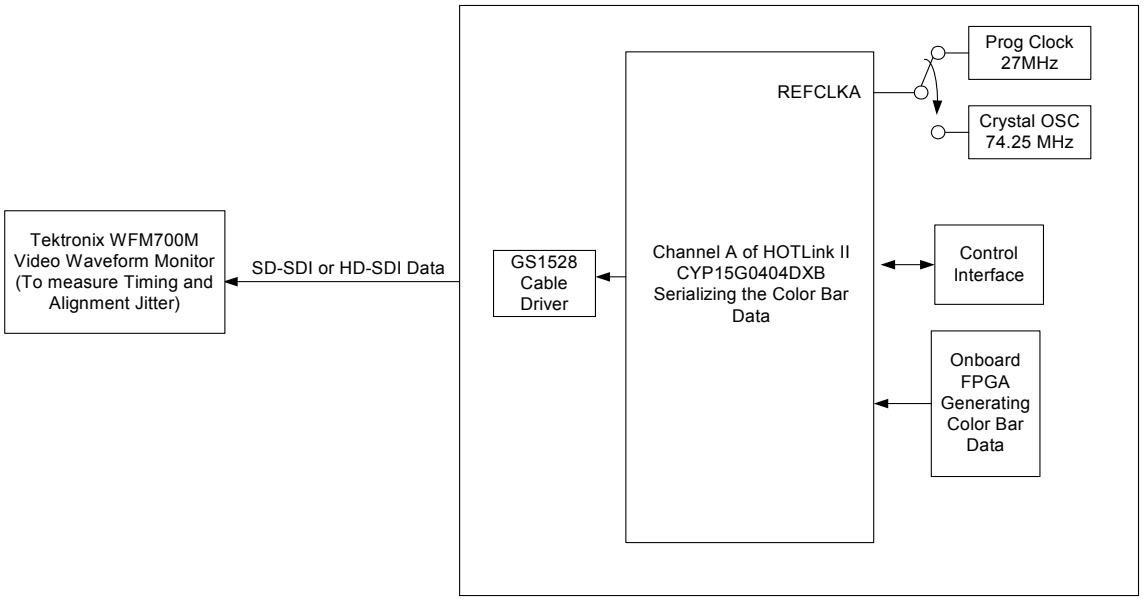


Figure 8. Block Diagram of Test Set-up to measure SD-SDI and HD-SDI Timing and Alignment jitter with GS1528 Cable Driver

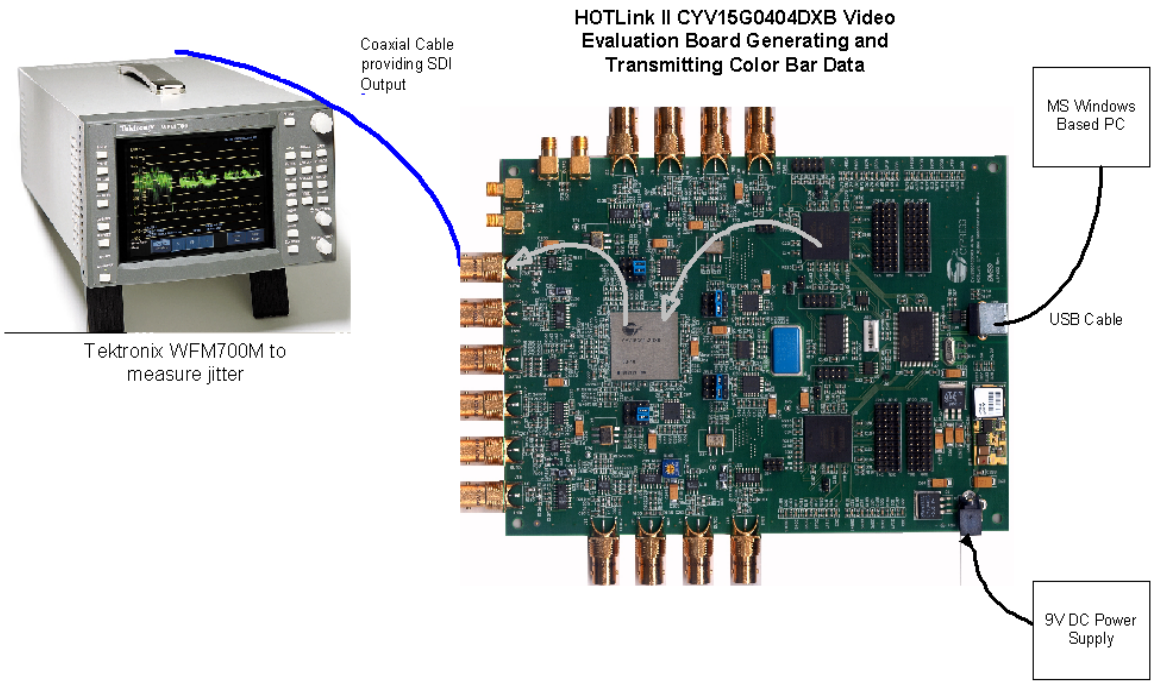


Figure 9. Pictorial Test Setup to measure SD-SDI and HD-SDI Timing and Alignment jitter with GS1528 Cable Driver

2.3.4 SMPTE 292M SDI Checkfield

The output jitter measured for SMPTE 292M SDI Checkfield Data (HD-SDI RP 198) using the method described in Section 2.3 is shown in *Table 6*. The results show that the combined output jitter of the Quad Independent Channel HOTLink II Video Board

Table 3. Typical Jitter generated by GS1528 Cable Driver when interfaced to HOTLink II Outputs while using an FPGA to generate SD-SDI color bar data

Parameter	Jitter measured at GS1528 output (UI)	SMPTE SPEC (UI)	Margin to Spec (UI)	Margin to Spec (%)
SMPTE 259M - SD Timing Jitter	0.107	0.2	0.093	46.5%
SMPTE 259M - SD Alignment Jitter	0.107	0.2	0.093	46.5%

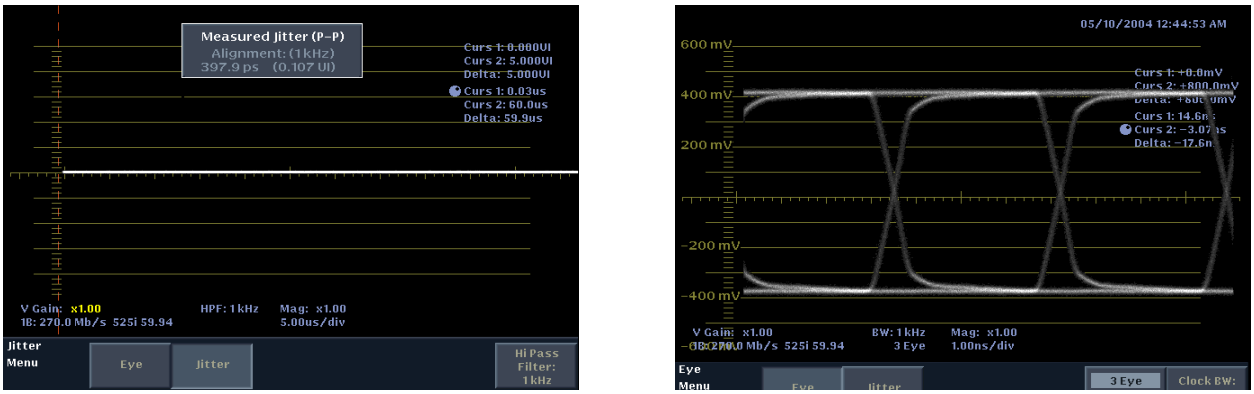


Figure 10. SD output alignment jitter

Table 4. Typical Jitter generated by GS1528 Cable Driver when interfaced to HOTLink II Outputs while using an FPGA to generate SD-SDI Checkfield data

Parameter	Jitter measured at GS1928 output (UI)	SMPTE SPEC (UI)	Margin to Spec (UI)	Margin to Spec (%)
SMPTE 259M - SD Timing Jitter	0.098	0.2	0.102	51%
SMPTE 259M - SD Alignment Jitter	0.098	0.2	0.102	51%

Table 5. Typical Jitter generated by GS1528 Cable Driver when interfaced to HOTLink II Outputs while using an FPGA to generate HD-SDI color bar data

Parameter	Jitter measured at GS1528 output (UI)	SMPTE SPEC (UI)	Margin to Spec (UI)	Margin to Spec (%)
SMPTE 292M - HD Timing Jitter	0.195	1	0.805	80.5%
SMPTE 292M - HD Alignment Jitter	0.156	0.2	0.044	22%

transmit path including the reference clock and cable driver meets the SMPTE Timing Jitter and Alignment Jitter specs for HD-SDI with sufficient margin.

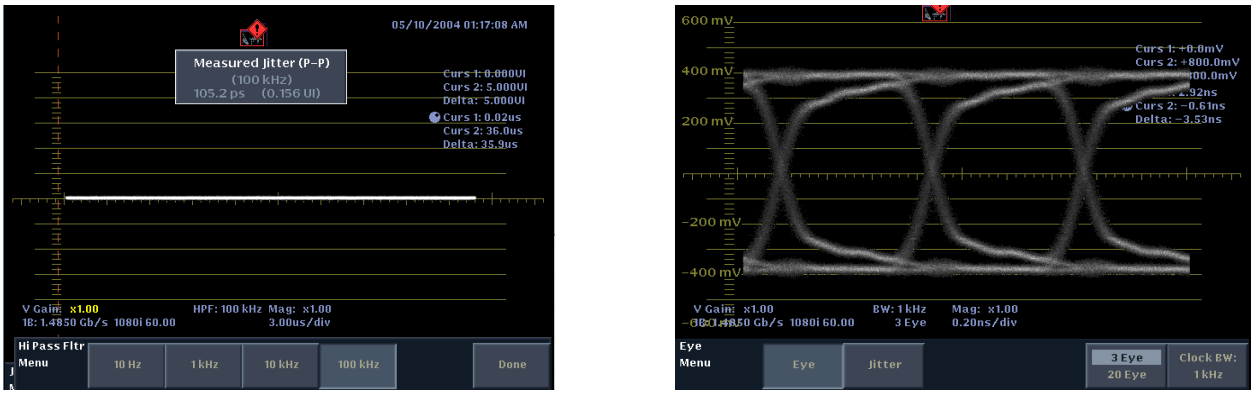


Figure 11. HD output alignment jitter

Table 6. Typical Jitter generated by GS1528 Cable Driver when interfaced to HOTLink II Outputs while using an FPGA to generate HD-SDI Checkfield data

Parameter	Jitter measured at GS1928 output (UI)	SMPTE SPEC (UI)	Margin to Spec (UI)	Margin to Spec (%)
SMPTE 292M - HD Timing Jitter	0.225	1	0.775	77.5
SMPTE 292M - HD Alignment Jitter	0.166	0.2	0.034	17%

2.4 Transmit Output Jitter of HOTLink II Transmitter alone

The transmit jitter directly from the HOTLink II serial outputs (without a cable driver) can be measured using the CYV15G0404DXB Evaluation board. This board is a dedicated board that can be used to evaluate HOTLink II CYV15G0404DXB devices alone without any interfacing devices like FPGAs, Equalizers or Cable Drivers. The test set-up to measure jitter using this method is shown in *Figure 12*. The CYV15G0404DXB evaluation board is configured to generate BIST (Built-In Self Test) output data at either SD-SDI or HD-SDI rates. The reference clock is provided from an external clock generator (Agilent 8133A). The serial output data is fed to the inputs of the wide bandwidth oscilloscope to generate an eye-diagram.

The equipment used for the testing described in this section is as follows:

1. Agilent 86100A Widebandwidth Oscilloscope
2. Agilent 8133A pulse generator
3. 3.3V Power supply
4. 50Ω Coaxial cables

2.4.1 SMPTE 259M (SD-SDI)

The eye-diagram and jitter results obtained using the above mentioned method at SD-SDI datarate (270 Mbps) are shown in *Figure 13*. The jitter histogram shows that the output jitter measured for approximately 10000 hits is around 133ps p-p (**0.035UI**). Note that this measurment is done without any jitter filters, while the actual SMPTE spec for SD-SDI alignment jitter with SMPTE jitter filters is 0.2UI.

2.4.2 SMPTE 292M (HD-SDI)

The eye-diagram and jitter results obtained using the above mentioned at HD-SDI datarate (1485 Mbps) method is shown in *Figure 14*. The jitter histogram shows that the output jitter measured for approximately 10000 hits is around 76ps p-p (**0.11UI**). Note that this measurment is done without any jitter filters, while the actual SMPTE spec for SD-SDI alignment jitter with SMPTE jitter filters is 0.2UI.

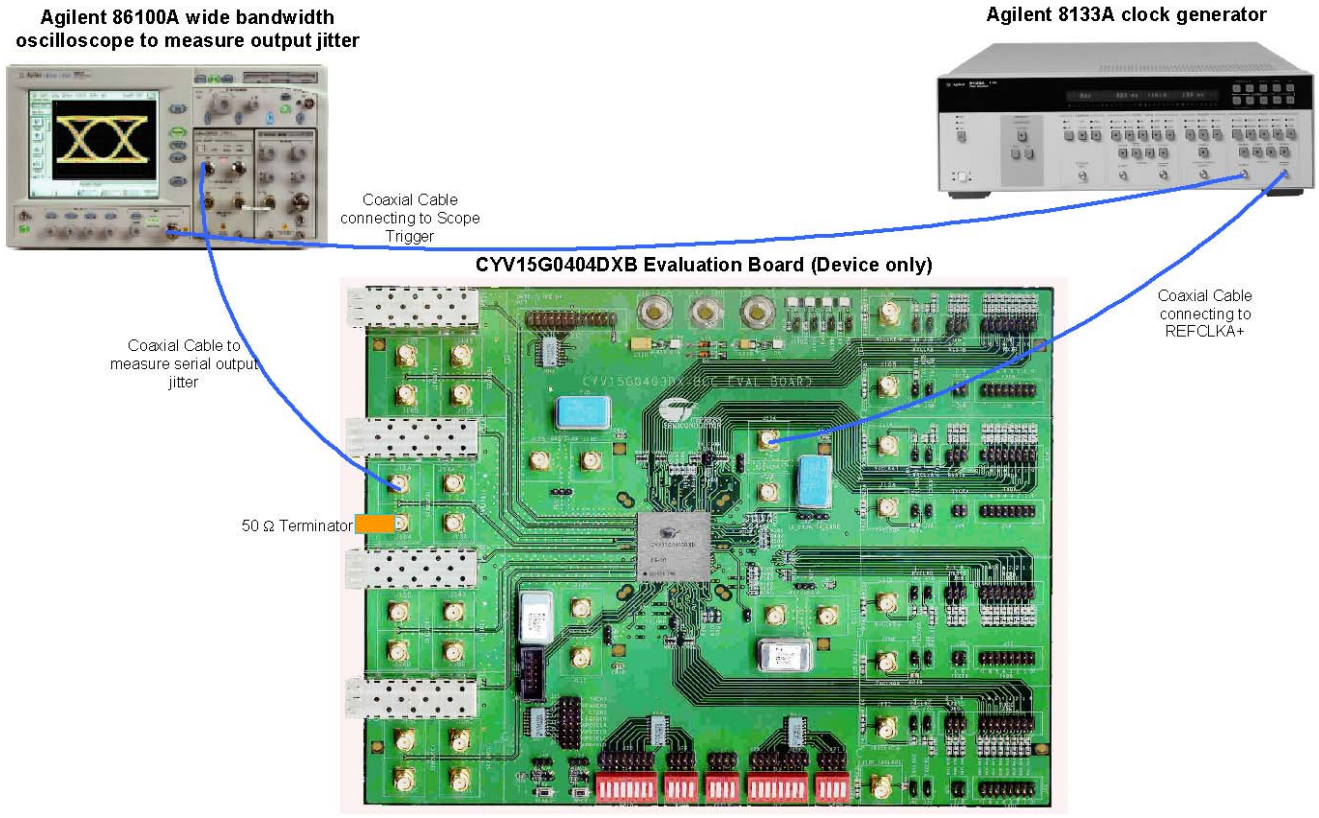


Figure 12. Test set-up to perform output jitter measurements on the HOTLink II Device alone

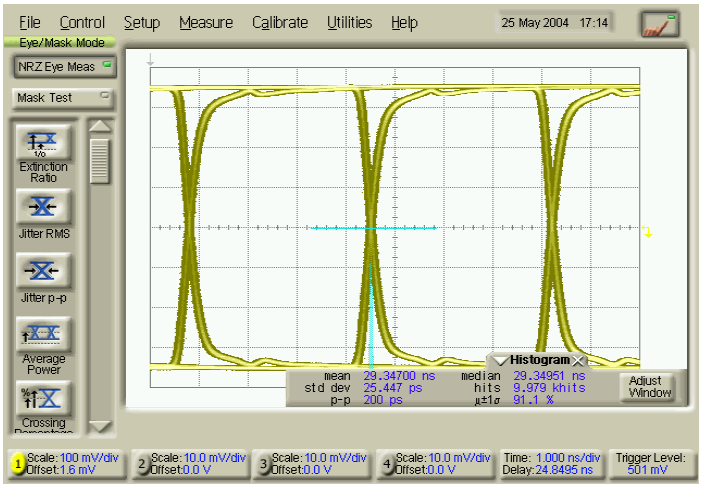


Figure 13. SD-SDI output jitter eye-diagram from the HOTLink II Device serial outputs

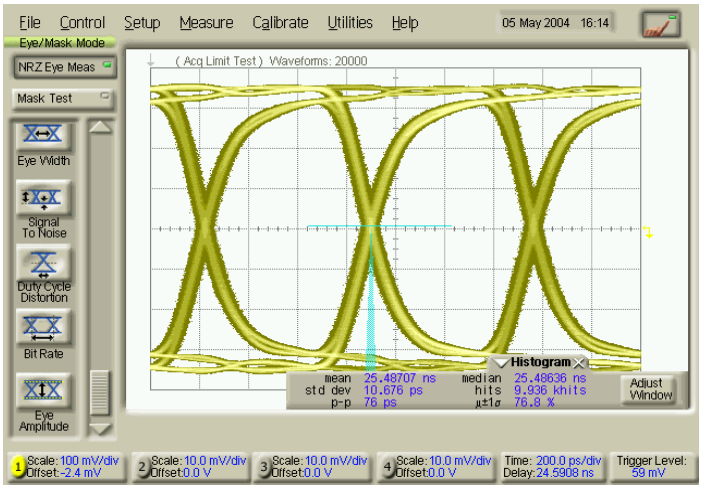


Figure 14. HD-SDI output jitter eye-diagram from the HOTLink II Device serial outputs

3. Jitter Tolerance of HOTLink II Receivers

Jitter tolerance is the ability of the receive CDR PLL to track the jitter in the incoming serial data stream. Jitter tolerance at a specific frequency is the amount of jitter the receive PLL can tolerate without any bit errors. The recommended methodology to perform this measurement is documented in SMPTE RP 192.

3.1 Jitter Tolerance of the HOTLink II Receiver with Cable Equalizer

The test procedure to perform this preliminary measurement is described below.

Test Set-up to perform Jitter Tolerance Testing

Jitter tolerance testing was performed on the Quad Independent Channel HOTLink II Video Board using industry standard video test equipment. The equipment used for the testing described in this section is as follows:

1. Tektronix WFM700M - SD/HD SDI Waveform monitor.
2. Tektronix TG2000 - SD/HD SDI Pattern generator.
3. HOTLink II CYV15G0404DXB Video Board.
4. Two 75Ω Coaxial cables.
5. Wall power supply - 9V DC Output

The test set-up is shown in *Figure 15*.

The Tektronix TG2000 is used to generate 75% color bar data at either SD-SDI or HD-SDI datarate with modulated jitter at a particular jitter frequency. The module called DVG1 is used for SD-SDI data generation with modulated jitter. The module called HDVG1 is used for HD-SDI data generation and module called HDST1 is used to modulate jitter to the HD-SDI data. The SDI data with modulated jitter from the TG2000 generator is fed to the serial input of the HOTLink II CYV15G0404DXB Evaluation board through the on-board GS1524 Equalizer. The selected channel of the HOTLink II device is configured through the GUI to perform a reclocking function. The reclocked serial output of the same channel is connected to the inputs of the Tektronix waveform monitor WFM700M. The waveform monitor is used to observe CRC errors. For each jitter frequency, the jitter amplitude is increased until the WFM 700M displays at least one CRC error in a span of 60 seconds. At each freqeuncy, the greatest jitter amplitude at each frequency for which there is no CRC error in the test duration is noted down as the jitter tolerance at that modulation frequency.

3.1.1 SMPTE 259M Color Bars

The typical and worst-case jitter tolerance exhibited by HOTLink II CYV15G0404DXB Device for SMPTE 259M Color Bars is shown graphically in *Figure 16* and tabulated in *Table 7*. The worst case jitter tolerance was measured over temperature (0 -70 Deg Celsius) and over 8 different transceiver channels. For some jitter frequencies, the Quad Independent Channel HOTLink II

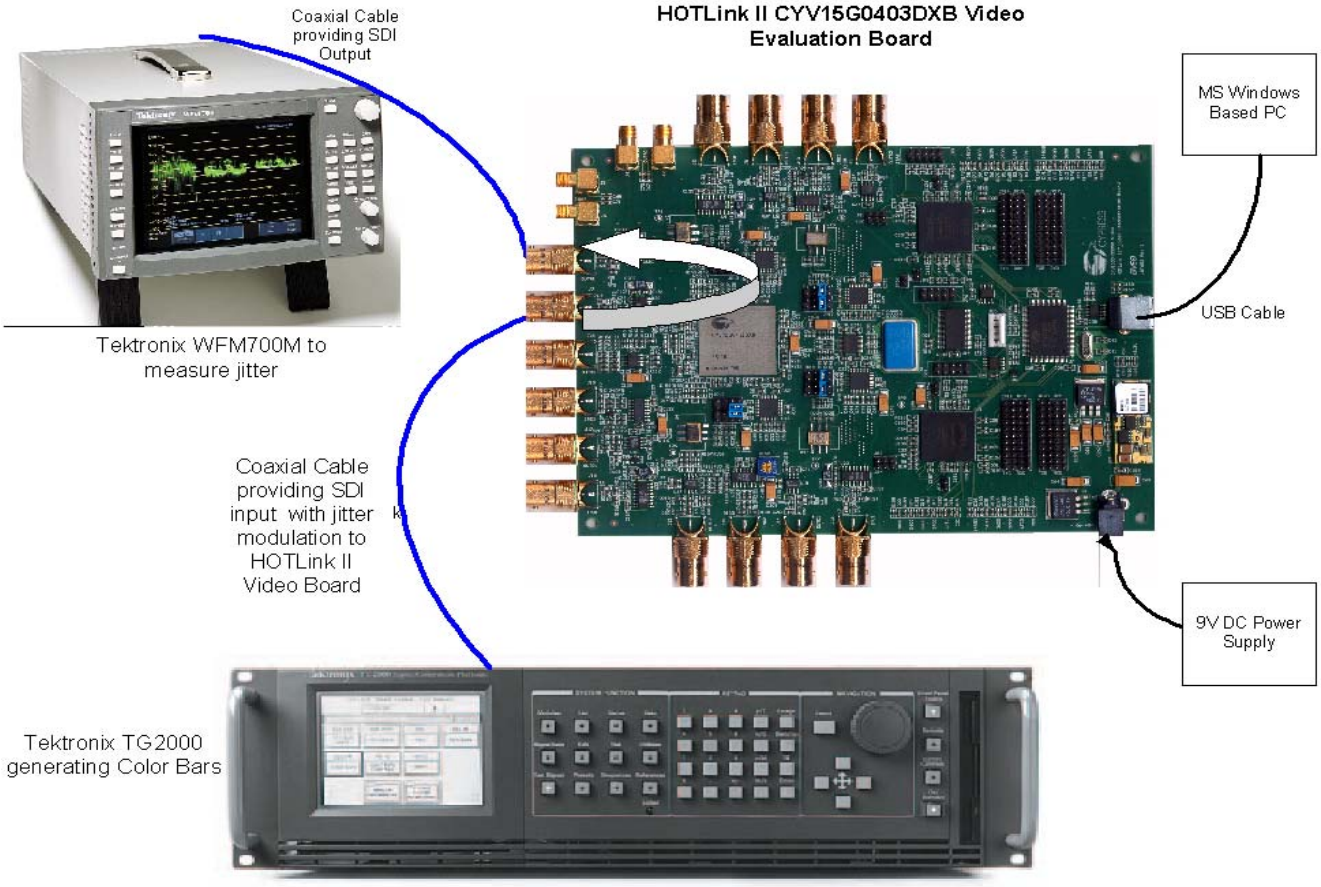


Figure 15. Test set-up to perform Jitter Tolerance Testing

Video Board Receiver was able to recover data with no errors for the maximum jitter that can be injected by the TG2000 equipment. This is indicated in the jitter tolerance plots as “Equipment Max” and in the tables with a “>” symbol.

Note that at high frequencies (around 10 MHz) the Quad Independent Channel HOTLink II Video Board Receiver can tolerate approximatley 0.6 UI of jitter as reported by Tektronix TG2000.

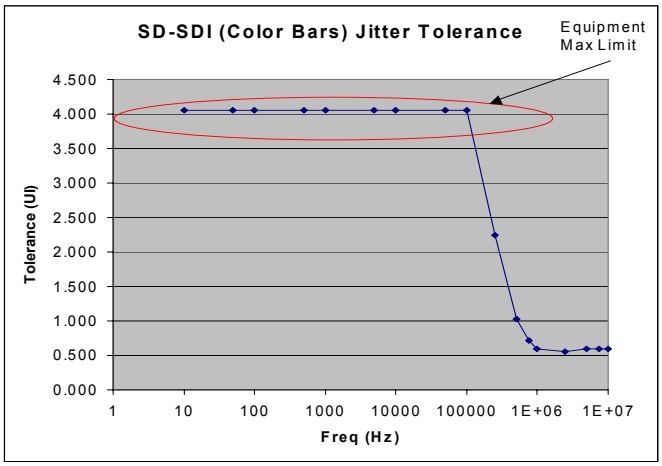
3.1.2 SMPTE 259M SDI Checkfield

The worst-case jitter tolerance exhibited by the HOTLink II CYV15G0404DXB Device for SMPTE 259M SDI Checkfield pattern is shown graphically in *Figure 17* and tabulated in *Table 8*. The worst case jitter tolerance was measured over temperature (0 -70 Deg Celsius) and over 8 different transceiver channels. For some jitter frequencies, the Quad Independent Channel HOTLink II Video Board Receiver was able to recover data with no errors for the maximum jitter that can be injected by the TG2000 equipment. This is indicated in the jitter tolerance plots as “Equipment Max” and in the tables with a “>” symbol.

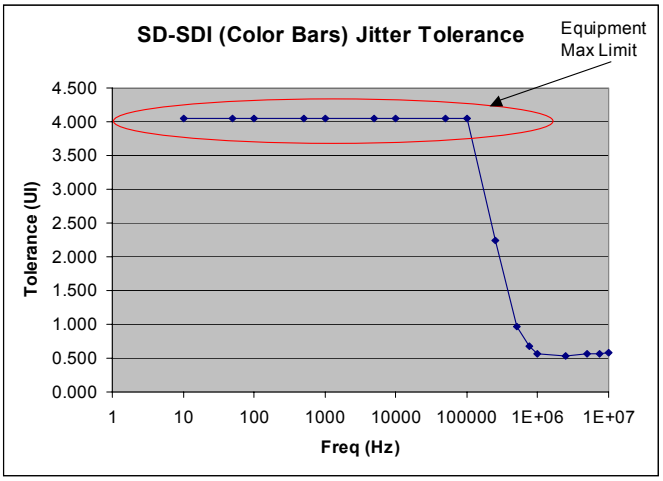
Note that as per SMPTE RP192, it is expected that the jitter tolerance for these pathological patterns will be worse than that for Color Bars.

3.1.3 SMPTE 292M Color Bars

The results of typical and worst case jitter tolerance testing for SMPTE 292M are shown graphically in *Figure 18* and tabulated in *Table 9*. The high frequency jitter tolerance is zoomed in and displayed in *Figure 19*. The worst case jitter tolerance was measured over temperature (0 -70 Deg Celsius) and over 8 different transceiver channels. For some jitter frequencies, the HOTLink II Receiver was able to recover data with no errors for the maximum jitter that can injected by the TG2000 equipment. This is indicated in the jitter tolerance plots as “Equipment Max” and in the tables with a “>” symbol. For frequencies greater than



Typical



Worst-Case

Figure 16. Quad Independent Channel HOTLink II Video Board SD-SDI Jitter Tolerance (Left - Typical, Right - Worst case)

Table 7. SD-SDI Jitter Tolerance of Quad Independent Channel HOTLink II Video Board

Freq (Hz)	Maximum TG2000 Jitter Modulation Tolerated by HOTLink II Receiver (UI)
10	> 4.05
50	> 4.05
100	> 4.05
500	> 4.05
1000	> 4.05
5000	> 4.05
10000	> 4.05
50000	> 4.05
100000	> 4.05
250000	2.24
500000	1.026
750000	0.71
1000000	0.594
2500000	0.55
5000000	0.59
7500000	0.59
10000000	0.59

Typical

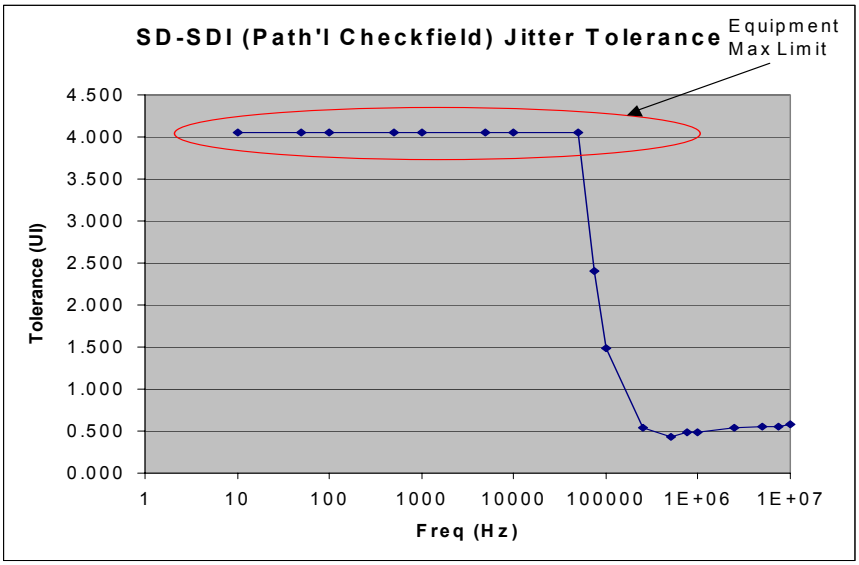
Freq (Hz)	Maximum TG2000 Jitter Modulation Tolerated by HOTLink II Receiver (UI)
10	> 4.05
50	> 4.05
100	> 4.05
500	> 4.05
1000	> 4.05
5000	> 4.05
10000	> 4.05
50000	> 4.05
100000	> 4.05
250000	2.24
500000	0.972
750000	0.675
1000000	0.567
2500000	0.54
5000000	0.567
7500000	0.567
10000000	0.58

Worst-Case

10000Hz the jump in the maximum equipment jitter is due to the limitations of the test equipment and it is not due to the actual roll-off of the PLL.

.

Although the TG2000 reports a certain amount of modulated jitter, the actual jitter entering the Quad Independent Channel HOTLink II Video Board Serial Inputs might be more due to added noise and imperfections in transmission medium and connectors. At the highest modulation frequency, the highest jitter amplitude tolerated by the Quad Independent Channel HOTLink II Video Board receiver as reported by TG2000 data generator was 0.41 UI. This signal's output jitter was measured using a wide bandwidth oscilloscope to determine the actual jitter tolerance as measured by a different piece of equipment, a wide bandwidth oscilloscope (Agilent 86100A). The scope was triggered using the unmodulated signal (jitter free signal) from the TG2000. The resulting eye diagram is shown *Figure 20*. This eye diagram was captured after 10 mins of acquisition. The total peak-to-peak



Worst Case

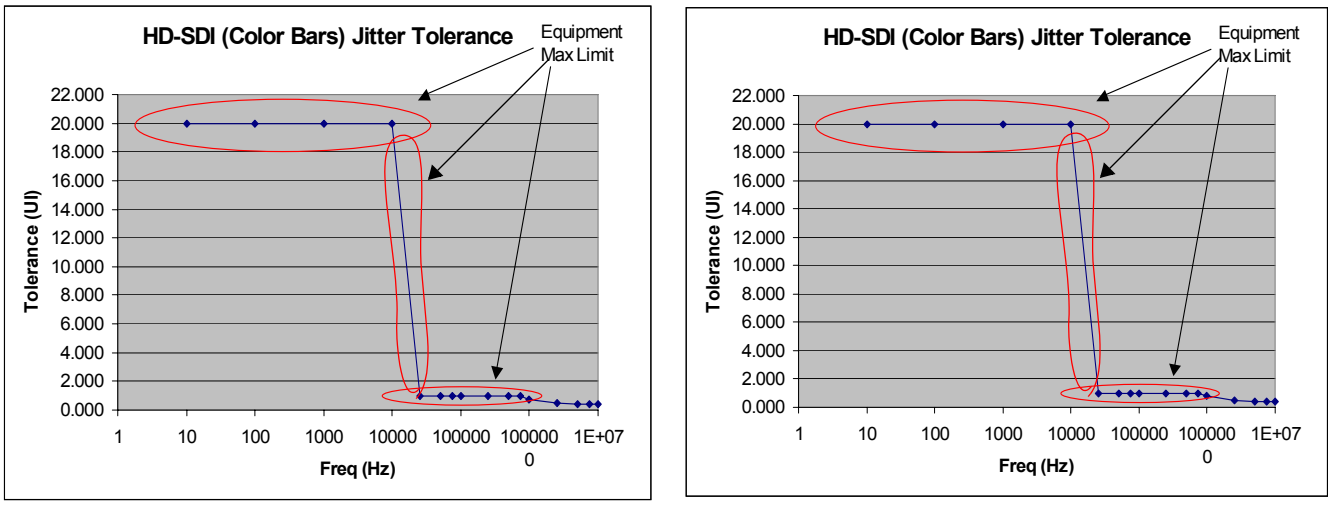
Figure 17. Quad Independent Channel HOTLink II Video Board worst case SD-SDI Jitter Tolerance for SDI pathological checkfield

Table 8. SD-SDI worst case Jitter Tolerance of the Quad Independent Channel HOTLink II Video Board for SDI pathological checkfield

Freq (Hz)	Maximum TG2000 Jitter Modulation Tolerated by HOTLink II Receiver (UI)
10	> 4.05
50	> 4.05
100	> 4.05
500	> 4.05
1000	> 4.05
5000	> 4.05
10000	> 4.05
50000	> 4.05
75000	2.4
100000	1.485
250000	0.54
500000	0.432
750000	0.486
1000000	0.486
2500000	0.54
5000000	0.56
7500000	0.56
10000000	0.58

Worst Case

jitter displayed by the scope is 424ps which is equivalent to 0.63UI of jitter. The deterministic jitter (in this case mostly sinusoidal jitter) can be determined from the distance between the two peaks in the histogram. This value is approximately 228ps which is equivalent to 0.339UI of jitter. Therefore, although TG2000 reports the 0.41 UI of jitter, the jitter measured by Agilent 86100A suggests that the signal contains 0.63UI of p-p jitter (measured for 10 mins) and a deterministic jitter p-p of around 0.339 UI.



Typical **Worst-Case**

Figure 18. HOTLink II Video Board HD-SDI Jitter Tolerance (Left - Typical, Right - Worst case)

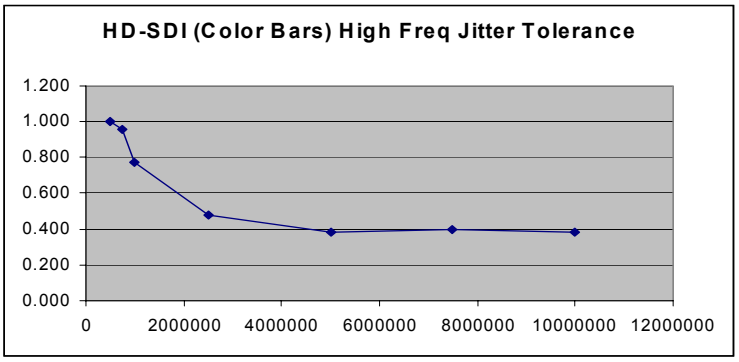


Figure 19. Quad Independent Channel HOTLink II Video Board Receiver HD-SDI Jitter Tolerance (High Frequency Zoomed in)

3.1.4 SMPTE 292M SDI Checkfield

The results of worst case jitter tolerance testing for SMPTE 292M SDI Pathological checkfield pattern is shown graphically in *Figure 21* and tabulated in *Table 10*. The worst case jitter tolerance was measured over temperature (0 -70 Deg Celsius) and over 8 different transceiver channels. For some jitter frequencies, the HOTLink II Receiver was able to recover data with no errors for the maximum jitter that can injected by the TG2000 equipment. This is indicated in the jitter tolerance plots as “Equipment Max” and in the tables with a “>” symbol. Note that as per SMPTE RP192 it is expected that the jitter tolerance for these pathological patterns will be worse than that for Color Bars.For frequencies greater than 10000Hz the jump in the maximum equipment jitter is due to the limitations of the test equipment and it is not due to the actual roll-off of the PLL.

Table 9. HD-SDI Jitter Tolerance of Quad Independent Channel HOTLink II Video Board

Freq (Hz)	Maximum TG2000 Jitter Modulation Tolerated by HOTLink II Receiver (UI)
10	> 20
100	> 20
1000	> 20
10000	> 20
25000	> 1
50000	> 1
75000	> 1
100000	> 1
250000	> 1
500000	> 1
750000	0.96
1000000	0.77
2500000	0.48
5000000	0.39
7500000	0.4
10000000	0.42

Freq (Hz)	Maximum TG2000 Jitter Modulation Tolerated by HOTLink II Receiver (UI)
10	> 20
100	> 20
1000	> 20
10000	> 20
25000	> 1
50000	> 1
75000	> 1
100000	> 1
250000	> 1
500000	> 1
750000	0.96
1000000	0.77
2500000	0.48
5000000	0.38
7500000	0.4
10000000	0.38

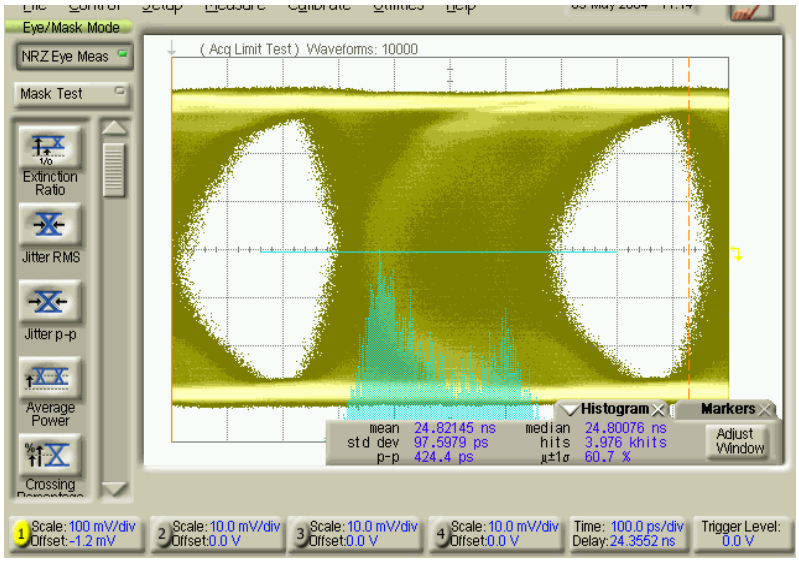


Figure 20. TG2000 Jitter Output tolerated by Quad Independent Channel HOTLink II Video Board Receiver Displayed in a scope (TG2000 set to 0.41 UI of jitter at 10 MHz)

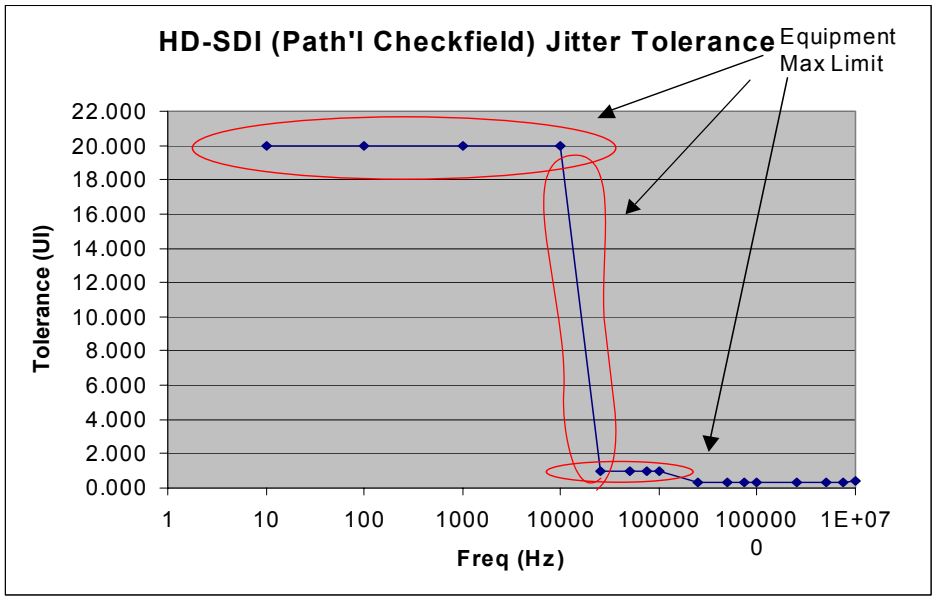


Figure 21. Quad Independent Channel HOTLink II Video Board HD-SDI Jitter Tolerance for SDI Pathological Checkfield (Worst case)

Table 10.HD-SDI Jitter Tolerance of Quad Independent Channel HOTLink II Video Board for SDI Pathological Checkfield

Freq (Hz)	Maximum TG2000 Jitter Modulation Tolerated by HOTLink II Receiver (UI)
10	> 20
100	> 20
1000	> 20
10000	> 20
25000	> 1
50000	> 1
75000	> 1
100000	> 1
250000	0.36
500000	0.3
750000	0.31
1000000	0.34
2500000	0.36
5000000	0.35
7500000	0.36
10000000	0.38

Worst-Case

4. SDI Checkfield Stress Testing using Pathological Patterns

Under normal conditions, the scrambled output has a high transition density with a good ratio of ones to zeros. The pathological conditions are specific high run-length patterns with very low transition density that may be generated by the SMPTE scrambler for specific combinations of the scrambler state and scrambler inputs. Although the probability of the specific inputs and specific scrambler state occurring at the same time in real video data is very low, component vendors are expected to be compliant to the

specified pathological conditions. The pathological serial digital signals are often very challenging to be handled by SDI receivers. SMPTE EG34-1999 documents the pathological patterns that may occur in a SMPTE scrambled system and need to be recovered by SDI receivers with no errors.

SMPTE RP 178 and SMPTE RP 198 document the SDI checkfield data for SMPTE 259M and SMPTE 292M, respectively. The SDI checkfield is the recommended data pattern to test compliance to pathological cases 2 and 3 defined in SMPTE EG34-1999.

The test set-up used to perform this test is the same as the set-up shown for jitter tolerance testing in *Figure 15*. The Tektronix TG2000 is used to generate the desired pathological checkfields at the desired data rate. The module called DVG1 is used for SD-SDI Checkfield generation as per SMPTE RP 178 and the module called HDVG1 is used for HD-SDI checkfield generation as per SMPTE RP 198. The SDI data from the generator is fed to the serial input of a channel of the HOTLink II CYV15G0404DXB Evaluation board. The selected channel is configured to perform a reclocking function. The reclocked serial output of the evaluation board is connected to the inputs of the Tektronix waveform monitor WFM700M. The waveform monitor is capable of displaying the received picture, eye diagram, jitter and CRC errors.

4.1 SMPTE 259M

HOTLink II receivers were tested and verified to be compliant to SD-SDI checkfield testing using the methodology described above. The results of the signal received by the waveform monitor for this test are shown in *Figure 22*.

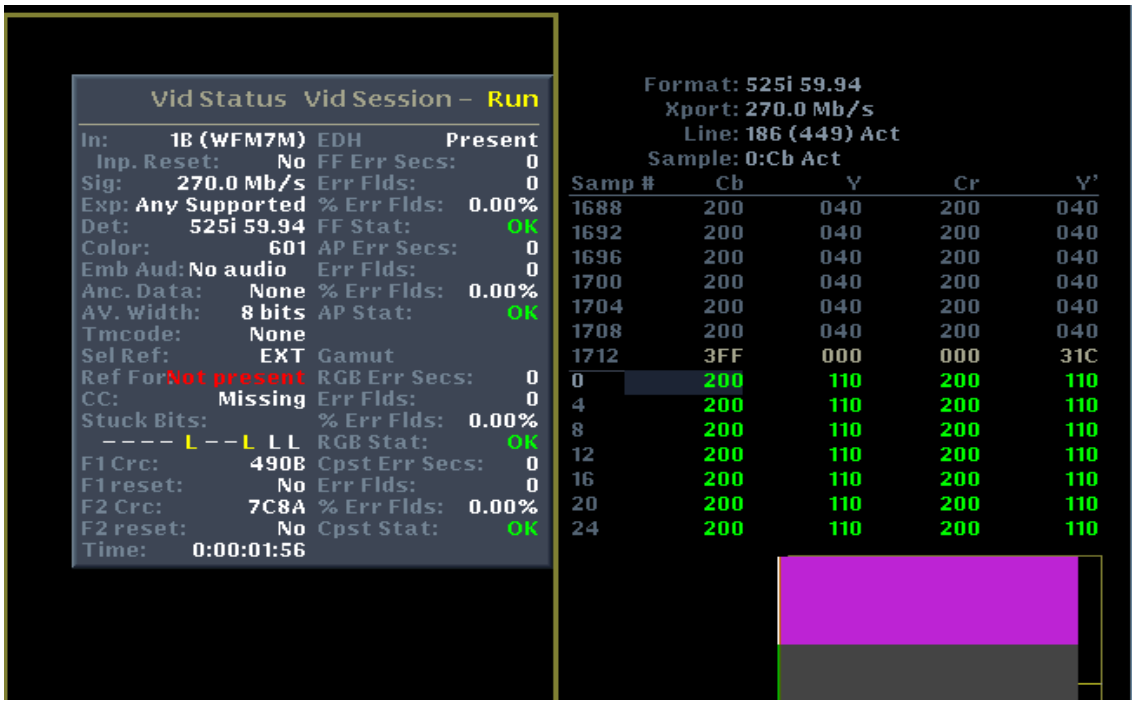


Figure 22. Results of SD-SDI Checkfield Testing from Tektronix WFM700M

4.1.1 Receiving SD-SDI Pathological Patterns through 300m of Belden 8281 Cable

The standard maximum length for SD-SDI links that use Belden 8281 cable as a transmission medium is 300m. One of the concerns for SDI transport is error-free transmission over such a long distance, even for stressful data patterns. The Quad Independent Channel HOTLink II Video Board receiver was tested to recover and reclock SD-SDI checkfield (RP178) received after 300m of Belden 8281 Cable. The reclocked output signal is shown in *Figure 23*.

4.2 SMPTE 292M

HOTLink II receivers were tested and verified to be compliant to HD-SDI checkfield testing using the methodology described in Section 4. The results of the equalized color bar signal recovered by HOTLink II receiver after 100m of Belden 8281 Cable is shown in *Figure 24*.

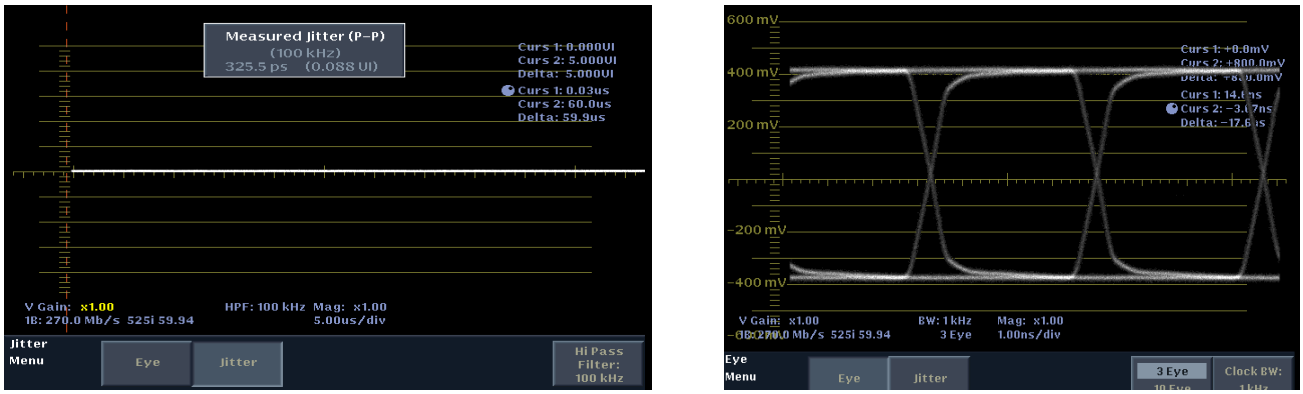


Figure 23. Reclocked SD-SDI checkfield output after 300m of cable

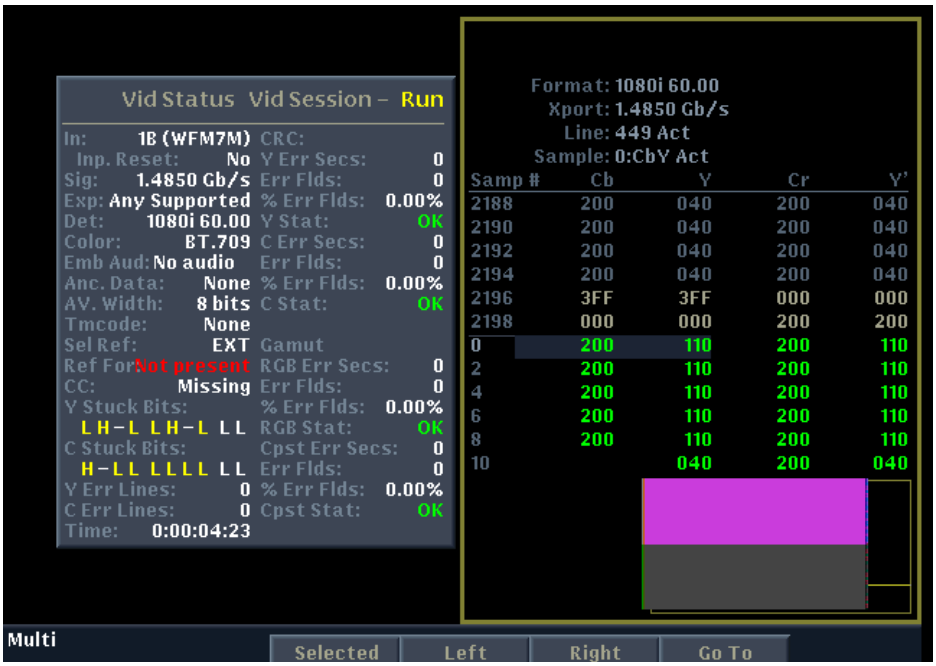


Figure 24. Results of HD-SDI Checkfield Testing from Tektronix WFM700M

4.2.1 Receiving Pathological Patterns through 100m of Belden 8281 Cable

The Quad Independent Channel HOTLink II Video Board receiver was tested to recover and reclock HD-SDI checkfield (RP198) received after 100m of Belden 8281 Cable.The reclocked output signal for color bar data over 100m of cable is shown in *Figure 25*.

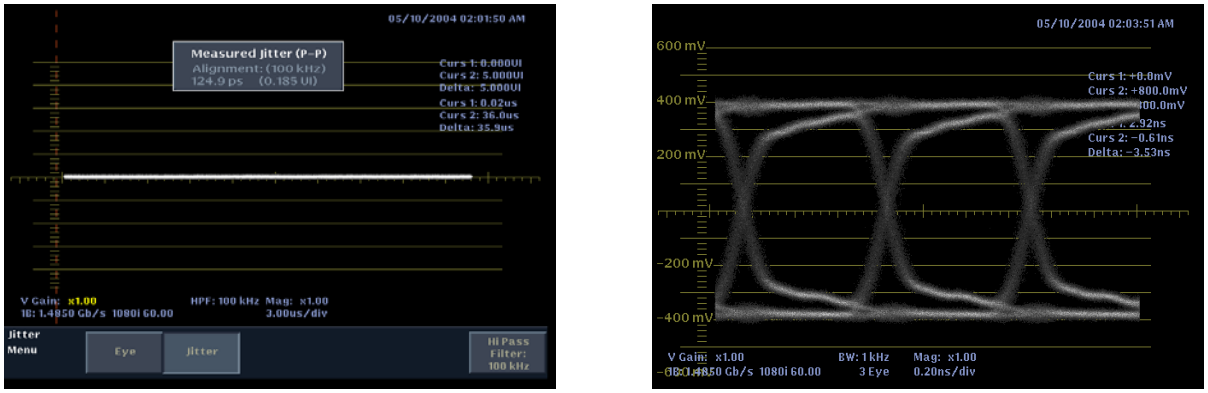


Figure 25. Reclocked HD-SDI checkfield output after 100m of cable

5. Summary

The Cypress HOTLink II family of transceivers is compliant to all jitter and pathological requirements specified by SMPTE for SD-SDI and HD-SDI serial interfaces. The HOTLink II family of devices meets all these requirements in a SDI system (Quad Independent Channel HOTLink II Video Board). The validation was performed with standard test equipment used by the Professional Video industry, thereby ensuring that customers can get the same results with their systems that use the HOTLink II family of transceivers.