This document outlines the critical areas, with respect to layout, that will help to optimize performance of the GS1560 and the GS1532. The high speed sections on both the GS1560 and GS1532 are in the same pin locations. Unless otherwise stated, the layout examples shown apply to both devices.

POWER SUPPLY ISOLATION

The GS1560 requires two voltages, +3.3V and +1.8V. The 1.8V feeds the Digital Core as well as the Analog portions like the serial output and the PLL components. The +3.3V feeds the Digital IO and the power to the on-board regulator for the external VCO. For optimal performance, it is essential that these supplies be isolated to avoid external noise coupling. The supplies can be broken down into four components; +1.8V ANALOG, +1.8V DIGITAL, +3.3V ANALOG and +3.3V DIGITAL.

+1.8V ANALOG: PD_VCC/PDBUFF_GND (3,2), *BUFF_VCC/PDBUFF_GND (4,2) and CD_VCC/CD_GND (20, 22).

+1.8V DIGITAL: CORE_VDD/CORE_GND (37,33 and 64, 68)

+3.3V ANALOG: CP_VCC/CP_GND (1,80).

+3.3V DIGITAL: IO_VDD/IO_GND (41,40 and 53,49 and 61,60).

*This pin is applies to the GS1560 only

ISOLATION METHODS

Because of the noise sensitive nature of the PLL and analog components of the GS1560 and GS1532, the reference design uses an isolation technique to filter power to these sections.

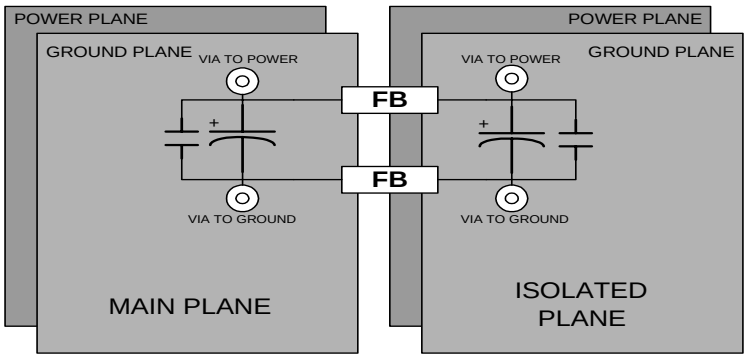

Fig. 1 Power Supply Isolation Method

Figure 1 shows the basic concept behind the technique used. The power plane and ground plane are isolated from the main plane in a “moat”. Power and ground connections to this “moat” are made through ferrite beads (0Ω resistors) which are decoupled on both sides. If possible, running traces across the moat should be avoided. Also, any copper (i.e. Planes or pours on other layers) which bridge the moat should be removed.

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SERIAL DIGITAL OUTPUT

The SDO outputs (available at Pins 23 and 24) are designed to be SMPTE compliant for voltage level, rise/fall time and return loss using the shown compensation network. For minimum variability, keep the components as close and symmetrical as possible. Figure 2 shows the components associated with the Serial Digital Output and Figure 3 shows the component Placement and suggested layout. Ground and power plane voids are placed under the ORL matching network, pull-up resistors and output pins to reduce capacitance and provide better matching to the 75Ω transmission line

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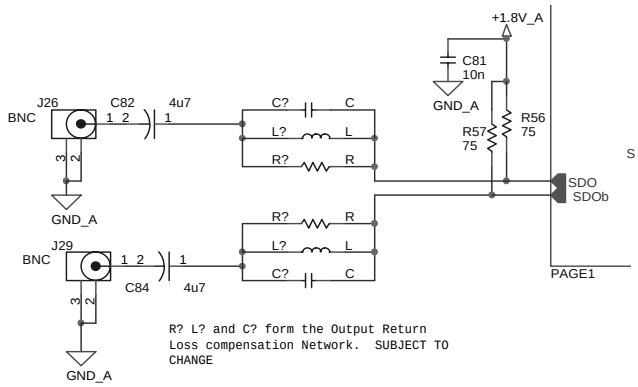

Fig. 2 Serial Digital Output Components

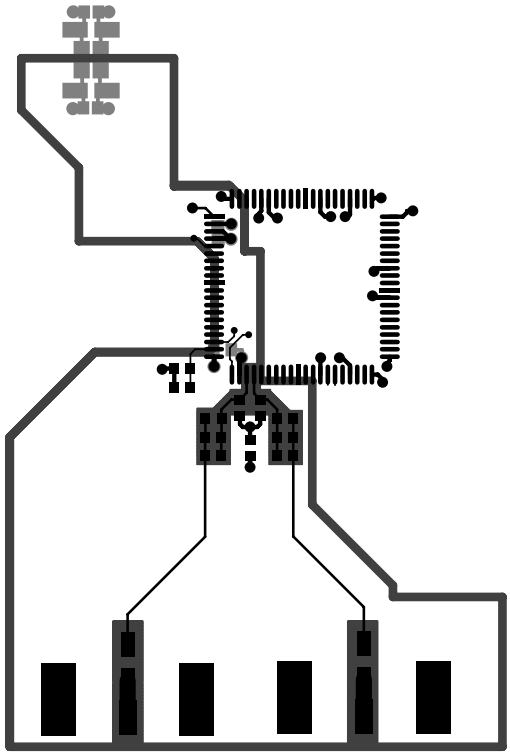

Fig. 3. Serial Output Layout

Table 1 shows the power and ground pins associated with the serial output. BUFF_VCC only applies to the GS1560. On the GS1560, if the serial output is not required, the CD_VCC and CD_GND should still be connected and the SDO_EN/DIS pin should be tied to ground.

TABLE 1. SERIAL OUTPUT AND PHASE DETECTOR POWER SUPPLY PINS

SUPPLY	VDD		GND	
Phase Detector	PD_VCC	3	PDBUFF_GND	2
Buffer	BUFF_VCC	4		
Cable Driver	CD_VCC	20	CD_GND	22

VCO POWER

The GO1525 is the external VCO which connects to the GS1560 and GS1532. VCO_VCC (pin 76) and VCO_GND (pin 75) make up the output of an internal regulator that supplies +2.5V to the GO1525. The +2.5V is derived from the +3.3V ANALOG connection to CP_VCC (pin 1) and CP_GND (pin 80).

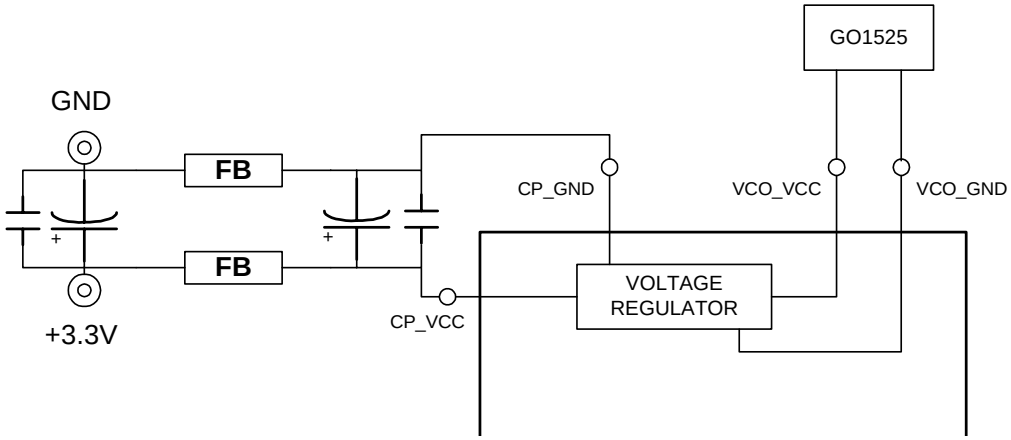

Fig. 3. VCO Power Regulator

Figure 3 shows the connection to the VCO supply and Figure 4 shows a suggested layout. Note that the isolation is complete and the only connection to the VCO plane is through the VCO_VCC and VCO_GND pins.

******DO NOT EXTERNALLY APPLY VOLTAGES TO THE VCO_VCC AND VCO_GND PINS*****

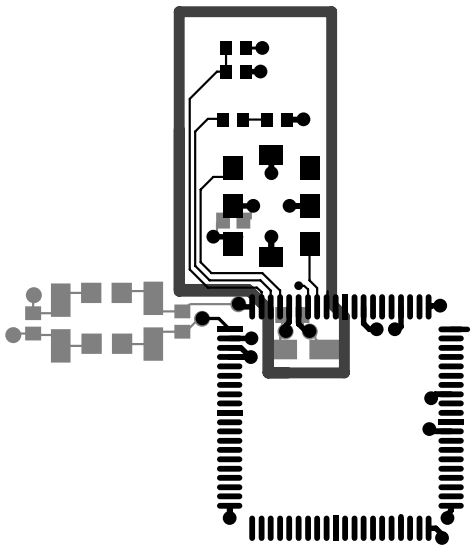

Fig. 4. VCO Section layout

SERIAL DIGITAL INPUTS (GS1560 ONLY)

The GS1560 has two sets of serial inputs. They are designed to interface to the GS1524 Multirate SDI Adaptive Cable Equalizer. Since the GS1524 is a +3.3V device and the inputs to the GS1560 are +1.8V, AC coupling using a 4.7uF capacitor (with polarity towards the Equalizers outputs) will be required to meet the common mode requirements of the GS1560. On board termination for each input is provided; TERM1 (pin 7) for input 1 and TERM2 (pin 16) for input 2. These termination pins should be connected to GND through a 10nF capacitor. Each input also has a $\overline{CD}$ input. This connects to the GS1524's $\overline{CD}$ output, allowing the GS1560 to sense a valid signal at the inputs. Figure 5 shows the suggested layout

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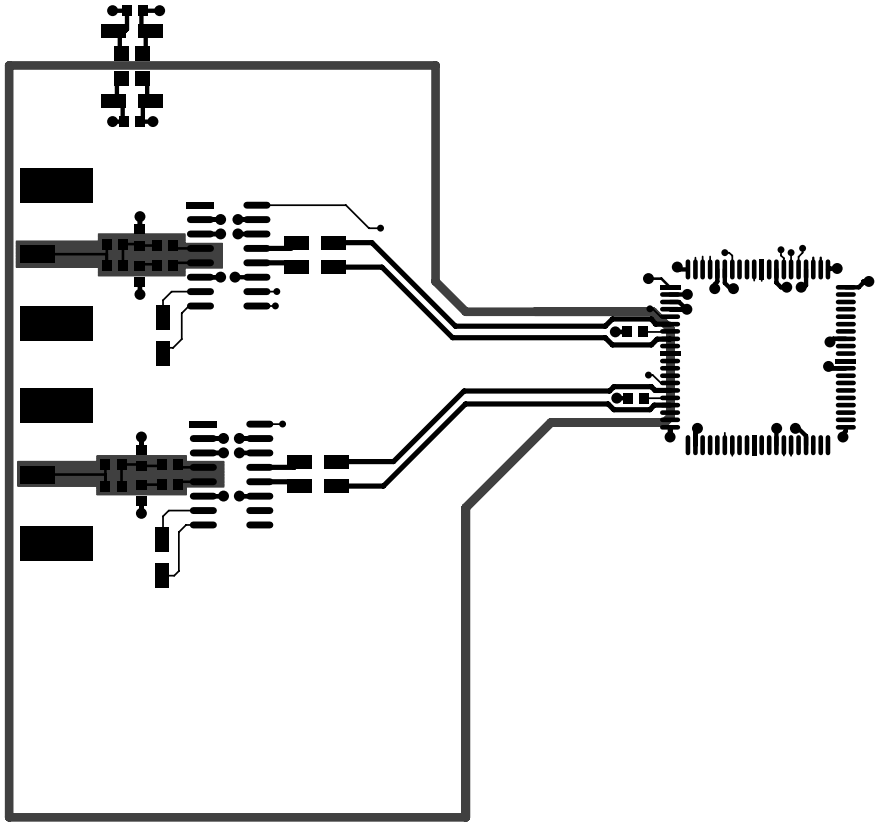

Fig. 5. Input Interfacing Layout

DIGITAL CORE AND I/O SUPPLIES

The digital functions of the GS1560 and the GS1532 require +1.8V at the CORE_VDD/CORE_GND pins and +3.3V at the IO_VDD/ IO_GND pins. These pins are much less sensitive to power supply noise and do not require special Isolation techniques. However, a 1µF capacitor in parallel with a 10nF should be placed at between each of the the IO_VDD and IO_GND to help reduce switching noise. Figures 6 and 7 show the complete layout for the GS1560 and GS1532

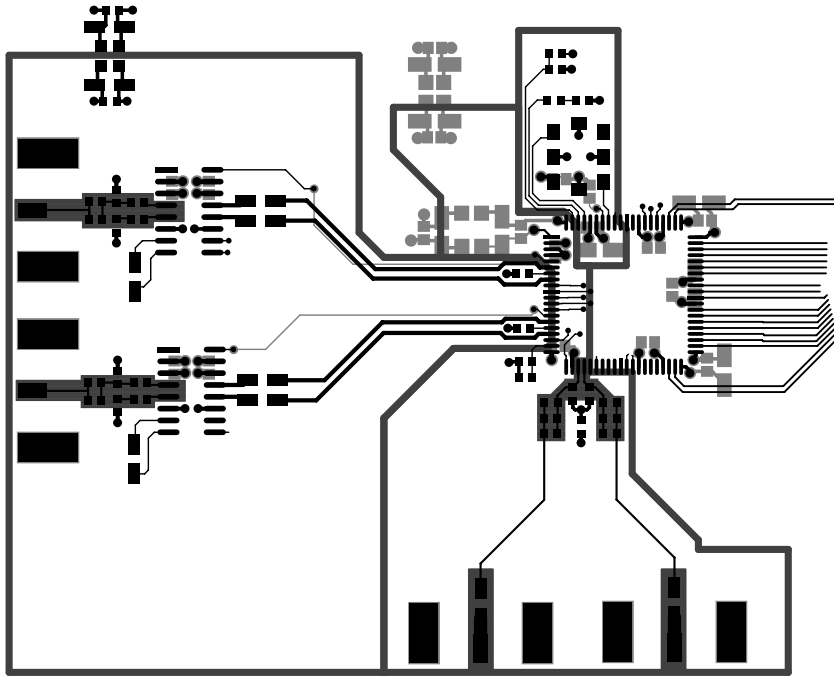

Fig. 6. GS1560 layout

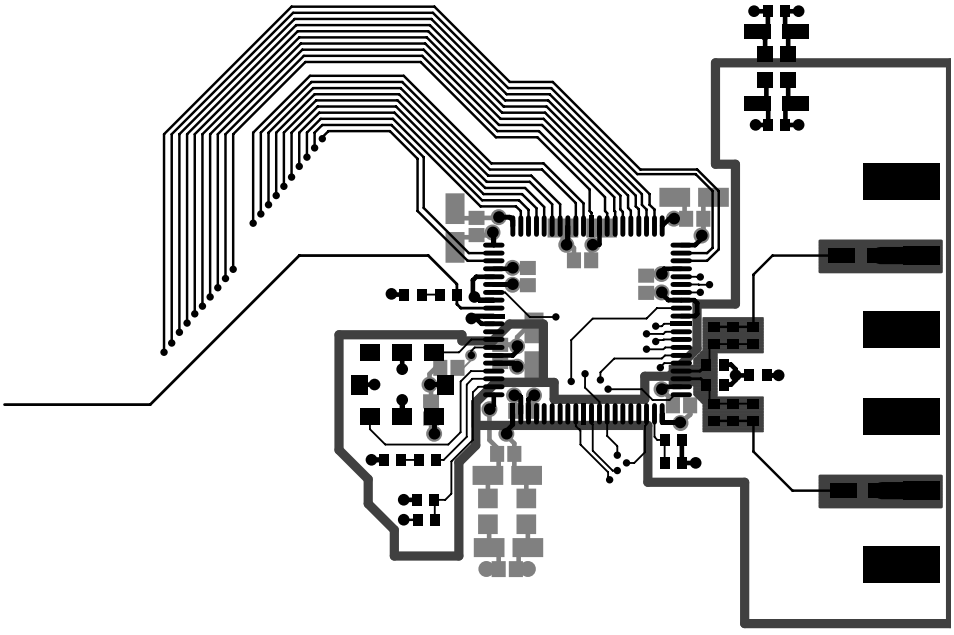

Fig. 7. GS1532 layout

LOOP BANDWIDTH OPTIMIZATION

Nominal Loop bandwidth is set in the GS1560 by a series RC to ground at CP_CAP (pin 78). A nominal loop bandwidth if 1.4 Mhz can be acheived by using 0 ohms for R and 2.2nF (+/- 5%) for C

Both the GS1560 and the GS1532 have a pin called LBCONT (pin 79) which is used to set the loop bandwidth of the device. With the GS1560, a resistor from LBCONT to ground serves to increase the loop bandwidth. For the GS1532, a resistor from LBCONT to VCC serves to decrease the loop bandwidth. In both cases, a 1nF decoupling capacitor is needed (from LBCONT to GND) to minimize noise coupling).

For further optimization, a resistor from LBOCONT to CP_CAP is required. Currently this resistor should be left open. This is a provision for future optimization.

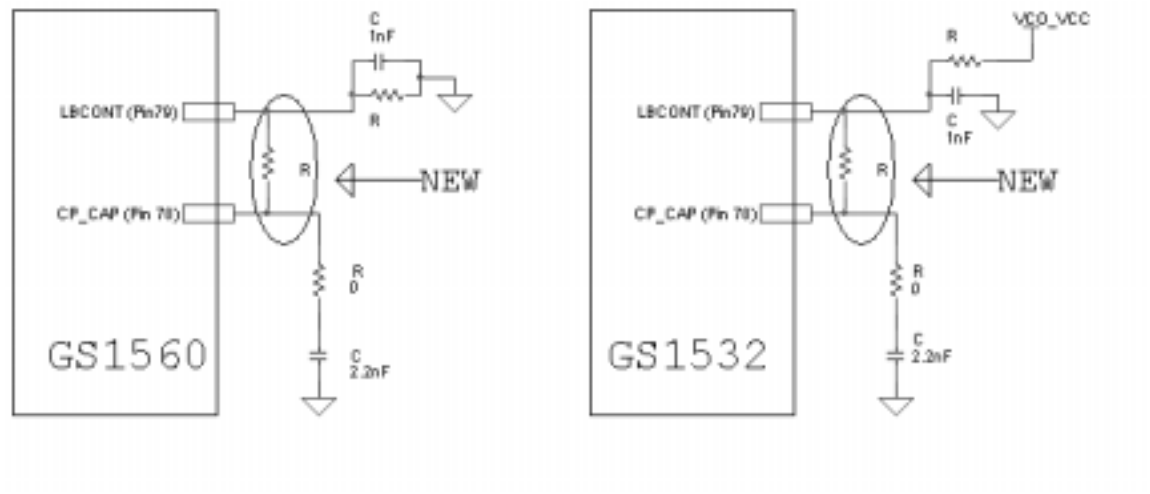

Fig. 8. Components for Loop Bandwidth Optimization.