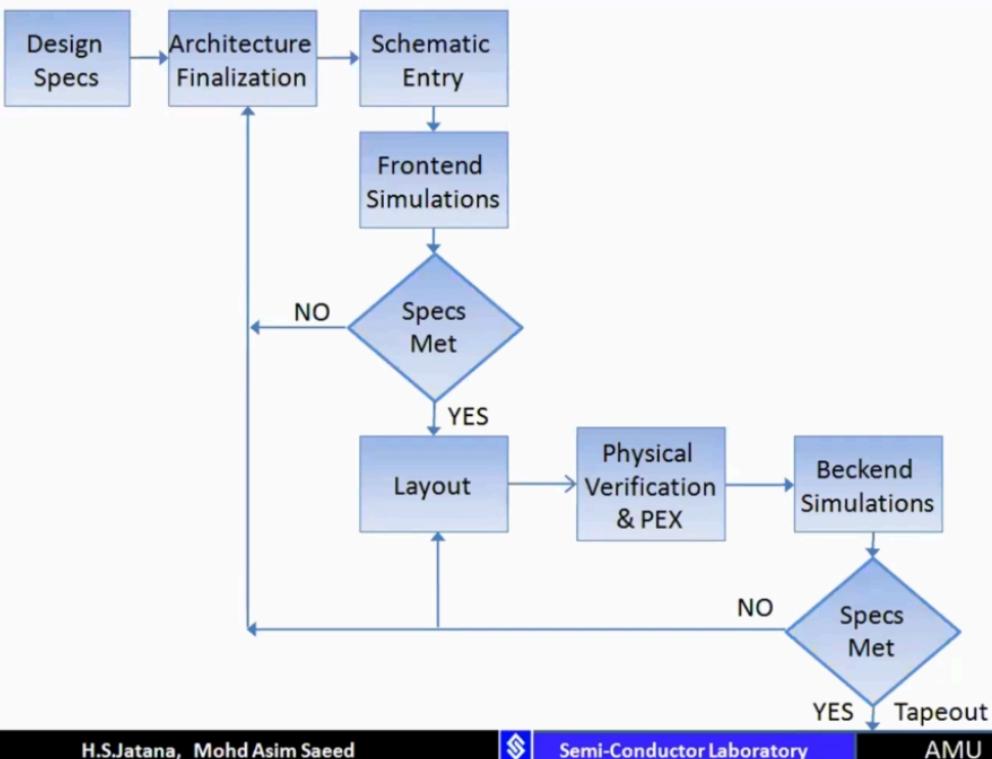


## Analog Design Flow

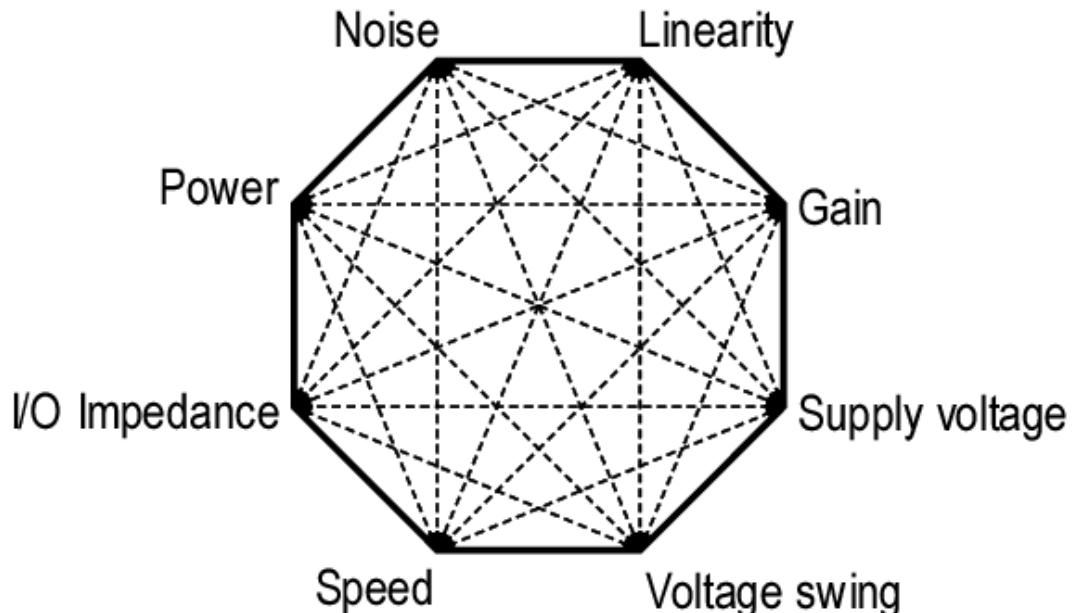


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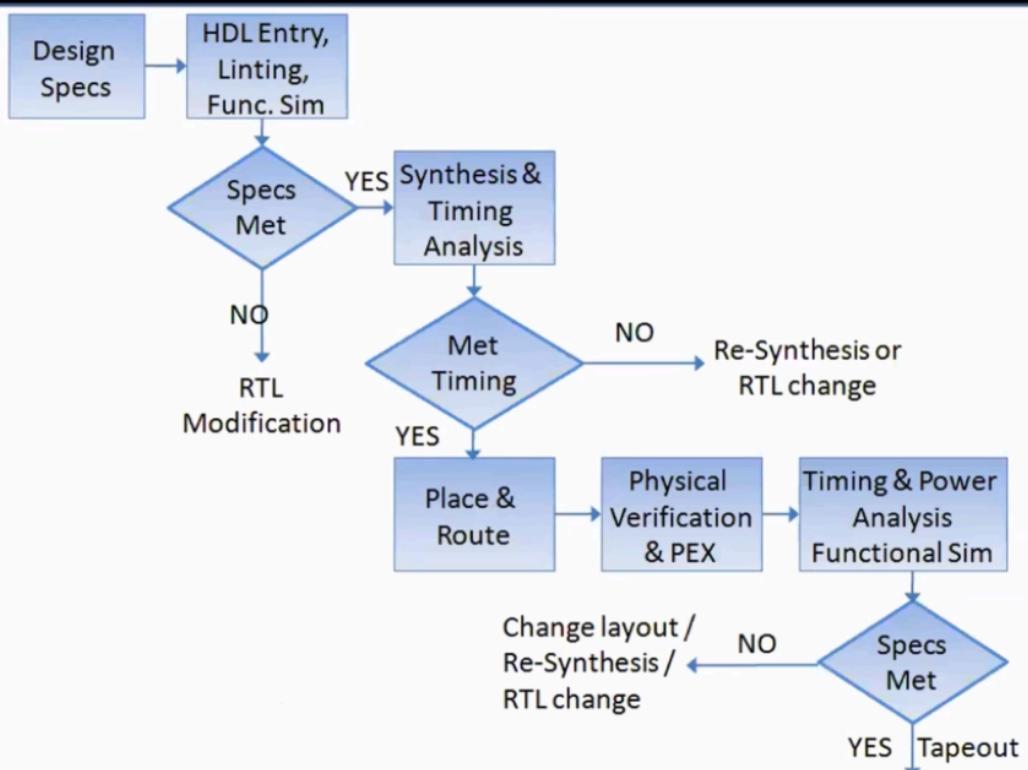
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The above octagon is decided upon and then architecture finalization takes place

## Digital Design Flow



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## IC Design EDA Tools

S. No.	IC design unit activities	EDA Vendor and Tool		
		Synopsys	Cadence	Mentor
1	Library Characterization	Liberty NCX		
2	Verilog / VHDL Simulation	VCS		
3	Design Synthesis	Design Compiler		
4	Placement and Routing	IC Compiler		
5	Timing Analysis	Prime Time		
6	Power Analysis	Prime Time - PX		
7	Signal Integrity Analysis	Prime Time - SI		
8	IR Drop Analysis	Prime Rail		
9	ATPG	TetraMax		
10	Netlist Entry	Hspice		
11	Schematic Editing		Virtuoso SE	
12	Layout Editing		Virtuoso LE	
13	Design Simulation	Hspice		
14	Mixed Signal Simulation	VCS - Hspice		
15	Fast Circuit Simulation	XA		
16	DRC , ERC & LVS			Calibre
17	Parasitic Extraction			Calibre xRC

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The SCL18 SL process supports 4 metal layers with CMOS devices of dual gate oxide thickness:

**Core CMOS:**

1.8V transistors ( $Tox=40A^\circ$ ), with two  $V_t$  options:

- Standard  $V_t$  for general-purpose applications.
- High  $V_t$  (low leakage) for low power applications.
- 1.8V Native transistors.

**I/O:**

- 3.3V transistors ( $Tox=70A^\circ$ ).
- 3.3V Native transistors.
- 3.3 V transistors can also be used for analog design.

**Storage Temperature**

-40°C to +150°C

**Operating Junction  
Temperature**

-40°C to +150°C

VDD	Operational Voltage Limits	Absolute Max Rating
1.8V	1.8V +/-10% < 1.98V	2.2V
3.3V	3.3V +/-10% < 3.63V	4.3V

## General Cross-section in 0.18 um



## General Cross-section in 0.18 um

S. No.	Dielectric Layer	Comments	Thickness
1	Pass	Passivation Nitride	0.3
2	IMD-Last	Metal Last Dielectric2	0.8
3	ML	Metal Last Dielectric1	0.84
4	D-Last	Via Last Dielectric	0.8
5	IMD3	M3 Dielectric	0.54
6	D3	Via 3 Dielectric	0.82
7	IMD2	M2 Dielectric	0.54
8	D2	Via 2 Dielectric	0.82
9	IMD1	M1 Dielectric	0.54
10	D1	Contact Dielectric	0.67
11	Poly	Gate	0.2

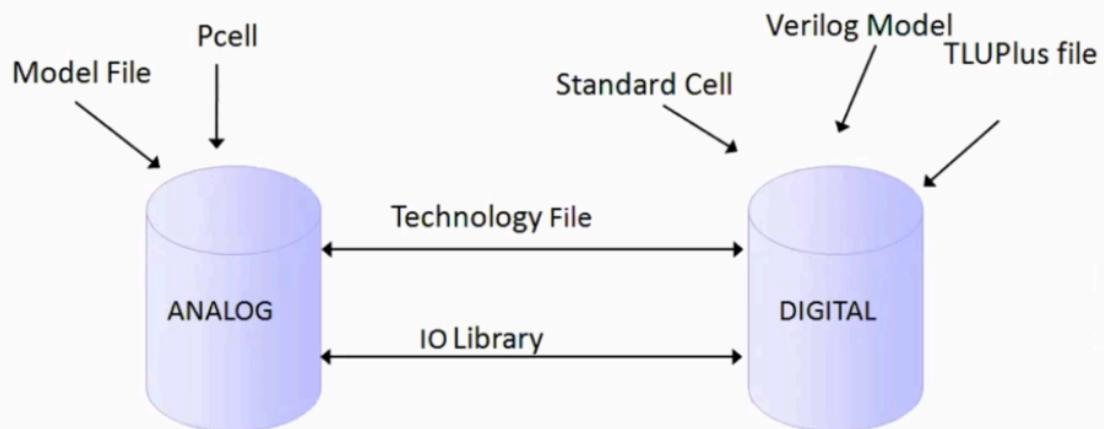
## General Cross-section in 0.18 um

Metal Layer	Width (μm)	Spacing (μm)	Thickness (μm)	Sheet Resistance (Ω/□)	Max Current @125 C (μA)
M1	0.23	0.23	0.54	0.08	154.1
M2	0.28	0.28	0.54	0.08	187.6
M3	0.28	0.28	0.54	0.08	187.6
M4	0.44	0.46	0.84	0.04	472.2

## Process Design Kit

- A process design kit (PDK) is a collection of verified data files that are used by a set of custom IC design EDA tools to provide a complete analog/mixed-signal/RF design flow
- These data files include schematic symbols, SPICE models, Parameterized Cells (PCELLS), DRC/LVS runsets, parasitic extraction runsets, and scripts that run by the EDA tools to automate the generation and verification of design data.

## Process Design Kit



## Technology File

Store all basic technology definition

- Layer names
- Layer purpose names
- Via definitions
- Stream in/out definitions
- Layer colors and style (display.drf)
- Basic drc (optional)
- Basic electrical parameters (optional)
- Look on tech file from delivery

## Technology File

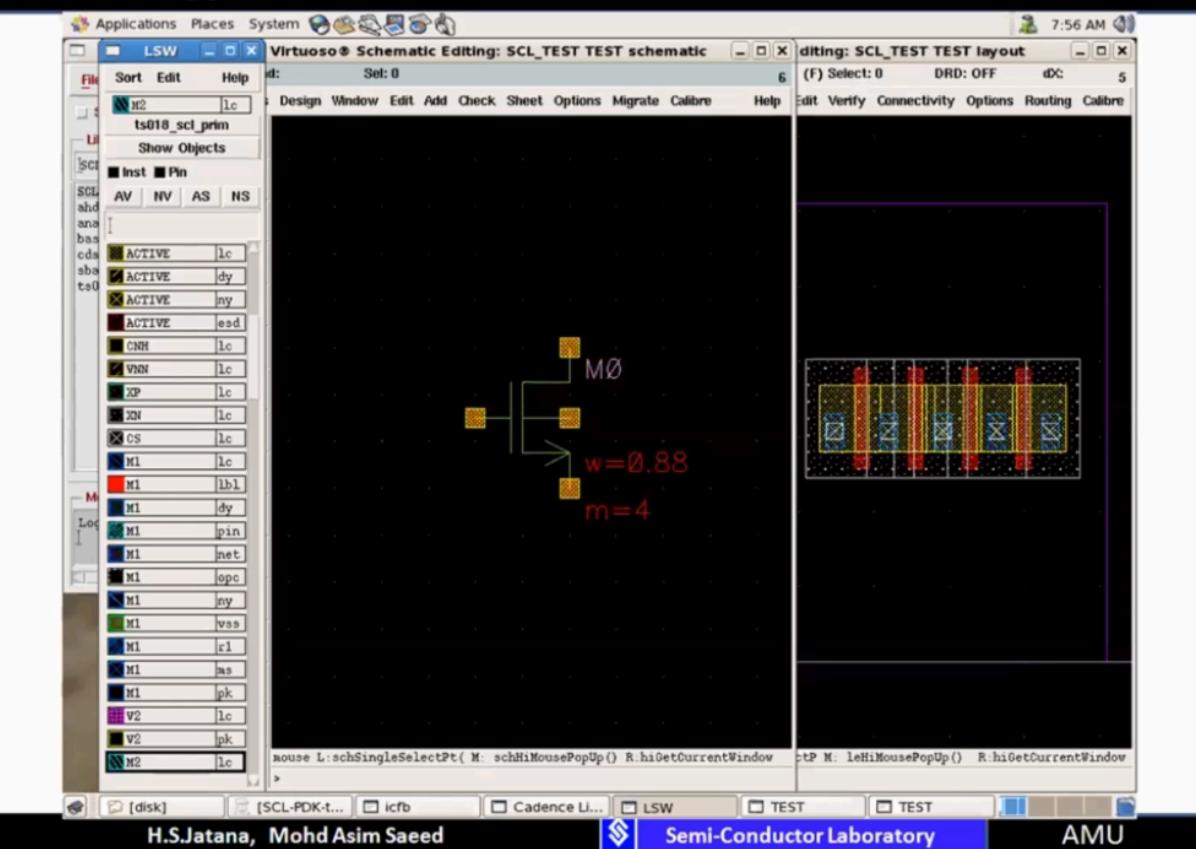
```
techLayers(  
    ;( LayerName          Layer#      Abbreviation )  
    ;User-Defined Layers:  
    ( WP                  2           PWELL)  
    ( WN                  3           NWELL )  
    ( WB                  4           WB )  
    ( GC                  8           POLY )  
    ( ACTIVE              9           ACTIVE)  
    ( XP                  31          PPLUS )  
    ( XN                  32          NPLUS )  
    ( CS                  34          CONT )  
    ( M1                  40          M1 )  
    ( V2                  41          VIA2 )  
    ( M2                  42          M2 )  
) ;techLayers
```

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## Technology File



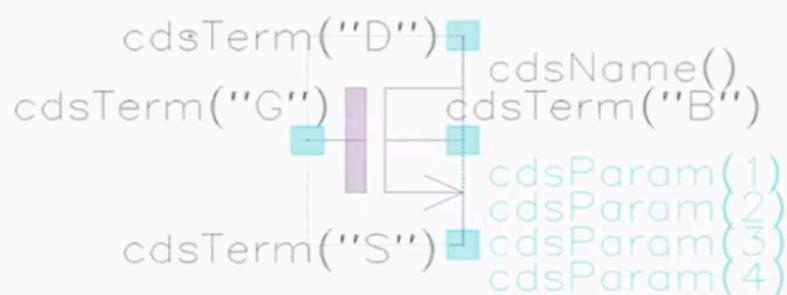
## Pcell (Primitive Cell Library),

- A library (In any tool) that contain view representation of process devices (Mosfets, resistor, capacitors and more).
- Each device is represented in several views for different design flows.
- These views provide a method to parameterize geometric information (Length, width) , electrical information (Capacitance, resistance) and logical information (Terminals, connectivity)
- By defining the special parameters one can get the final representation of the device

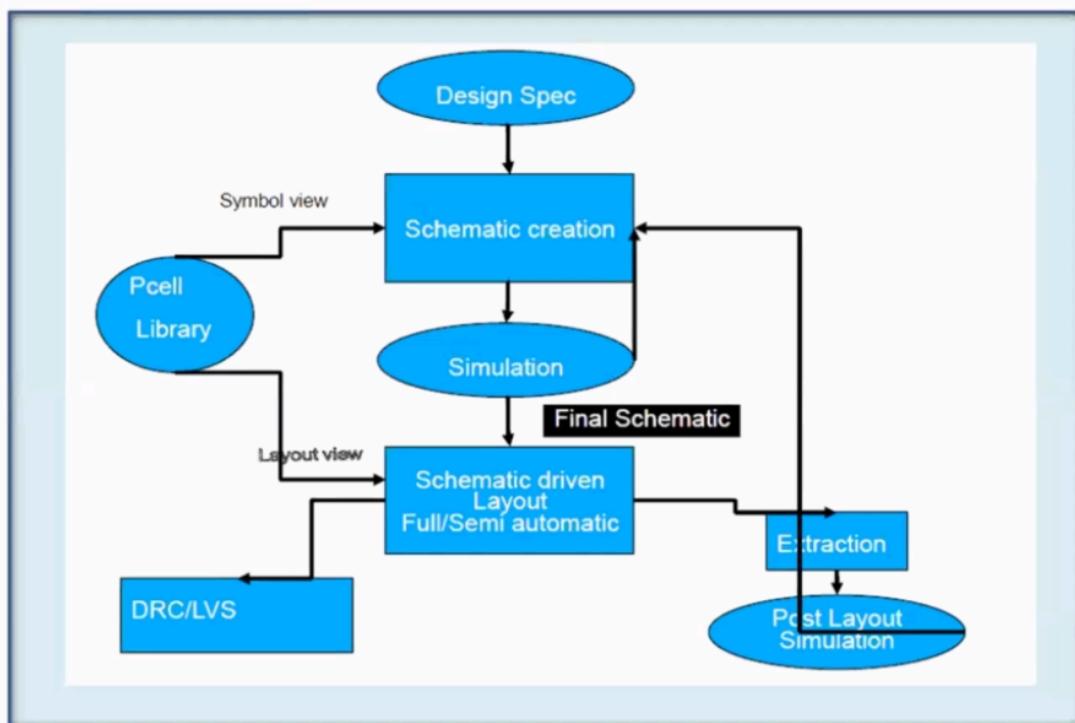
Parameters	Views
Connectivity and pins	symbols
Component description format (CDF)	auCdl, auLvs, hspiceD, hspiceS
Layout drawing of the device	Layout

## Symbol Library

Symbol represent the device in schematic and store pins name and direction.



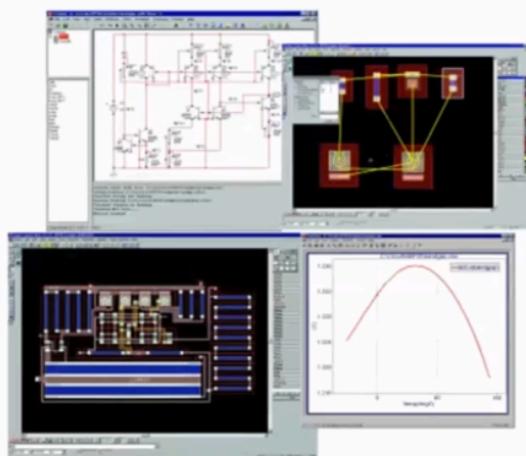
## Schematic Driven Layout using PCells



## Schematic Driven Layout using PCells

At top left is a bandgap circuit captured with Schematic Capture using symbols from the PDK

- Pcells are instantiated by Layout Editor with flight lines
- Cells are placed and wired to make final layout
- SPICE simulates extracted bandgap over temperature



## Model File

- Model file contain all device models with typical, fast and slow process corners.
  - BSIM3V3 used for MOS models.
  - Bin method for MOS devices.
  - Separate file for MOS matching.
- The SPICE models were measured and extracted from the Engineering Vehicle - PYTHON using ICCAP and BsimProPlus Extraction Tools.
- The model valid in the temperature range -40°C to 125°C.

## Bin Method for MOS Tx

- Binned W and L to get better accuracy
- Example of size limits for 9 bin of nmos\_18:

Bin1	$I_{min}=1.65E-07$	$I_{max} = 5e-07$	$w_{min} = 2.05e-07$	$w_{max} = 5e-07$
Bin2	$I_{min}=5.00E-07$	$I_{max} = 1.2e-06$	$w_{min} = 2.05e-07$	$w_{max} = 5e-07$
Bin3	$I_{min}=1.20E-06$	$I_{max} = 1.02e-05$	$w_{min} = 2.05e-07$	$w_{max} = 5e-07$
Bin4	$I_{min}=1.65E-07$	$I_{max} = 5e-07$	$w_{min} = 5e-07$	$w_{max} = 1.2e-06$
Bin5	$I_{min}=5.00E-07$	$I_{max} = 1.2e-06$	$w_{min} = 5e-07$	$w_{max} = 1.2e-06$
Bin6	$I_{min}=1.20E-06$	$I_{max} = 1.02e-05$	$w_{min} = 5e-07$	$w_{max} = 1.2e-06$
Bin7	$I_{min}=1.65E-07$	$I_{max} = 5e-07$	$w_{min} = 1.2e-06$	$w_{max} = 10.02e-05$
Bin8	$I_{min}=5.00E-07$	$I_{max} = 1.2e-06$	$w_{min} = 1.2e-06$	$w_{max} = 10.02e-05$
Bin9	$I_{min}=1.20E-06$	$I_{max} = 1.02e-05$	$w_{min} = 1.2e-06$	$w_{max} = 10.02e-05$

## MOSFETS – Legal Devices

S.No.	Device	Spice Name	Voltage Range
1	N18(1.8V NMOS,Std Vt Transistor)	n18	0 to 1.8V
2	P18(1.8V PMOS,Std Vt Transistor)	p18	0 to 1.8V
3	N18LL (1.8V NMOS,Low Leakage Transistor)	n18llb3	0 to 1.8V
4	P18LL (1.8V PMOS,Low Leakage Transistor)	p18llb3	0 to 1.8V
5	NATLV(1.8V NMOS,Native Vt Transistor)	natlv	0 to 1.8V
6	NHV(3.3V NMOS Transistor)	nhv	0 to 3.3V
7	PHV(3.3V NMOS Transistor)	phv	0 to 3.3V
8	NATHV(3.3V NMOS,Native Vt Transistor)	nathv	0 to 3.3V

## Diodes - Legal Devices

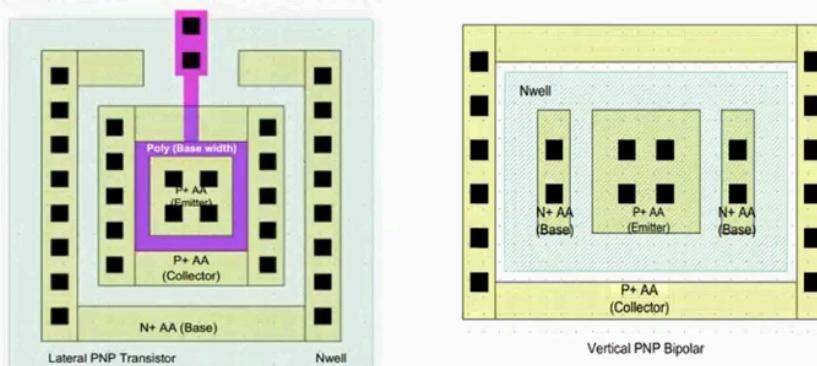
S.No.	Device	Spice Name	Voltage Range
1	Diode N+/Pwell 1.8V	DN18	-1.5V to 10V
2	Diode P+/Nwell 1.8V	DP18	-10V to 1.5V
3	Diode Nwell/Psub 1.8V	DNWELL	-1.5V to 13V
4	Diode N+/Pwell 3.3V	DNH	-1.5V to 10V
5	Diode P+/Nwell 3.3V	DPH	-10V to 1.5V
6	Diode Nwell/Psub 3.3V	DNWELL33	-1.5V to 13V
7	Diode IsoPwell/WB 1.8V	DDWNPW18	-10V to 1.5V
8	Diode WB/Psub 1.8V	DDWNPS18	-1.5V to 13V
9	Diode P+ w/o salicidation/Nwell 1.8V	DPH	-10V to 1.5V
10	Diode N+ w/o salicidation/Pwell 1.8V	DNH	-1.5V to 10V

## Resistors – Legal Devices

S.No.	Device	SpiceName2T	SpiceName3T	Voltage Range
1	HIPO-High Ohmic P-type Poly resistor	RPHPOLY2T	RPHPOLY3T	-8V to 8V
2	NMOP0-Medium Ohmic N-Poly resistor	RNMPOLY2T	RNMPOLY3T	-8V to 8V
3	PMOP0-Medium Ohmic P-Poly resistor	RPMPOLY2T	RPMPOLY3T	-8V to 8V
4	N+ AA Diffusion resistor	RNPLUS2T	RNPLUS3T	0 to 3.3V
5	P+ AA Diffusion resistor	RPPLUS2T	RPPLUS3T	-3.3 V to 0
6	N-Well under AA resistor	RNWELLA2T	RNWELLA3T	0 to 3.3V
7	N-Well under STI resistor	RNWELLSTI2T	RNWELLSTI3T	0 to 3.3V
8	Metal 1 resistor	RM1		-3.3V to 3.3V
9	Metal 2 resistor	RM2		-3.3V to 3.3V
10	Metal 3 resistor	RM3		-3.3V to 3.3V
11	Metal-Top resistor	RML		-3.3V to 3.3V
12	N+LOPO (Salicided Poly) resistor	RNLPOLY2T	RNLPOLY3T	-3.3V to 3.3V
13	P+LOPO (Salicided Poly) resistor	RPLPOLY2T	RPLPOLY3T	-3.3V to 3.3V
14	N+ AA Diffusion (Salicided) resistor	NASR2T	NASR3T	0 to 3.3 V
15	P+ AA Diffusion (Salicided) resistor	PASR2T	PASR3T	-3.3V to 0

## Bipolar Devices

S.No.	Device	Spice Name	Voltage Range
1	1.8V VPPNP 10umX10um	VD10	-3.3V to 3.3V
2	1.8V VPPNP 5umX5um	VD5	-3.3V to 3.3V
3	1.8V VPPNP 2umX2um	VD2	-3.3V to 3.3V
4	3.3V VPPNP 10umX10um	VDH10	-3.3V to 3.3V
5	3.3V VPPNP 5umX5um	VDH5	-3.3V to 3.3V
6	3.3V VPPNP 2umX2um	VDH2	-3.3V to 3.3V



## Capacitors

S.No.	Device	Spice Name 2T	Spice Name 3T	Voltage Range
1	MIM Capacitor Units	CMIM_SQ		-5V to 5V
2	Accumulation capacitor 1.8V(NW)	NWCAP2T	NWCAP3T	0V to 1.8V
3	Accumulation capacitor 3.3V(NW)	NWCAPH2T	NWCAPH3T	0V to 3.3V

S.No.	Device	Typ fF/ $\mu\text{m}^2$	Low Limit fF/ $\mu\text{m}^2$	High Limit fF/ $\mu\text{m}^2$
1	MIM Capacitor Units	1	0.83	1.17
2	Accumulation capacitor 1.8V(NW)	9.15	8.6	9.7
3	Accumulation capacitor 3.3V(NW)	5.10	4.55	5.65

## NMOS Parameters

Process Corner      Typical  
 • Temperature      27 °C  
 • Supply Voltage    1.8 V

- MOS Model = n18
- Wn                = 0.24  $\mu\text{m}$
- Ln                = 0.18  $\mu\text{m}$

Parameter	Value				
	Vds = 1.8 V	Vds = 1.8 V	Vds = 0.1 V	Vds = 0.8 V	Vds = 0.1 V
	Vgs = 1.8 V	Vgs = 0.0 V	Vgs = 1.8 V	Vgs = 0.8 V	Vgs = 0.4 V
IDS(A)	155.52 $\mu$	4.64p	35.76 $\mu$	20.91 $\mu$	171.69 $\mu$
gm (A / V)	138.71 $\mu$	155.18p	18.01 $\mu$	95.54 $\mu$	3.61 $\mu$
gds ( A / V )	5.03 $\mu$	1.94p	324.55 $\mu$	3.86 $\mu$	281.85 $\mu$
Ft (Hz)	63.19G	128.57K	7.31G	44.94G	2.15G
VTH (V)	0.446	0.446	0.454	0.451	0.454
Cgs (F)	0.263f	0.055f	0.178f	0.246f	0.155f
Cgd (F)	0.053f	0.053f	0.183f	0.052f	0.056f

## Memory IP

S No.	SPRAM	DPRAM	Via-ROM
1	SPRAM_1024x36	DPRAM_1024x36	VROM_1024x16
2	SPRAM_16x4	DPRAM_16x4	VROM_128x8
3	SPRAM_2048x36	DPRAM_2048x36	VROM_2048x36
4	SPRAM_32x8	DPRAM_2048x52	VROM_2048x72
5	SPRAM_4096x52	DPRAM_2048x72	VROM_256x16
6	SPRAM_4096x72	DPRAM_2048x8	VROM_4096x36
7	SPRAM_512x24	DPRAM_32x8	VROM_4096x8
8	SPRAM_640x24	DPRAM_4096x36	VROM_512x8
9	SPRAM_8192x36	DPRAM_512x24	VROM_64x4
10	SPRAM_8192x8	DPRAM_640x24	VROM_8192x72

## Static CMOS Inverter

- Process Corner              Typical
- Temperature              27 °C
- Supply Voltage              1.8 V
- $W_p = 0.36 \mu\text{m}$        $W_n = 0.24 \mu\text{m}$
- $L_p = 0.18 \mu\text{m}$        $L_n = 0.18 \mu\text{m}$

S.No.	Parameter	Value
1	Logic Swing	0 - 1.8V
2	Noise Margin ( low input )	0.487V
3	Noise Margin ( high input )	0.849V
4	Rise time	38.38ps
5	Fall time	25.26ps
6	Propagation delay(rising)	66.16ps
7	Propagation delay(falling)	38.41ps
8	Leakage power(high)	15.85pW
9	Leakage power(low)	6.48pW
10	Short Circuit current(rising)	9.51uA
11	Short Circuit current(falling)	6.51uA
12	Capacitive switching power	36.16nW/MHz
13	Area	1.12um*5.6um

## Design Rule Check

- Semiconductor foundry allows the designers to design only the layout pattern on the top view.
- The thickness of layers are fixed by the semiconductor foundry.
- The designers have to design the layout according to design rules which is fixed for each technology
- The purpose of design rule is as follows;
  - Warranty of dimensional precision in fabrication
  - Warranty of precision on electrical characteristics
  - Prevention of latch-up triggered by parasitic bipolar-transistors
  - Design rule violation is automatically detected and reported in DRC (Design Rule Check)
- A semiconductor company accepts only the design that is passed the specified design rules

