```
1  ----------------------------------------------------------------------------------
2  -- Company:
3  -- Engineer:
4  --
5  -- Create Date:    10:31:44 11/01/2018
6  -- Design Name:
7  -- Module Name:    FourRegister - Behavioral
8  -- Project Name:
9  -- Target Devices:
10 -- Tool versions:
11 -- Description:
12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19 ----------------------------------------------------------------------------------
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22
23 -- Uncomment the following library declaration if using
24 -- arithmetic functions with Signed or Unsigned values
25 --use IEEE.NUMERIC_STD.ALL;
26
27 -- Uncomment the following library declaration if instantiating
28 -- any Xilinx primitives in this code.
29 --library UNISIM;
30 --use UNISIM.VComponents.all;
31
32 entity FourRegister is
33    Port( D : in STD_LOGIC_VECTOR(3 DOWNTO 0);
34          CLK : in STD_LOGIC;
35          Q : out STD_LOGIC_VECTOR(3 DOWNTO 0));
36 end FourRegister;
37
38 architecture Behavioral of FourRegister is
39
40 begin
41    process (CLK)
42 begin
43    if (CLK'event and (CLK = '1')) then
44       Q <= D;
45       end if;
46 end process;
47
48
49 end Behavioral;
50
51
```