ECE-2206 Digital Design Lab

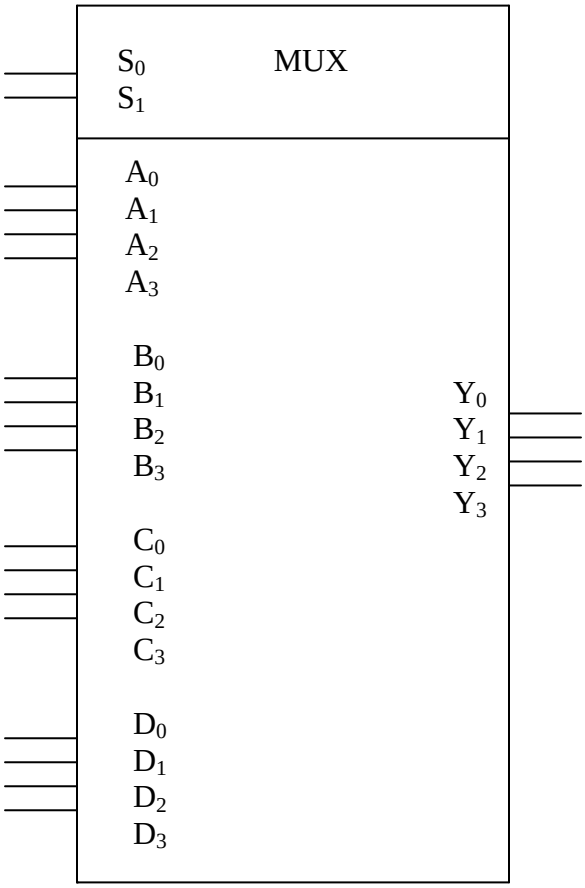
Experiment # 6
Multiplexers and Decoders

Objective:

1) Implementing functions using decoders and multiplexers.
2) Designing complex multiplexers.

Prelab: Please turn in the following parts at the **beginning of lab hour**.
Parts: 1A, 2A, 2B, 3A

1) A) Using 4:1 MUXs , design a multiplexer circuit that multiplexes a set of four, 4-digit input lines to 4-digit output lines. Use S_1 and S_0 as your select lines. (i.e.: If $S_1S_0 = 00$, then $A_3A_2\ A_1A_0 \Rightarrow Y_3Y_2\ Y_1Y_0$)



B) Simulate your design for the following selected combinations of inputs.
(For simulation : Force the inputs and simulate for 5ns.)

S(1:0) = 00	A(3:0) = 0000	B(3:0) = 0001	C(3:0) = 0010	D(3:0) = 0011
S(1:0) = 00	A(3:0) = 0110	B(3:0) = 0001	C(3:0) = 0010	D(3:0) = 0011
S(1:0) = 00	A(3:0) = 1100	B(3:0) = 0001	C(3:0) = 0010	D(3:0) = 0011
S(1:0) = 01	A(3:0) = 0001	B(3:0) = 0101	C(3:0) = 0010	D(3:0) = 0011
S(1:0) = 01	A(3:0) = 0001	B(3:0) = 1101	C(3:0) = 0010	D(3:0) = 0011
S(1:0) = 01	A(3:0) = 0001	B(3:0) = 1111	C(3:0) = 0010	D(3:0) = 0011
S(1:0) = 10	A(3:0) = 0001	B(3:0) = 0001	C(3:0) = 0100	D(3:0) = 0011
S(1:0) = 10	A(3:0) = 0001	B(3:0) = 0001	C(3:0) = 0110	D(3:0) = 0011
S(1:0) = 10	A(3:0) = 0001	B(3:0) = 0001	C(3:0) = 1001	D(3:0) = 0011
S(1:0) = 11	A(3:0) = 0001	B(3:0) = 0001	C(3:0) = 0010	D(3:0) = 1010
S(1:0) = 11	A(3:0) = 0001	B(3:0) = 0001	C(3:0) = 0010	D(3:0) = 1100
S(1:0) = 11	A(3:0) = 0001	B(3:0) = 0001	C(3:0) = 0010	D(3:0) = 0011

2) Realize the following function using:

$$F(A,B,C,D) = \sum (1 , 3 , 6 , 7 , 13 , 15)$$

A) An 8:1 MUX (Additional gates may be required.)

B) A 4:1 MUX (Additional gates may be required.)

C) Simulate your designs for all possible combinations of the inputs.
(For simulation : Use clock and assign 16ns for (bit3)
8ns for (bit2)
4ns for (bit1)
2ns for (bit0)
Simulate for 20 ns.)

D) Download and test your designs on the board.

E) Which one of the two circuits is more efficient? Give reasons for your answer.

3) A) Implement the following functions using a 4 to 16 decoder.
(Additional gates may be required.)

$F_0 (A, B, C, D) = \sum m(0 , 14, 15)$

$F_1 (A, B, C, D) = \sum m(1, 13 , 15)$

$F_2 (A, B, C, D) = \sum m(2 , 12 , 15)$

$F_3 (A, B, C, D) = \sum m(3, 11 , 15)$

$F_4 (A, B, C, D) = \sum m(4 , 10 , 15)$

$F_5 (A, B, C, D) = \sum m(5 , 9 , 15)$

$F_6 (A, B, C, D) = \sum m(6 , 8 , 15)$

$F_7 (A, B, C, D) = \sum m(7 , 15)$

B) Simulate your design for all possible combinations of the inputs.
(For simulation: Use clock and assign 16ns for MSB (bit3)
8ns for (bit2)
4ns for (bit1)
2ns for (bit0)
Simulate for 20 ns.)

C) Download and test it on the board.

Note: Assign F_0 to LD0, F_1 to LD1, …., F_7 to LD7

The Schematics for all circuits and their simulation results should be included in the lab report.