```
1  ----------------------------------------------------------------------------------
2  -- Company:
3  -- Engineer:
4  --
5  -- Create Date:    14:40:37 10/25/2018
6  -- Design Name:
7  -- Module Name:    MUXfourtoone - Behavioral
8  -- Project Name:
9  -- Target Devices:
10 -- Tool versions:
11 -- Description:
12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19 ----------------------------------------------------------------------------------
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22
23 -- Uncomment the following library declaration if using
24 -- arithmetic functions with Signed or Unsigned values
25 --use IEEE.NUMERIC_STD.ALL;
26
27 -- Uncomment the following library declaration if instantiating
28 -- any Xilinx primitives in this code.
29 --library UNISIM;
30 --use UNISIM.VComponents.all;
31
32 entity MUXfourtoone is
33     Port ( S : in  STD_LOGIC_VECTOR(1 DOWNTO 0);
34
35            A,B,C,D : in  STD_LOGIC_VECTOR(3 DOWNTO 0);
36
37            Y : out  STD_LOGIC_VECTOR(3 DOWNTO 0));
38 end MUXfourtoone;
39
40 architecture Behavioral of MUXfourtoone is
41
42 begin
43
44    with S select
45       Y <= A when "00",
46            B when "01",
47            C when "10",
48            D when "11",
49            "XXXX" when others;
50
51 end Behavioral;
52
53
```