```
1  ----------------------------------------------------------------------------------
2  -- Company:
3  -- Engineer:
4  --
5  -- Create Date:    11:03:25 11/08/2018
6  -- Design Name:
7  -- Module Name:    SelfStartSeq - Behavioral
8  -- Project Name:
9  -- Target Devices:
10 -- Tool versions:
11 -- Description:
12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19 ----------------------------------------------------------------------------------
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22
23 -- Uncomment the following library declaration if using
24 -- arithmetic functions with Signed or Unsigned values
25 --use IEEE.NUMERIC_STD.ALL;
26
27 -- Uncomment the following library declaration if instantiating
28 -- any Xilinx primitives in this code.
29 --library UNISIM;
30 --use UNISIM.VComponents.all;
31
32 entity SelfStartSeq is
33    Port( UD,clk,reset : in STD_LOGIC;
34          Q : out STD_LOGIC_VECTOR (3 DOWNTO 0)
35          );
36 end SelfStartSeq;
37
38 architecture Behavioral of SelfStartSeq is
39
40 signal Qsig,Dsig : std_logic_vector(3 downto 0);
41
42 begin
43 process(clk,reset)
44    begin
45       if(reset='1') then
46          Qsig <= "0001";
47
48       elsif (clk'event and clk='1') then
49          Qsig <= Dsig;
50       end if;
51 end process;
52
53
54 process(Qsig,UD)
55 begin
56 case UD is
57    when '1' =>
```

```
58            case Qsig is
59               when "0001" => Dsig <= "0011";
60               when "0011" => Dsig <= "0101";
61               when "0101" => Dsig <= "0111";
62               when "0111" => Dsig <= "1001";
63               when "1001" => Dsig <= "1011";
64               when "1011" => Dsig <= "1101";
65               when "1101" => Dsig <= "1111";
66               when "1111" => Dsig <= "0001";
67               when others => Dsig <= "0001";
68               end case;
69      when '0' =>
70            case Qsig is
71               when "0001" => Dsig <= "1111";
72               when "1111" => Dsig <= "1101";
73               when "1101" => Dsig <= "1011";
74               when "1011" => Dsig <= "1001";
75               when "1001" => Dsig <= "0111";
76               when "0111" => Dsig <= "0101";
77               when "0101" => Dsig <= "0011";
78               when "0011" => Dsig <= "0001";
79               when others => Dsig <= "0001";
80               end case;
81      when others => null;
82      end case;
83      Q <= Qsig(3 downto 0);
84   end process;
85   end Behavioral;
86
87
```