ECE-2206 Digital Design Lab

Experiment # 4
Full Adder

Objective: To simplify circuits using logic minimization techniques.

Prelab: Develop a full adder

A full adder has three inputs (A, B, CIN) and two outputs (SUM, COUT).

```
                A
                B
            + CIN
              -----
COUT         SUM
```

Use K-Map's to develop a 2 level and-or circuit for implementing a full adder.

Turn in a copy of your design at the beginning of the lab hour. (Truth Table and K-maps)

Experiment:

1.

A. In Xilinx ISE draw your design in a schematic file. Save the schematic.

B. Compile the schematic (highlight your schematic file and click on the **Synthesize** in the **Processes** window) and correct errors if there are any.

C. Simulate the circuit for all input combinations (Behavioral simulation). Check your simulation results to make sure your design is working accurately. Print the simulation results. A copy of the simulation results should be submitted with your lab report.

D. Simulate the circuit for all input combinations with time delays included (Post-Route Simulation). Print the simulation results. A copy of the simulation results should be submitted with your lab report. (Step 20 from lab #3)

E. Next follow the necessary steps to download your design to the board. Assign the inputs to the switches and the output to the LEDs available on the board.

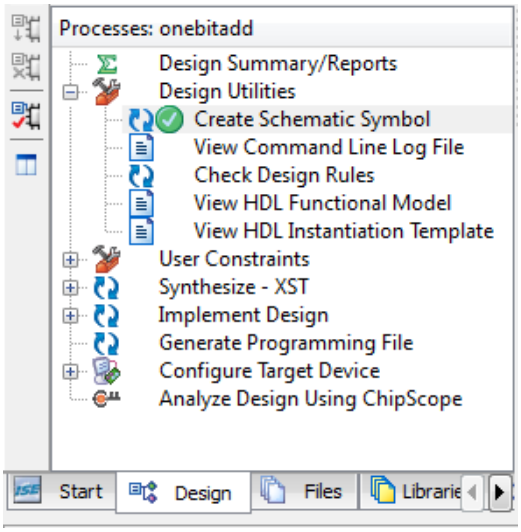
2. Extend one of you single bit full adder circuits to a 3 bit adder with a single carry in and a carry out. This will produce a 4 bit result.

A. To accomplish this, it is necessary to create a schematic symbol for your one-bit-adder.

Steps for Creating a Schematic Symbol:

I) In the **Design** window highlight your schematic file. (one-bit-adder file)

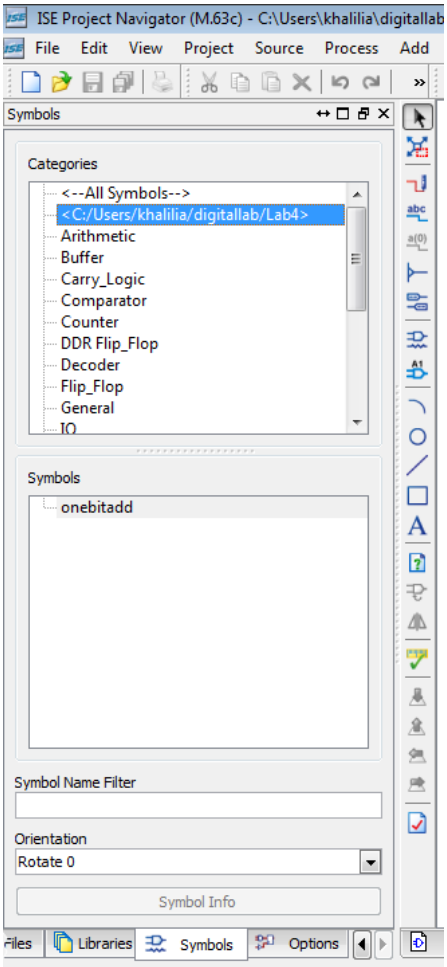
II) In the **Processes** window, expand **Design Utilities and** double click on **Create Schematic Symbol.**



B) Steps for designing the Three bit Full Adder:

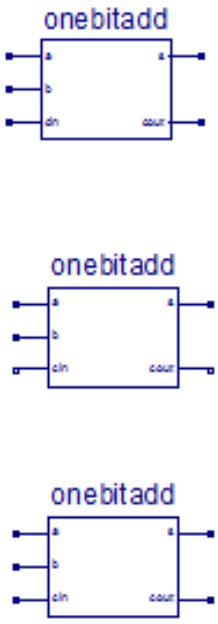
I) Create a new schematic for the three-bit-adder (Project =>new source => schematic =>…).

II) Click on **Symbols** in your **schematic** window then, select your design directory in the **Categories** window. (Make sure **Symbol Name Filter** is blank). A symbol with the same name as your schematic (one-bit-adder) should be present.

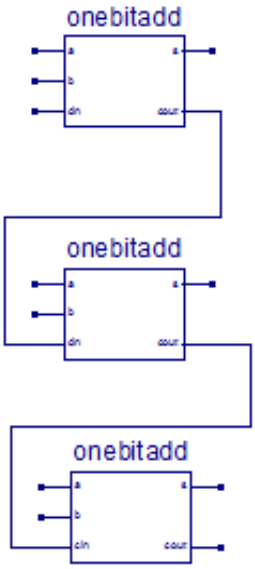


III) Place 3 copies of your one-bit-adder symbol in the new schematic.

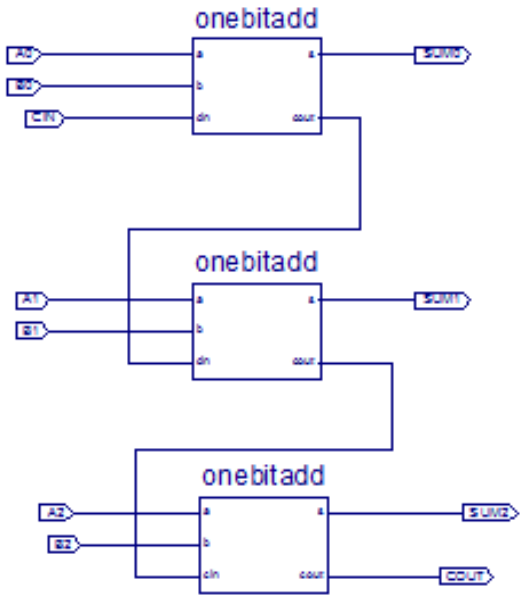
NOTE1: When the software makes the schematic symbols, it may rearrange the order of the inputs or outputs on the schematic symbol. Therefore, make sure you are accessing the intended input or output.



IV) Connect COUT0 to CIN1 and COUT1 to CIN2, shown below.



V) The schematic has 7 inputs (out of 9 inputs) and 4 outputs (out of 6 outputs) that should be connected to I/O markers. Add the I/O markers and save your schematic. You should have a schematic diagram similar to the following diagram.



VI) Compile and simulate your three bit adder for the following input combinations. Check your simulation results for accuracy. A copy of the simulation results should be submitted with your lab report.

Force and run 5ns for each combination.

CIN	$A_2A_1A_0$	$B_2B_1B_0$
0	000	000
0	001	010
0	011	011
0	011	100
0	011	101
0	001	110
0	110	101
0	111	111
1	111	111

VII) Simulate the three bit adder with time delays included (Post-Route). Use only the first four input combinations given in step VI and simulate each combination for 20ns. A copy of the simulation results should be submitted with your lab report.

VIII) Download it to the board and test your circuit. (Repeat steps 17-19 of Exp. #3)

Question: In your report state your observations of time delays in both one-bit adder and three-bit adder.

Note: The Schematics for both circuits and their simulation results should be included in the lab report.