ECE 3216: Computer Systems Design Lab

Lab 6: ISA Write

Anthony Lam, Robert Campbell

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Objective:

The goal of this lab is to use simulated digital logic on an ISA card to generate a programmable clock frequency with a multibit clock. Through checking if an ISA write is being performed to an address, and latching it as necessary, an ISA attached x86 IO register will be essentially created.

Equipment:

-Xilinx ISE

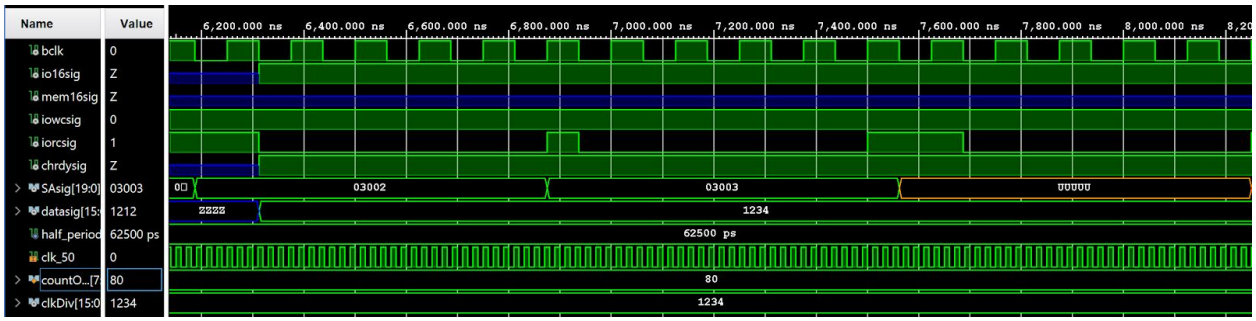
-MESA 4i38

Procedure:

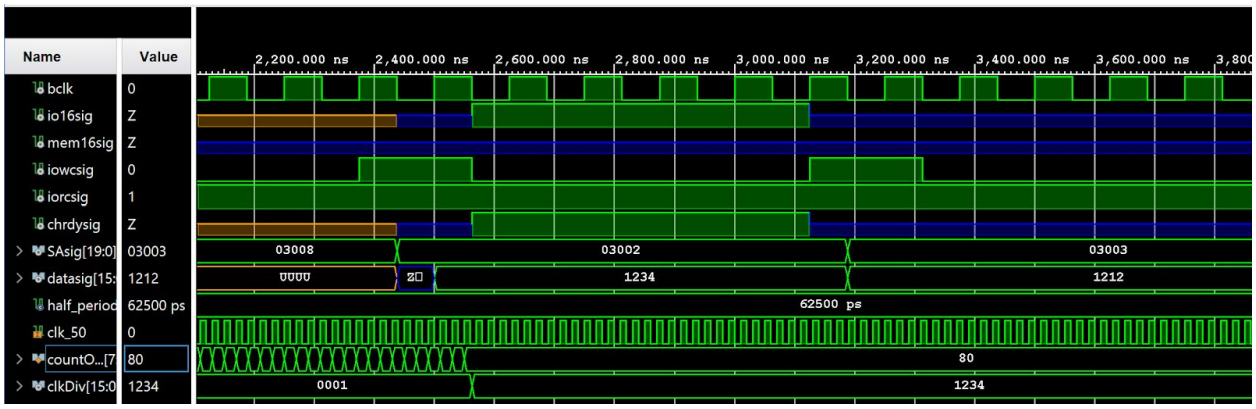
VHDL was written to implement an 8 bit variable frequency with a 50% duty cycle using the 50MHz clock on the MESA 4i38. The design was then verified in a behavioral simulation.

Data and Observations:

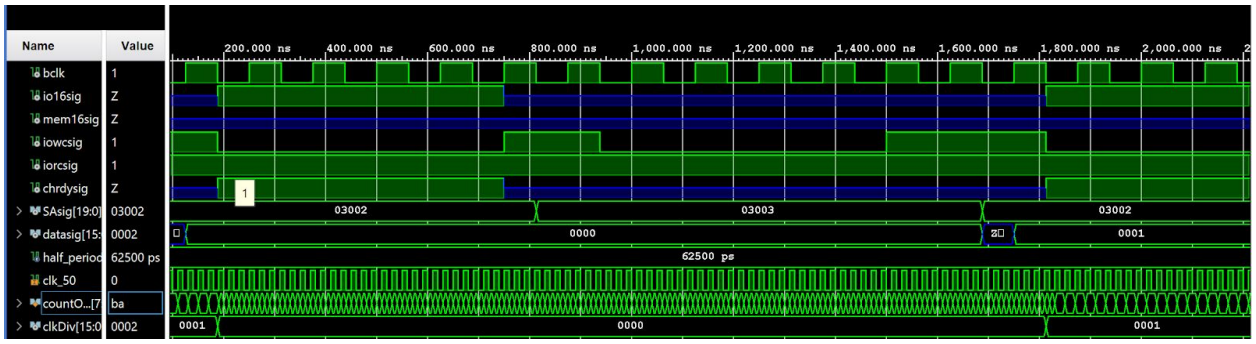
Counter IO Read



Counter IO Write



50MHz-25MHz



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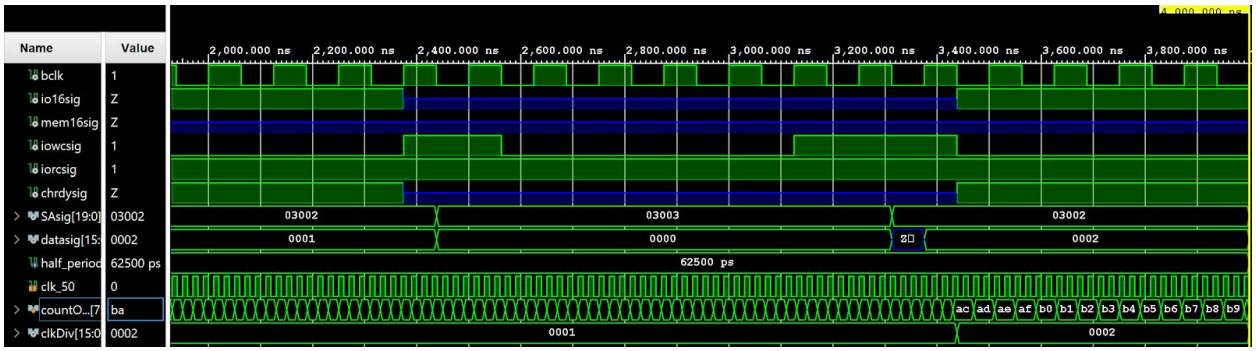

Analysis and Discussion:

This lab was successful. The waveforms from the program are shown above, verifying that the clock is performing as expected. Analysis is not applicable in this experiment.

Questions:

Discuss the difficulties in choosing a valid IO port on a PC compatible.

> The difficulties of choosing a valid IO port on a PC compatible are that it is not possible to determine the address of individual ISA devices when there are multiple devices connected. Address overlaps can occur because of this.

How did you handle allowing the master clock to be seen on the output, that is, how did you handle dividing the master clock by 1?

> On the rising edge of every master clock, the output was set. This mirrors the clock but subjects it to timing constraints.

Estimate the propagation delay of the longest delay path through your counter. The output files from the Xilinx compiler may help with this endeavor. You may also be able to measure this on the scope but know that the scopes have a 5ns resolution.

Conclusion:

The purpose of this lab was to design a programmable clock placed in ISA IO space, gain familiarity with ISA IOWrite and the signals involved, as well as how to make a counter-as-clock-divider pass a clock through without dividing its frequency. The solution to the last portion was to tie the source clock through as the LSB of the counter. The rest of the design went smoothly after the initial setup of the simulation and once we had a grasp on the sequences the signals needed to go through.