ECE-2206 Digital Design Lab

Experiment # 8
Registers and Register Banks

Objective: Creating registers and register banks in VHDL.

Prelab: Please turn in the following parts at the **beginning of lab hour**.
Parts: 1A , 2A and 2A.a.

Background:

A register is a string of flip-flops all having the same clock line.

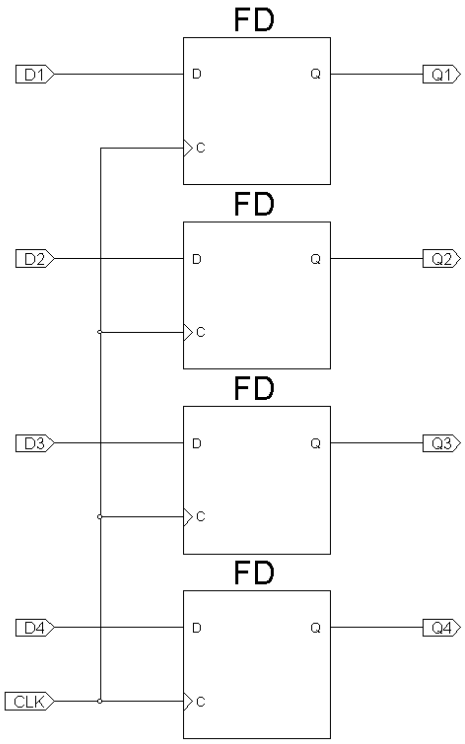

Figure 8-1: Edge Triggered 4 Bit Register

When the clock line goes from low to high the input to the filp-flop is transferred to the output. Circuit diagram in figure 1 is a collection of positive edge triggered flip-flops because the outputs get updated on a low to high transition of the clock line. Negative edge triggered flip-flop can be built by making the output change on a high to low transition of the clock.

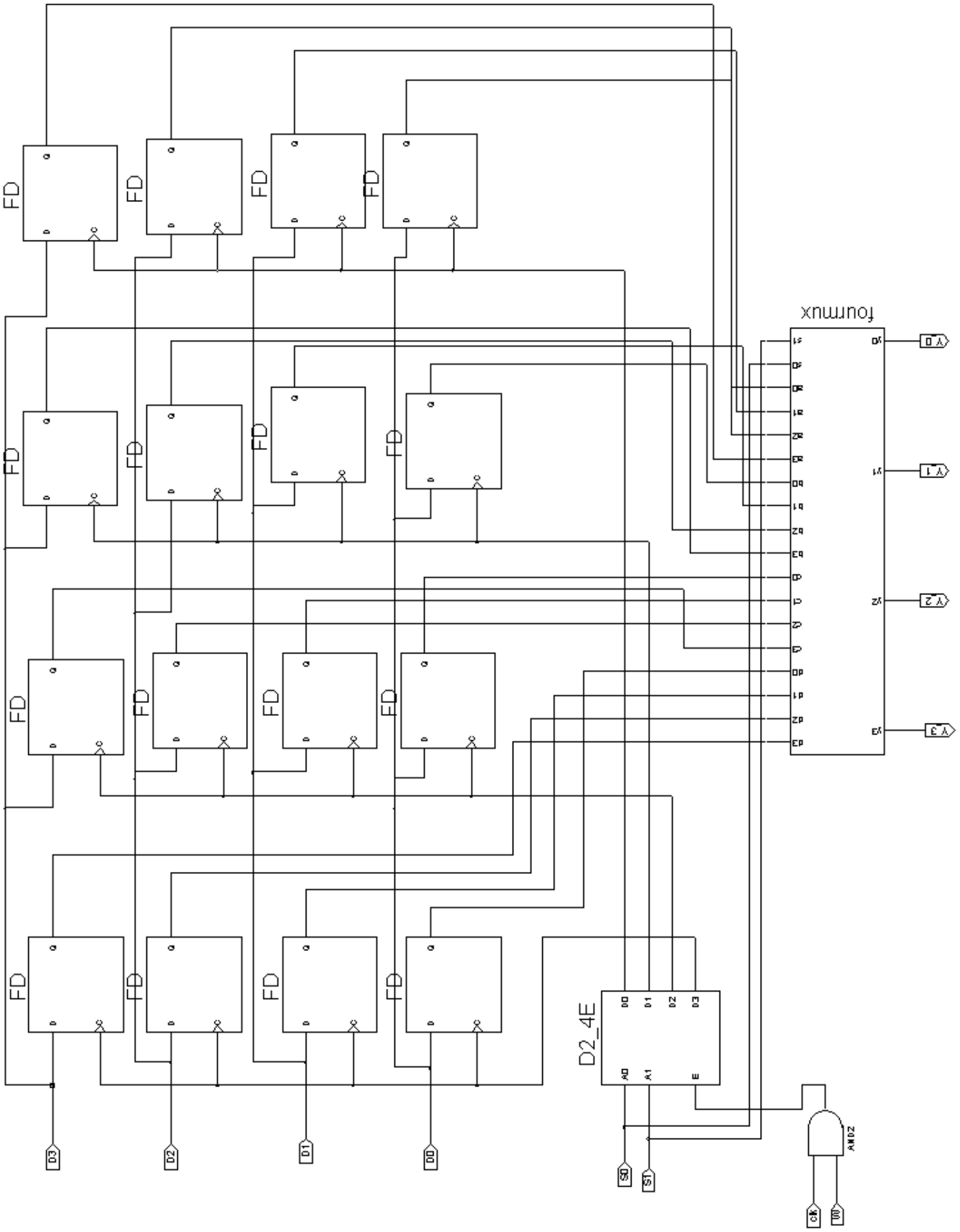

Figure 8-2: 4x4Bit Register Bank

A register bank is a set of address selectable registers.

Study of Figure 8-2 will show that when the input W =1, the address lines (S_1S_0) control which register gets updated on the low to high transition of the clock line. Study will also show the address lines (S_1S_0) are used to control which register's output is routed to the output lines.

Design:

1) A) Write a VHDL description to implement a 4-bit positive edge triggered register. **Turn in a hard copy as prelab.**

B) Compile and simulate the code for selected input combinations.
(For simulation : For clock input of your register, assign 4ns clock period. For the flip-flop inputs, force the following combinations and run 8ns for each combination.
0000, 0010 1010, 1100, 0011.

NOTE : Since the clock of the flip-flops will be driven ***directly*** by a regular I/O pin (not by GCK pins of the FPGA) , there would be a mapping error during implementing the design. The compiler adds an IBUFG buffer to the clock input, as a result the clock cannot be connected to a regular I/O pin. In order to change the error message to a warning, and to allow connection of the clock to an I/O pin, the following line should be added to the **.ucf** file. The following statement should be added after I/O planning step and all pin assignments. (Assign one of the switches to your clock signal.)

NET "XXXXX" CLOCK_DEDICATED_ROUTE = "FALSE";
XXXXX should be replaced by the clock assignment given your VHDL file.

C) Download and test it on the board.

2) A) Write a VHDL description to implement the 4x4Bit Register Bank of Figure 2**. Turn in a hard copy as prelab.**

a. Write a VHDL description for a 2 to 4 decoder with enable. (Use it as a component.) **Turn in a hard copy as prelab.**
Compile and simulate the code for all input combinations.

b. Use 4 copies of 4-bit register of part one. (Components)

c. Use a copy of multiplexer designed in Lab 7. (Component).

d. Add the necessary code to complete the source code.

B) Compile and simulate the code for the following input combinations.

(W and (S_1S_0) cannot change at the same time and W has to be equal to 0 when (S_1S_0) change.)

Assign 4ns period for clk with **FALLING** edge.

W = 0		run 8ns
(W = 0)	$S_1S_0 = 00$ D_3D_2 $D_1D_0 = 0011$	run 8ns
W = 1		run 8ns
W = 0		run 8ns

(W = 0) $S_1S_0 = 01$ $D_3D_2\ D_1D_0 = 1010$ run 8ns
W = 1 run 8ns
W = 0 run 8ns
(W = 0) $S_1S_0 = 10$ $D_3D_2\ D_1D_0 = 0101$ run 8ns
W = 1 run 8ns
W = 0 run 8ns
(W = 0) $S_1S_0 = 11$ $D_3D_2\ D_1D_0 = 1100$ run 8ns
W = 1 run 8ns
W = 0 run 8ns
(W = 0) $S_1S_0 = 00$ run 8ns Check the outputs Y_3 through Y_0
(W = 0) $S_1S_0 = 01$ run 8ns Check the outputs Y_3 through Y_0
(W = 0) $S_1S_0 = 10$ run 8ns Check the outputs Y_3 through Y_0
(W = 0) $S_1S_0 = 11$ run 8ns Check the outputs Y_3 through Y_0

C) Download and test it on the board.

All final VHDL files and simulation results of each part should be included in the report.