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1   ----------------------------------------------------------------------------------
2   -- Company:
3   -- Engineer:
4   --
5   -- Create Date:    14:11:32 10/25/2018
6   -- Design Name:
7   -- Module Name:    TestFuncfourtosixteen - Behavioral
8   -- Project Name:
9   -- Target Devices:
10  -- Tool versions:
11  -- Description:
12  --
13  -- Dependencies:
14  --
15  -- Revision:
16  -- Revision 0.01 - File Created
17  -- Additional Comments:
18  --
19  ----------------------------------------------------------------------------------
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22
23  -- Uncomment the following library declaration if using
24  -- arithmetic functions with Signed or Unsigned values
25  --use IEEE.NUMERIC_STD.ALL;
26
27  -- Uncomment the following library declaration if instantiating
28  -- any Xilinx primitives in this code.
29  --library UNISIM;
30  --use UNISIM.VComponents.all;
31
32  entity TestFuncfourtosixteen is
33      Port ( F0 : out  STD_LOGIC;
34             F1 : out  STD_LOGIC;
35             F2 : out  STD_LOGIC;
36             F3 : out  STD_LOGIC;
37             F4 : out  STD_LOGIC;
38             F5 : out  STD_LOGIC;
39             F6 : out  STD_LOGIC;
40             F7 : out  STD_LOGIC;
41             A : in  STD_LOGIC;
42             B : in  STD_LOGIC;
43             C : in  STD_LOGIC;
44             D,En : in  STD_LOGIC);
45  end TestFuncfourtosixteen;
46
47  architecture Behavioral of TestFuncfourtosixteen is
48  COMPONENT fourtosixteen
49     PORT(
50        A : IN std_logic;
51        B : IN std_logic;
52        C : IN std_logic;
53        D : IN std_logic;
54        En : IN std_logic;
55        Y0 : OUT std_logic;
56        Y1 : OUT std_logic;
57        Y2 : OUT std_logic;
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58          Y3 : OUT std_logic;
59          Y4 : OUT std_logic;
60          Y5 : OUT std_logic;
61          Y6 : OUT std_logic;
62          Y7 : OUT std_logic;
63          Y8 : OUT std_logic;
64          Y9 : OUT std_logic;
65          Y10 : OUT std_logic;
66          Y11 : OUT std_logic;
67          Y12 : OUT std_logic;
68          Y13 : OUT std_logic;
69          Y14 : OUT std_logic;
70          Y15 : OUT std_logic
71          );
72       END COMPONENT;
73       signal out0: std_logic_vector(15 downto 0);
74
75    begin
76    Inst_fourtosixteen: fourtosixteen PORT MAP(
77          Y0 => out0(0),
78          Y1 => out0(1),
79          Y2 => out0(2),
80          Y3 => out0(3),
81          Y4 => out0(4),
82          Y5 => out0(5),
83          Y6 => out0(6),
84          Y7 => out0(7),
85          Y8 => out0(8),
86          Y9 => out0(9),
87          Y10 => out0(10),
88          Y11 => out0(11),
89          Y12 => out0(12),
90          Y13 => out0(13),
91          Y14 => out0(14),
92          Y15 => out0(15),
93          A => A,
94          B => B,
95          C => C,
96          D => D,
97          En => En
98       );
99
100   F0 <= (out0(0) or out0(14) or out0(15));
101   F1 <= (out0(1) or out0(13) or out0(15));
102   F2 <= (out0(2) or out0(12) or out0(15));
103   F3 <= (out0(3) or out0(11) or out0(15));
104   F4 <= (out0(4) or out0(10) or out0(15));
105   F5 <= (out0(5) or out0(9) or out0(15));
106   F6 <= (out0(6) or out0(8) or out0(15));
107   F7 <= (out0(7) or out0(15));
108
109
110   end Behavioral;
111
112
```