```
1   ----------------------------------------------------------------------------------
2   -- Company:
3   -- Engineer:
4   --
5   -- Create Date:    14:02:43 11/08/2018
6   -- Design Name:
7   -- Module Name:    SegmentOddCounter - Behavioral
8   -- Project Name:
9   -- Target Devices:
10  -- Tool versions:
11  -- Description:
12  --
13  -- Dependencies:
14  --
15  -- Revision:
16  -- Revision 0.01 - File Created
17  -- Additional Comments:
18  --
19  ----------------------------------------------------------------------------------
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22
23  -- Uncomment the following library declaration if using
24  -- arithmetic functions with Signed or Unsigned values
25  --use IEEE.NUMERIC_STD.ALL;
26
27  -- Uncomment the following library declaration if instantiating
28  -- any Xilinx primitives in this code.
29  --library UNISIM;
30  --use UNISIM.VComponents.all;
31
32  entity SegmentOddCounter is
33     Port ( clk,UD,reset : in STD_LOGIC;
34            Y : out std_logic_vector (6 downto 0)
35
36     );
37  end SegmentOddCounter;
38
39  architecture Behavioral of SegmentOddCounter is
40  COMPONENT SelfStartSeq
41     PORT(
42        UD : IN std_logic;
43        clk : IN std_logic;
44        reset : IN std_logic;
45        Q : OUT std_logic_vector(3 downto 0)
46        );
47     END COMPONENT;
48
49  COMPONENT SevenSegmentA
50     PORT(
51        I0 : IN std_logic;
52        I1 : IN std_logic;
53        I2 : IN std_logic;
54        I3 : IN std_logic;
55        SegAout : OUT std_logic;
56        SegBout : OUT std_logic;
57        SegCout : OUT std_logic;
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58          SegDout : OUT std_logic;
59          SegEout : OUT std_logic;
60          SegFout : OUT std_logic;
61          SegGout : OUT std_logic
62          );
63       END COMPONENT;
64
65    signal clkSig,UDsig,resetSig :  STD_LOGIC;
66    signal Qsig : std_logic_vector (3 downto 0);
67    signal Ysig :  std_logic_vector (6 downto 0);
68
69    begin
70
71    Inst_SelfStartSeq: SelfStartSeq PORT MAP(
72          UD => UDsig,
73          clk => clkSig,
74          reset => resetSig,
75          Q => Qsig(3 downto 0)
76       );
77
78    Inst_SevenSegmentA: SevenSegmentA PORT MAP(
79          SegAout => Ysig(0),
80          SegBout => Ysig(1),
81          SegCout => Ysig(2),
82          SegDout => Ysig(3),
83          SegEout => Ysig(4),
84          SegFout => Ysig(5),
85          SegGout => Ysig(6),
86          I0 => Qsig(0),
87          I1 => Qsig(1),
88          I2 => Qsig(2),
89          I3 => Qsig(3)
90       );
91
92       clkSig <= clk;
93       resetSig <= reset;
94       UDsig <= UD;
95       Y <= Ysig;
96
97    end Behavioral;
98
99
```