```
1  ----------------------------------------------------------------------------------
2  -- Company:
3  -- Engineer:
4  --
5  -- Create Date:    11:09:44 11/01/2018
6  -- Design Name:
7  -- Module Name:    FourByFour - Behavioral
8  -- Project Name:
9  -- Target Devices:
10 -- Tool versions:
11 -- Description:
12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19 ----------------------------------------------------------------------------------
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22
23 -- Uncomment the following library declaration if using
24 -- arithmetic functions with Signed or Unsigned values
25 --use IEEE.NUMERIC_STD.ALL;
26
27 -- Uncomment the following library declaration if instantiating
28 -- any Xilinx primitives in this code.
29 --library UNISIM;
30 --use UNISIM.VComponents.all;
31
32 entity FourByFour is
33    Port ( X : in std_logic_vector(3 downto 0);
34           S : in std_logic_vector(1 downto 0);
35           Clock, W : in std_logic;
36           Z : out std_logic_vector(3 downto 0)
37    );
38 end FourByFour;
39
40 architecture Behavioral of FourByFour is
41
42
43 COMPONENT twotofour
44    PORT(
45       A : IN std_logic_vector(1 downto 0);
46       En : IN std_logic;
47       Y : OUT std_logic_vector(3 downto 0)
48       );
49    END COMPONENT;
50
51 COMPONENT FourRegister
52    PORT(
53       D : IN std_logic_vector(3 downto 0);
54       CLK : IN std_logic;
55       Q : OUT std_logic_vector(3 downto 0)
56       );
57    END COMPONENT;
```

```
58
59    COMPONENT MUXfourtoone
60       PORT(
61          S : IN std_logic_vector(1 downto 0);
62          A : IN std_logic_vector(3 downto 0);
63          B : IN std_logic_vector(3 downto 0);
64          C : IN std_logic_vector(3 downto 0);
65          D : IN std_logic_vector(3 downto 0);
66          Y : OUT std_logic_vector(3 downto 0)
67          );
68       END COMPONENT;
69
70    signal ClkEn : std_logic;
71    signal ClkSig: std_logic_vector(3 downto 0);
72    signal SwitchSig: std_logic_vector(1 downto 0);
73    signal Bank3,Bank2,Bank1,Bank0,Zsig,Xsig : std_logic_vector(3 downto 0);
74
75
76    begin
77    Inst_twotofour: twotofour PORT MAP(
78       A => SwitchSig(1 downto 0),
79       En => ClkEn ,
80       Y => ClkSig(3 downto 0)
81    );
82
83    Inst_FourRegister0: FourRegister PORT MAP(
84       D => Xsig(3 downto 0),
85       CLK => ClkSig(0),
86       Q => Bank0(3 downto 0)
87    );
88
89    Inst_FourRegister1: FourRegister PORT MAP(
90       D => Xsig(3 downto 0),
91       CLK => ClkSig(1),
92       Q => Bank1(3 downto 0)
93    );
94
95    Inst_FourRegister2: FourRegister PORT MAP(
96       D => Xsig(3 downto 0),
97       CLK => ClkSig(2),
98       Q => Bank2(3 downto 0)
99    );
100
101   Inst_FourRegister3: FourRegister PORT MAP(
102      D => Xsig(3 downto 0),
103      CLK => ClkSig(3),
104      Q => Bank3(3 downto 0)
105   );
106
107   Inst_MUXfourtoone: MUXfourtoone PORT MAP(
108      S => SwitchSig(1 downto 0),
109      A => Bank0(3 downto 0),
110      B => Bank1(3 downto 0),
111      C => Bank2(3 downto 0),
112      D => Bank3(3 downto 0),
113      Y => Zsig
114   );
```

```
115
116       ClkEn <= (Clock and W);
117       SwitchSig <= S(1 downto 0);
118       Xsig <= X(3 downto 0);
119       Z <= Zsig;
120
121    end Behavioral;
122
123
```