```
1   ----------------------------------------------------------------------------------
2   -- Company:
3   -- Engineer:
4   --
5   -- Create Date:    10:55:52 11/01/2018
6   -- Design Name:
7   -- Module Name:    twotofour - Behavioral
8   -- Project Name:
9   -- Target Devices:
10  -- Tool versions:
11  -- Description:
12  --
13  -- Dependencies:
14  --
15  -- Revision:
16  -- Revision 0.01 - File Created
17  -- Additional Comments:
18  --
19  ----------------------------------------------------------------------------------
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22
23  -- Uncomment the following library declaration if using
24  -- arithmetic functions with Signed or Unsigned values
25  --use IEEE.NUMERIC_STD.ALL;
26
27  -- Uncomment the following library declaration if instantiating
28  -- any Xilinx primitives in this code.
29  --library UNISIM;
30  --use UNISIM.VComponents.all;
31
32  entity twotofour is
33        Port ( A : in STD_LOGIC_VECTOR(1 DOWNTO 0);
34               En : in STD_LOGIC;
35               Y : out STD_LOGIC_VECTOR(3 DOWNTO 0));
36  end twotofour;
37
38  architecture Behavioral of twotofour is
39  begin
40  process (A,En)
41  begin
42     Y <= "0000";
43     if (En = '1') then
44        case A is
45           when "00" => Y <= "0001";
46           when "01" => Y <= "0010";
47           when "10" => Y <= "0100";
48           when "11" => Y <= "1000";
49           when others => Y <= "0000";
50        end case;
51     end if;
52  end process;
53  end Behavioral;
54
55
```