Digital Design and Logical Synthesis for Electrical Computer Engineering

Error Correction Encoder & Decoder

Digital High Level Synthesis

Version 0.1

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Revision Log

Rev	Change	Description	Reason for change	Done By	Date
0.1	Initial document			Shy Hamami	4,Jun,2007
0.2	Digital Changes			Amir Kolaman	14,Jul,2007
0.3					

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1. INTRODUCTION

In this third part of the project, we will perform synthesis flow for the hardware design we have created in previous labs. We will convert our design from Verilog code to Gate Level code using the synthesis tool "Design Compiler", and will analyze the results using the generated reports.

1.1 Design Constraints

We have chosen to use the suggested required constraints that were presented in the Lab PDF, and to not add any further constraints. The only variation that was made was to the clock period. The constraints used can be seen in the following table:

Constraint Type	Value
Clock period	50 MHz
Clock uncertainty	0.1 ns
Clock transition time	0.1 ns
Input delay	0.2 ns
Input transition	0.1 ns
Output delay	0.5 ns
Design area	50,000,000 um
Wire load model	Tsmc18_wl50

Table 1: Design Constraints

2. REPORTS & RESULTS

We have performed the requested synthesis, and included the reports in the admission files. We will elaborate on the here:

2.1 Area report

```
****************************************
Report : area
Design : ecc_enc_dec
Version: O-2018.06-SP4
Date   : Tue Dec 28 18:34:14 2021
****************************************

Library(s) Used:

    slow (File: /users/agnon/pp2022/aharonlu/Desktop/DC/LibraryFiles/db/slow.db)

Number of ports:                          716
Number of nets:                          1917
Number of cells:                         1391
Number of combinational cells:           1116
Number of sequential cells:               264
Number of macros/black boxes:               0
Number of buf/inv:                        366
Number of references:                       3

Combinational area:              17140.939373
Buf/Inv area:                     2661.120046
Noncombinational area:           18880.646469
Macro/Black Box area:                0.000000
Net Interconnect area:          818070.888824

Total cell area:                 36021.585843
Total area:                     854092.474667
1
```

Fig 1: Area report

As can be seen, the Total area we have received is 854,092 um, which is far below than the 50 million um that we have set for our constraint. How could we have reduced even further the design size?

In this project, we have used a multi-cycle approach. We have the encoder and decoder act combinational, but everything else is synced to a clock, and working by a controller that is activating the encoder and decoder using an FSM machine. This approach allows us to use a relatively high clock frequency, but is also forcing us to use more flip-flops, thus increasing the overall size. We believe that if we used an approach more like a single cycle, we would have received a smaller design size.

2.2 Timing Report

```
Point                                                   Incr       Path
-----------------------------------------------------------------------------
clock clk (rise edge)                                   0.00       0.00
clock network delay (ideal)                             0.60       0.60
Register_Bank/CTRL_reg[0]/CK (DFFRHQX1)                 0.00       0.60 r
Register_Bank/CTRL_reg[0]/Q (DFFRHQX1)                  2.54       3.14 r
Register_Bank/CTRL[0] (Register_Bank_AMBA_WORD32_AMBA_ADDR_WIDTH20)
                                                        0.00       3.14 r
controller/CTRL[0] (controller_AMBA_WORD32_DATA_WIDTH32)
                                                        0.00       3.14 r
controller/U84/Y (INVX1)                                1.11       4.25 f
controller/U83/Y (NOR2X1)                               1.49       5.74 r
controller/U63/Y (INVX1)                                1.53       7.27 f
controller/U80/Y (OAI222XL)                             1.54       8.81 r
controller/U5/Y (NAND2X4)                               0.17       8.98 f
controller/U82/Y (NAND2BX1)                             1.65      10.63 r
controller/U62/Y (NAND2X1)                              1.07      11.70 f
controller/U59/Y (OAI21XL)                              1.91      13.61 r
controller/U53/Y (INVX1)                                1.05      14.66 f
controller/U52/Y (CLKINVX3)                             2.30      16.96 r
controller/U94/Y (OAI2BB2X2)                            1.38      18.33 f
controller/Decoder/data_in[6] (Decoder_AMBA_WORD32_DATA_WIDTH32)
                                                        0.00      18.33 f
controller/Decoder/U85/Y (INVX1)                        1.61      19.94 r
controller/Decoder/U188/Y (XNOR2X1)                     1.75      21.69 r
controller/Decoder/U191/Y (XNOR2X1)                     1.61      23.30 r
controller/Decoder/U50/Y (XOR2X1)                       0.97      24.27 r
controller/Decoder/U49/Y (XOR2X1)                       1.12      25.39 r
controller/Decoder/U197/Y (XNOR2X1)                     1.25      26.64 r
controller/Decoder/U196/Y (NAND3BX1)                    0.80      27.44 f
controller/Decoder/U42/Y (NOR2X1)                       1.99      29.43 r
controller/Decoder/U20/Y (INVX1)                        1.30      30.73 f
controller/Decoder/U44/Y (NOR2X1)                       2.06      32.78 r
controller/Decoder/U22/Y (INVX1)                        1.01      33.79 f
controller/Decoder/U195/Y (NOR4BX1)                     1.22      35.01 r
controller/Decoder/U176/Y (AOI221X1)                    0.56      35.58 f
controller/Decoder/U175/Y (NAND2X1)                     0.64      36.22 r
controller/Decoder/data_out_reg[3]/D (DFFRHQX1)         0.00      36.22 r
data arrival time                                                 36.22

clock clk (rise edge)                                  50.00      50.00
clock network delay (ideal)                             0.60      50.60
clock uncertainty                                      -0.10      50.50
controller/Decoder/data_out_reg[3]/CK (DFFRHQX1)        0.00      50.50 r
library setup time                                     -0.25      50.25
data required time                                                50.25
-----------------------------------------------------------------------------
data required time                                                50.25
data arrival time                                                -36.22
-----------------------------------------------------------------------------
slack (MET)                                                       14.03
```

Fig 2: Timing Report

Here is some of the Timing Report for our synthesis. As you can see, our total slack we received is 14.03 ns, which is fairly good, meaning we could have used a faster clock frequency than we had used. Also, the critical path is depicted in the report, going from the Register_Bank Ctrl_reg[0], which activates the controller, which in itself is activating the Decoder, which is his sub-module. This makes sense, as the Decoder is doing more calculations than the Encoder, making it reasonable that this would be the critical path.

2.3 Constraints Violations

```
****************************************
Report : constraint
         -all_violators
Design : ecc_enc_dec
Version: O-2018.06-SP4
Date   : Tue Dec 28 18:34:23 2021
****************************************

This design has no violated constraints.

1
```

Fig 3: Constraints Violations

Here is the constraints report. As you can see, our design have not violated any constraints.

3. APPENDIX

3.1 Terminology

LSB - Least Significant Bit

TBR - To Be Reviewed

TBD - To Be Defined

3.2 References