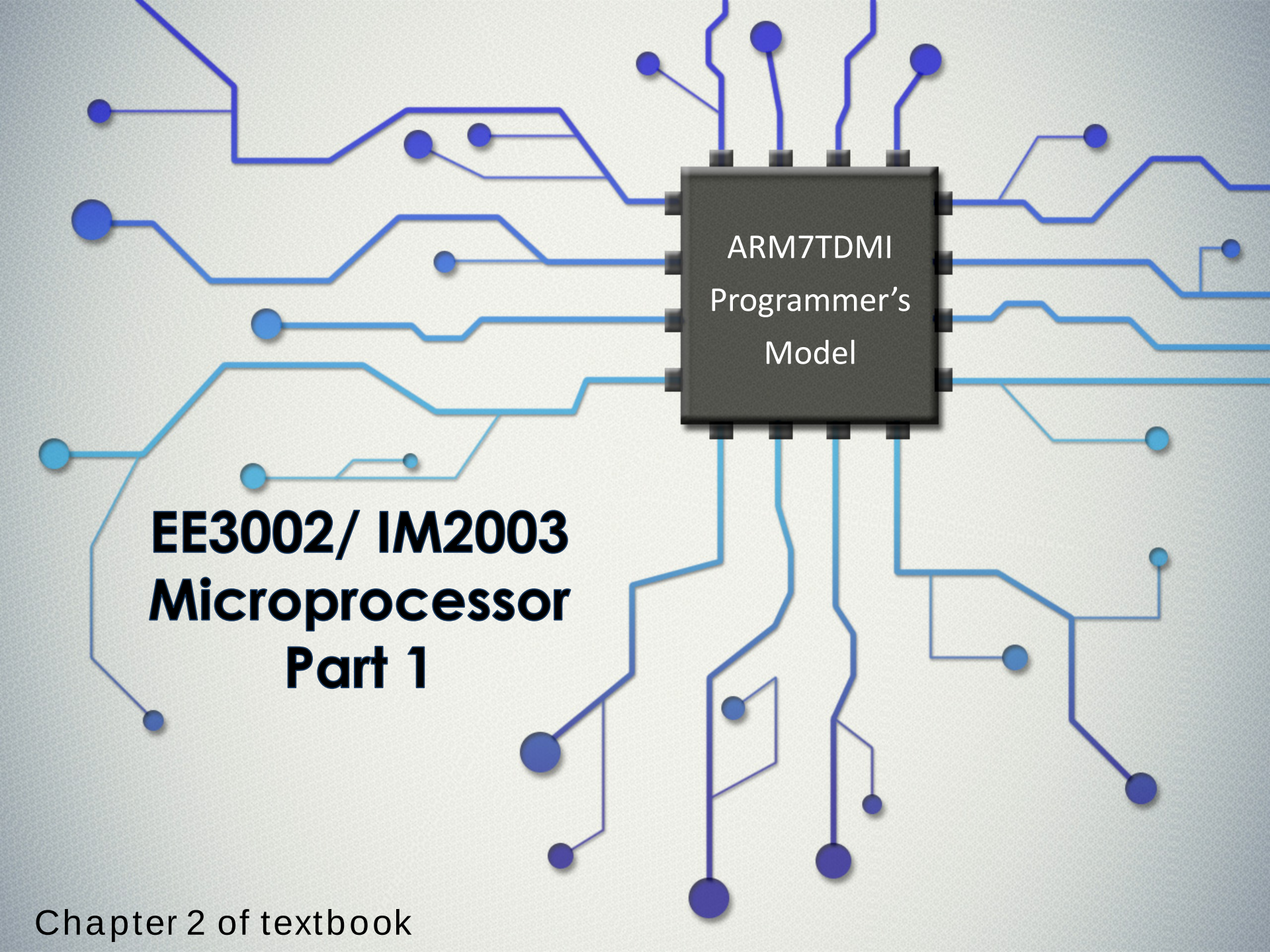


EE3002/ IM2003 Microprocessor Part 1

Chapter 2 of textbook

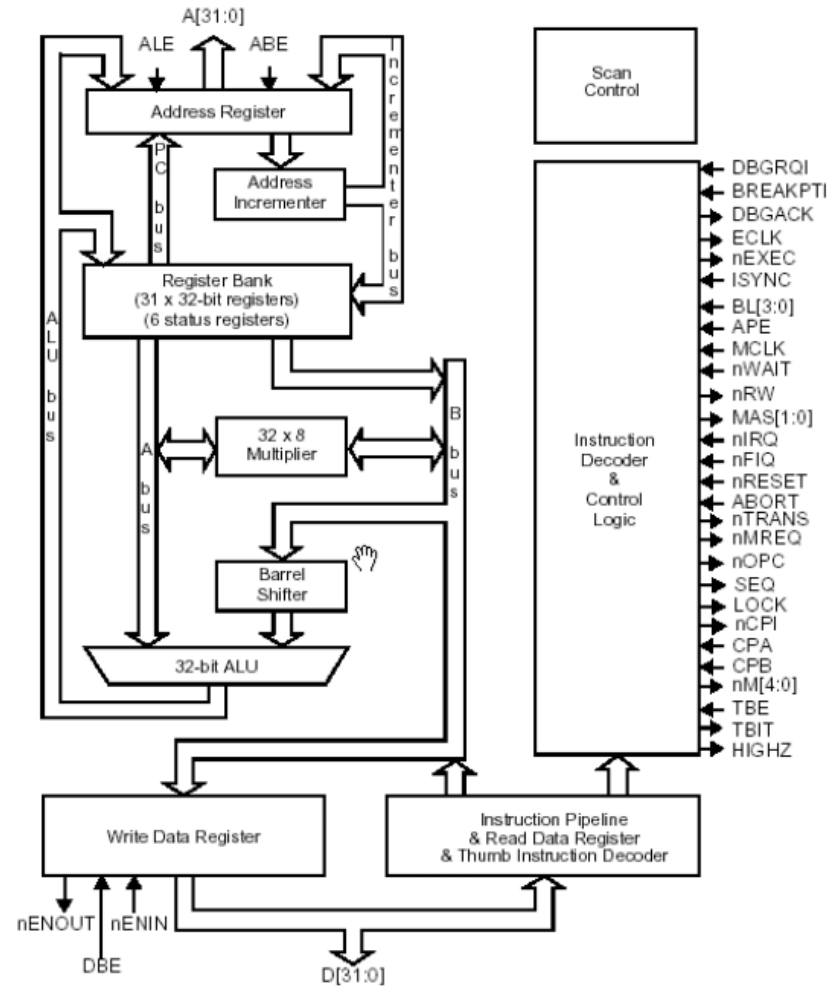
ARM7TDMI

- ARM7 was introduced in 1993.
- The updated version ARM7TDMI became hugely popular.
- T for THUMB: a 16 bit instruction set, which is more compact than the standard 32 bit instruction set (We will focus on the standard instructions for now).
- D for Debug: new debugging hardware is added into the processor.
- M for Multiplier: a larger hardware multiplier is included.
- I for In-Circuit-Emulation: allows hardware emulation of the actual processor.

2 ARM States

- ARM State : Standard 32-bit length instructions are used.
- THUMB State : Compressed 16-bit length instructions are used. Provides flexibility of putting more instructions into the same amount of memory or reduce the amount of memory needed for a given design.

ARM7TDMI Architecture



7 ARM Processor Modes

Mode	Description	
Supervisor (SVC)	Entered on reset and when a Software Interrupt (SWI) Instruction is executed.	Privileged modes
FIQ	Entered when a high priority (fast) interrupt is raised	
IRQ	Entered when a low priority (normal) interrupt is raised.	
Abort	Used to handle memory access violations	
Undef	Used to handle undefined instructions	
System	Privileged mode using the same registers as User mode	
User	Mode under which most applications/OS tasks run	Unprivileged mode

Registers

- A Register is the most fundamental storage area on the chip, can be used to stored any data you wish.
- ARM7TDMI has 37 32-bit registers
  - 30 general-purpose registers
  - 6 status registers
  - A program counter (PC)
- Not all registers are visible at any one time.

ARM State General Registers and Program Counter

System & User	FIQ	Supervisor	Abort	IRQ	Undefined
R0	R0	R0	R0	R0	R0
R1	R1	R1	R1	R1	R1
R2	R2	R2	R2	R2	R2
R3	R3	R3	R3	R3	R3
R4	R4	R4	R4	R4	R4
R5	R5	R5	R5	R5	R5
R6	R6	R6	R6	R6	R6
R7	R7	R7	R7	R7	R7
R8	R8_fiq	R8	R8	R8	R8
R9	R9_fiq	R9	R9	R9	R9
R10	R10_fiq	R10	R10	R10	R10
R11	R11_fiq	R11	R11	R11	R11
R12	R12_fiq	R12	R12	R12	R12
R13	R13_fiq	R13_svc	R13_abt	R13_irq	R13_und
R14	R14_fiq	R14_svc	R14_abt	R14_irq	R14_und
R15 (PC)	R15 (PC)	R15 (PC)	R15 (PC)	R15 (PC)	R15 (PC)

ARM State Program Status Registers

CPSR	CPSR	CPSR	CPSR	CPSR	CPSR
	SPSR_fiq	SPSR_svc	SPSR_abt	SPSR_irq	SPSR_und

= banked register

Banking of registers

- For example, when the processor changes to FIQ mode, a large number of registers (r8-r14) are banked, or swap out.
- Done to save the current state of the machine. During an interrupt, it is necessary to stop what you are doing and begin work on a task.
- Rather than backing the original content of the registers into the external memory which takes time, the machine simply used a new set of registers instead. Hence execution speed improves!!!

Reserved Registers

- R13 is also known as Stack Pointer (SP). It holds the address of the stack in memory and a unique stack pointer exists in each mode (except System mode which shares the User mode stack pointer).
- R14 is also known as Link Register (LR). It is used as subroutine return address link register. It is unique except for system mode which shares the same register as User mode.
- R15 is the Program Counter (PC). It holds the address of the instruction being FETCHED (not the one being executed).

Instruction Execution

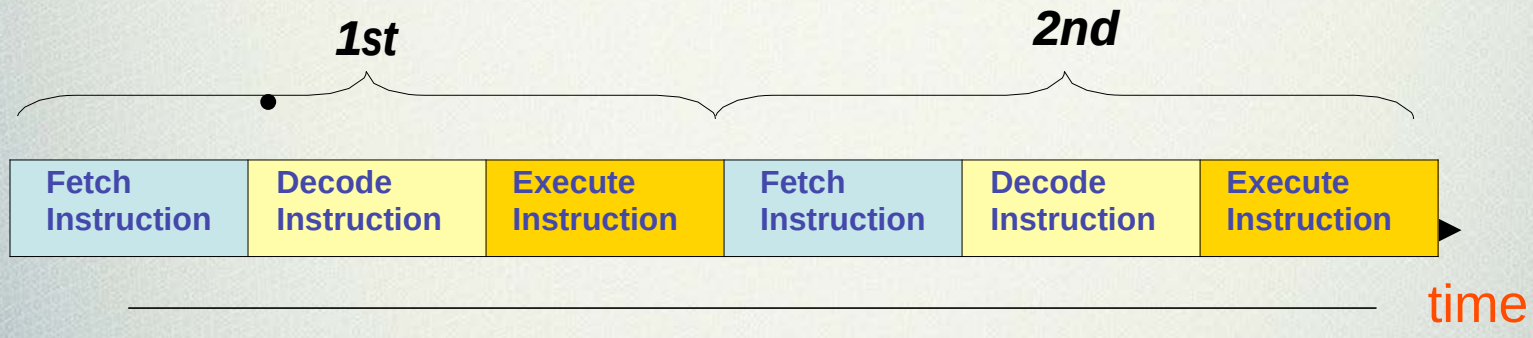
Multiple stages are involved in executing an instruction. Example:

1)Fetching the instruction code

2)Decoding the instruction code

3)Executing the instruction code

Hence multiple processor clock cycles are needed to execute one single instruction.

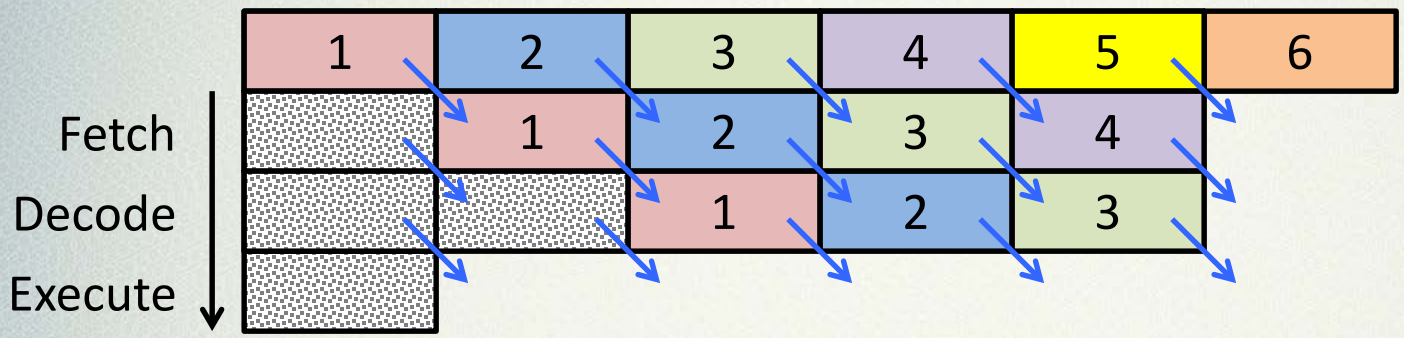


Instruction Pipeline

- Pipeline allows concurrent execution of multiple different instructions
- execution of different stages of multiple instructions at the same time

- During a normal operation
- while one instruction is being executed
- the next instruction is being decoded
- and a third instruction is being fetched from memory
- allows effective throughput to increase to one instruction per clock cycle

Pipelined Architecture



The ARM7 three-stage pipeline as independent fetch, decode and execute stages.

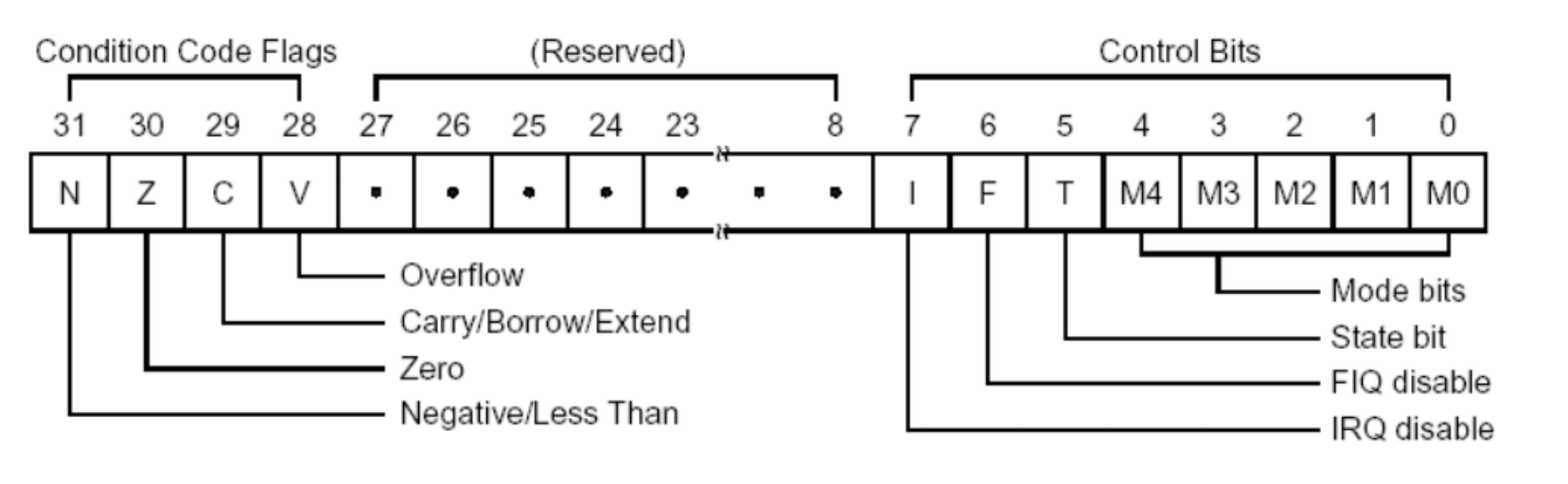
- FETCH: Instruction fetched from memory
- DECODE : Decoding of registers used in instruction
- EXECUTE :
  - Register(s) read from Register Bank,
  - Shift and ALU operation
  - Write register(s) back to Register Bank

Current Program Status Register(CPSR)

- CPSR shows the state of the machine.
- It contains condition code flags, interrupt enable flags, the current mode and the current state.
- Each privileged mode (except System mode) has Saved Program Status Register (SPSR) that is used to preserve the value of CPSR when an exception occurs.

Program Status Register

- Most significant 4 bits are condition code flags
- Least significant 8 bits are control bits



Control Bits

- I and F bits are interrupt disable bits which disable IRQ interrupts and FIQ interrupts respectively. For example, when I = 1, no IRQ interrupts are entertained.
- T is the status bits to indicate the state of the machine (ARM or THUMB). T =1 implies the machine is currently executing THUMB code. This bit is read only (not writable), you can only change between ARM and THUMB state via a special instruction.

Mode Bits

- Least significant 5 bits, M[4:0] are the mode bits.

xPSR[4:0]	Mode
10000	User
10001	FIQ
10010	IRQ
10011	Supervisor
10111	Abort
11011	Undefined
11111	System

The Vector Table

- The exception vector table consists of designated addresses in external memory that hold information necessary to handle an exception, an interrupt, or other atypical event such as a reset.
- For example, when an interrupt (IRQ) comes along, the processor will change the PC to 0x18 and fetch the actual ARM Instruction, which is most likely a Branch (B) instruction.

Exception Vector Table

Exception Type	Mode	Vector Address
Reset	Supervisor (SVC)	0x00000000
Undefined Instructions	Undefined (UNDEF)	0x00000004
Software Interrupt (SWI)	SVC	0x00000008
Prefetch abort	ABORT	0x0000000C
Data abort	ABORT	0x00000010
IRQ	IRQ	0x00000018
FIQ	FIQ	0x0000001C

Summary

- ARM7TDMI has two states : ARM and THUMB
- 7 modes of operation : User, Supervisor, FIQ, IRQ, Undefined, System and Abort.
- 37 Registers.
- 3-state Pipelined Architecture.
- Program status register (control bits and condition code flags)
- Vector Table