

**Table 2.** Threshold voltage assignment of the three proposed registers.

	<i>Register 1</i>	<i>Register 2</i>	<i>Register 3</i>
M1	low- $V_{th}$	low- $V_{th}$	low- $V_{th}$
M2	low- $V_{th}$	high- $V_{th}$	low- $V_{th}$
M3	low- $V_{th}$	high- $V_{th}$	low- $V_{th}$
M4	low- $V_{th}$	low- $V_{th}$	low- $V_{th}$
M7	low- $V_{th}$	low- $V_{th}$	high- $V_{th}$
M8	low- $V_{th}$	low- $V_{th}$	high- $V_{th}$
M9	low- $V_{th}$	low- $V_{th}$	high- $V_{th}$
M10	low- $V_{th}$	low- $V_{th}$	high- $V_{th}$
M13	high- $V_{th}$	low- $V_{th}$	low- $V_{th}$
M14	high- $V_{th}$	low- $V_{th}$	low- $V_{th}$
M17	high- $V_{th}$	low- $V_{th}$	low- $V_{th}$
M18	high- $V_{th}$	low- $V_{th}$	low- $V_{th}$
M19	high- $V_{th}$	low- $V_{th}$	low- $V_{th}$
M20	high- $V_{th}$	low- $V_{th}$	low- $V_{th}$
M21	high- $V_{th}$	low- $V_{th}$	low- $V_{th}$
M22	high- $V_{th}$	low- $V_{th}$	low- $V_{th}$

#### 4.3. Reduction in the Leakage Current

The amount of reduction in the leakage current achieved by utilizing the proposed three registers is evaluated in this section. Four CMOS technology generations, 45 nm, 32 nm, 22 nm, and 16 nm, are considered using a predictive technology model [28,29].

The register illustrated in Figure 8 is simulated for each technology node where the  $W/L$  ratios of the transistors are maintained constant. The leakage current drawn from the power supply is evaluated for the three registers and the results are compared with the leakage current of the original register where only low- $V_{th}$  transistors are used.

The results are illustrated in Figure 9. Note that for the first register, the state of the clock signal does not change the results since all of the high- $V_{th}$  transistors are within the slave latch. For the second and third registers, however, high- $V_{th}$  transistors exist within the tristate inverters. The state of the clock signal is therefore important in evaluating the results. For example, for the second register, clock signal should be at  $V_{SS}$  to guarantee that the initial tristate inverter is not in the high impedance state. Similarly, for the third register, clock signal should be at  $V_{DD}$  so that the second tristate inverter located along the feedback path is not in the high impedance state. The leakage current of the original register is therefore compared with the first two registers and third register when the clock signal is, respectively, at  $V_{SS}$  and  $V_{DD}$ .

The leakage current increases with technology, exhibiting a large jump in the 16 nm node. A significant amount of reduction in the leakage current, 79% on average, is achieved by the first register since the number of high- $V_{th}$  transistors is higher, as listed in Table 2. The second register also achieves a considerable amount of reduction in the leakage current, 13% on average and higher below 32 nm