SPI

SERIAL PERIPHERAL INTERFACE

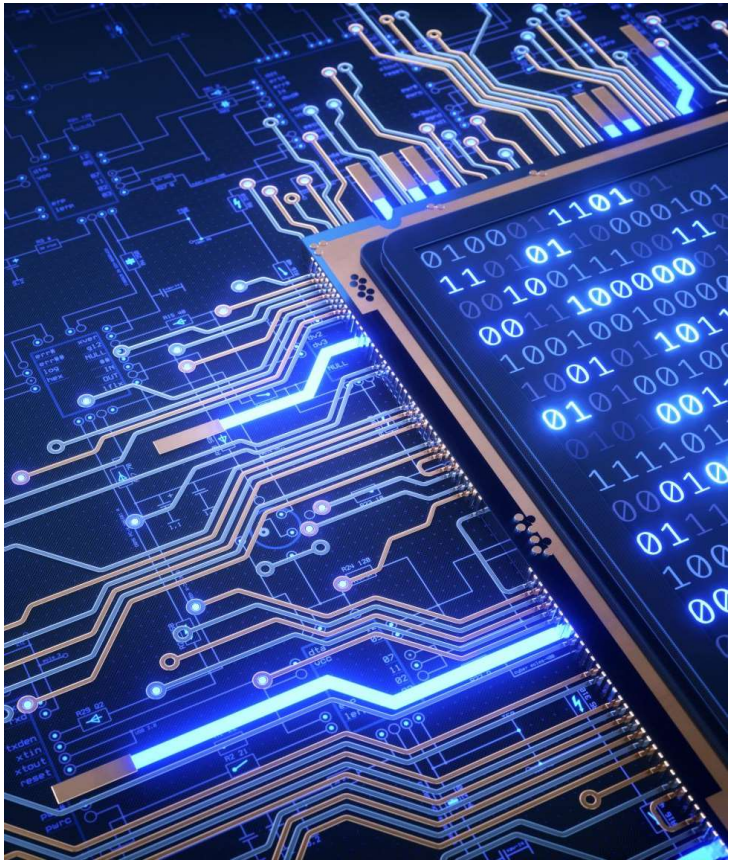
Developed by Motorola in mid-1980's.

Serial Communication

Full duplex Communication.

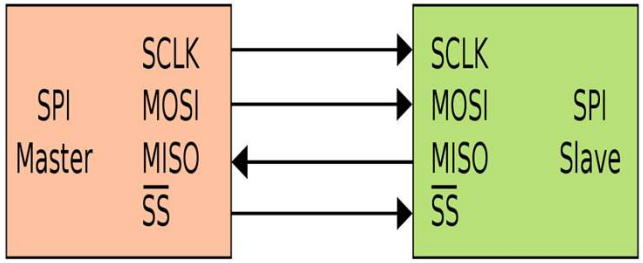
Master – Slave Configuration.

4-wire protocol.



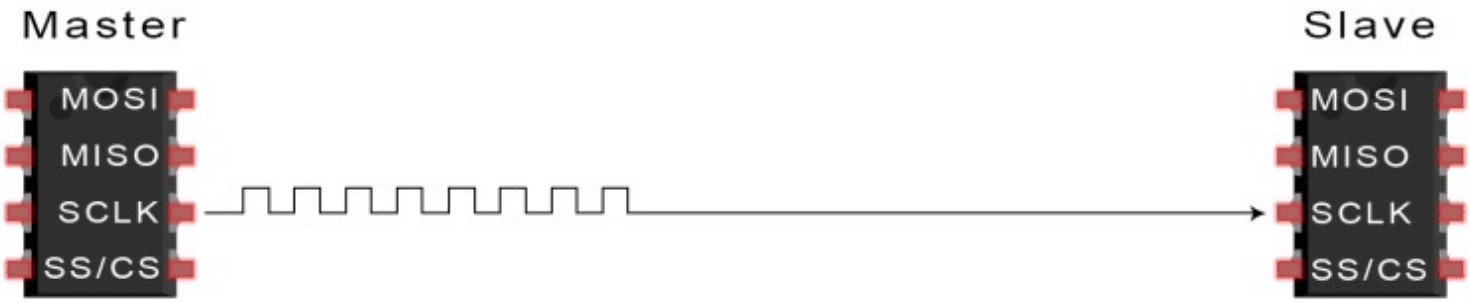
CONNECTION

- MOSI – Master Out Slave In (Data Out)
- MISO – Master In Slave Out (Data In)
- SS (CS) – Slave Select (Chip Select)
- SCLK – Serial Clock

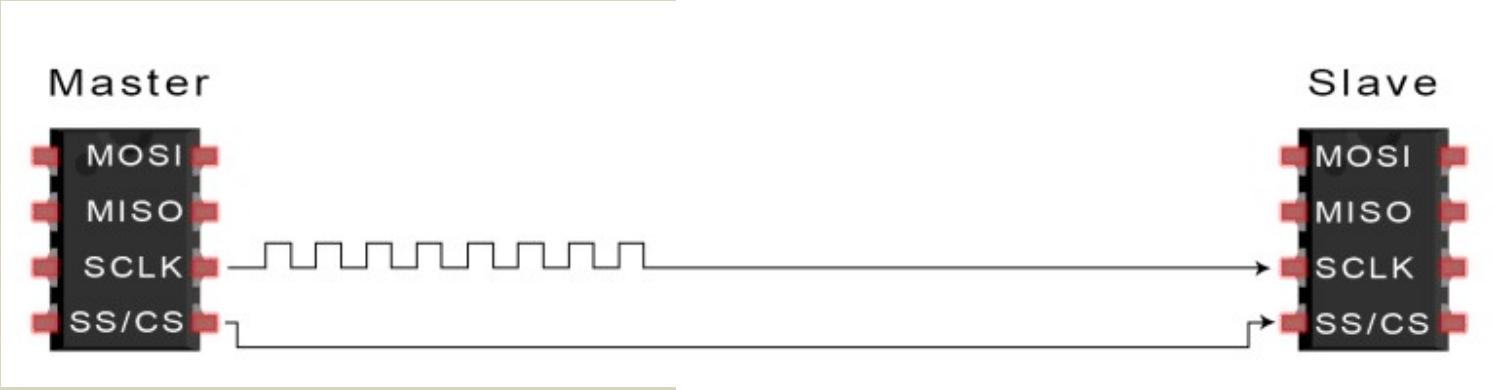


SPI DATA TRANSMISSION

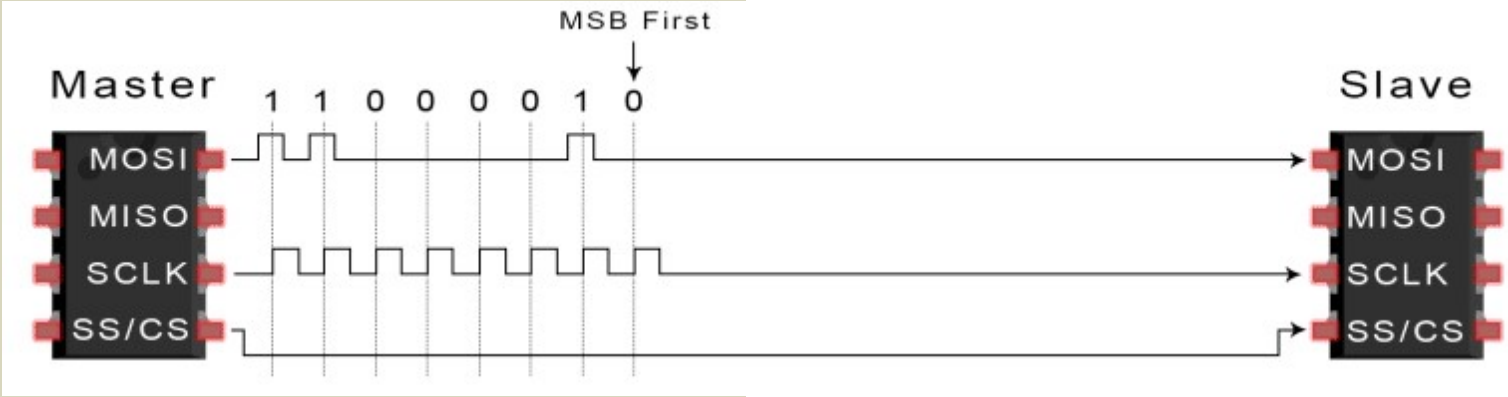
1. The master outputs the clock signal:



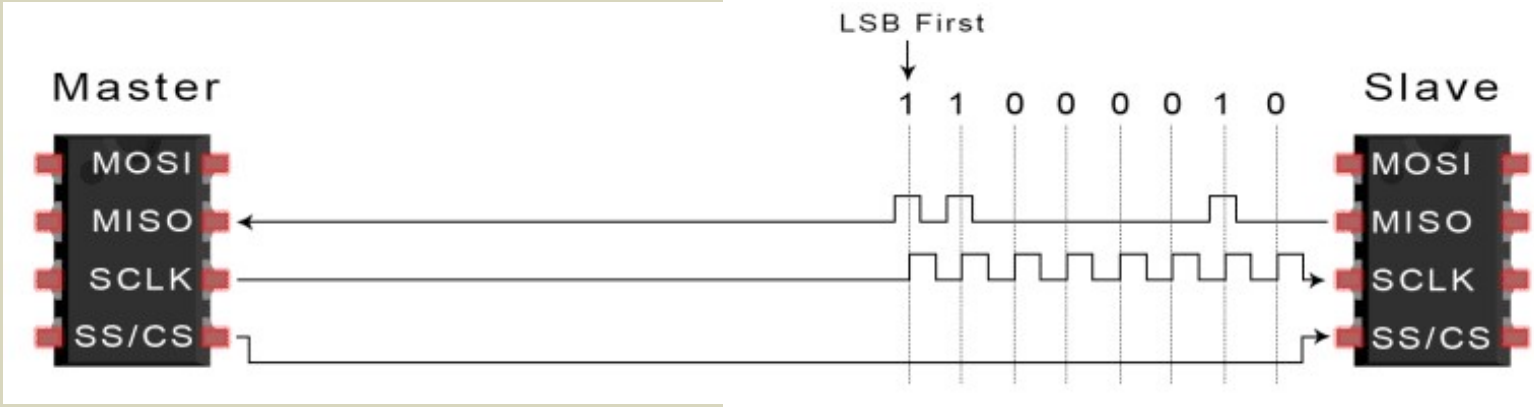
2. The master switches the SS/CS pin to a low voltage state, which activates the slave:



3. The master sends the data one bit at a time to the slave along the MOSI line. The slave reads the bits as they are received:



4. If a response is needed, the slave returns data one bit at a time to the master along the MISO line. The master reads the bits as they are received:



CLOCK POLARITY (CPOL)

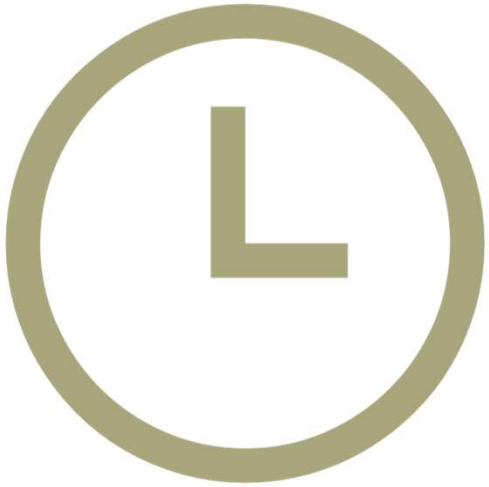
Clock Polarity determines the state of the clock.

CPOL is LOW:

- SCK is LOW when idle and toggles to HIGH during active state.

CPOL is HIGH:

- SCK is HIGH during idle and LOW during active state.



CLOCK PHASE (CPHA)

Clock Phase determines the clock transition i.e., rising (LOW to HIGH) or falling (HIGH to LOW).

CPHA is 0, the data is transmitted on the rising edge of the clock.

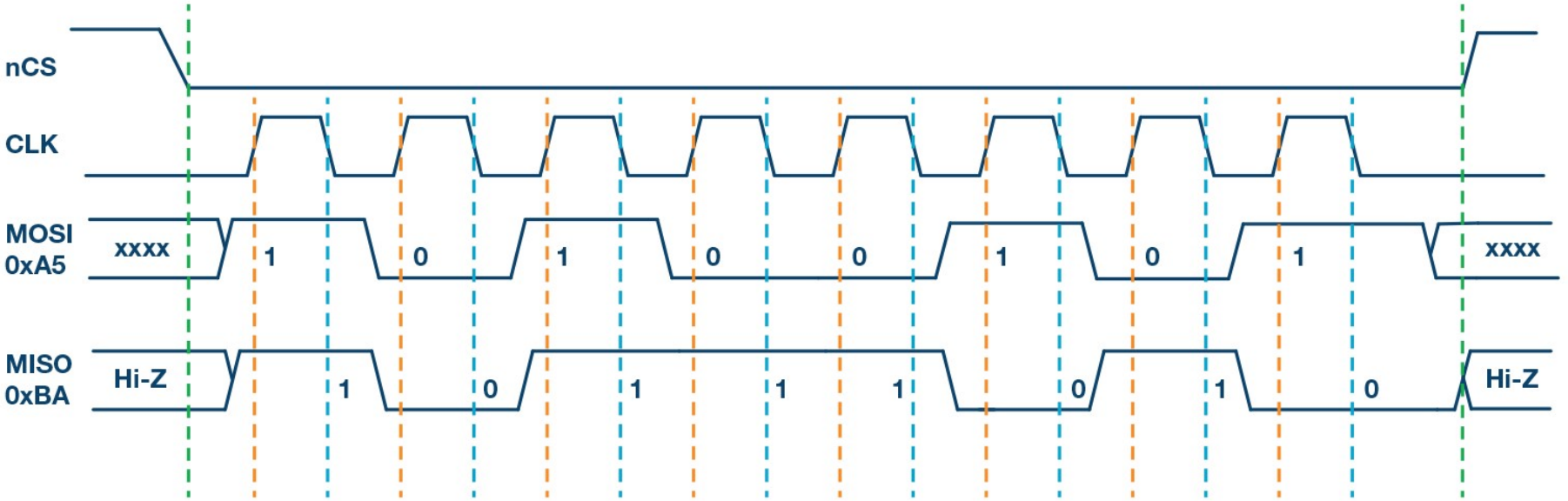
CPHA is 1, the data is transmitted on the falling edge of the clock.

SPI MODES

SPI Mode	CPOL	CPHA	Clock Polarity in Idle State	Clock Phase Used to Sample and/or Shift the Data
0	0	0	Logic low	Data sampled on rising edge and shifted out on the falling edge
1	0	1	Logic low	Data sampled on the falling edge and shifted out on the rising edge
2	1	0	Logic high	Data sampled on the rising edge and shifted out on the falling edge
3	1	1	Logic high	Data sampled on the falling edge and shifted out on the rising edge

MODE 0

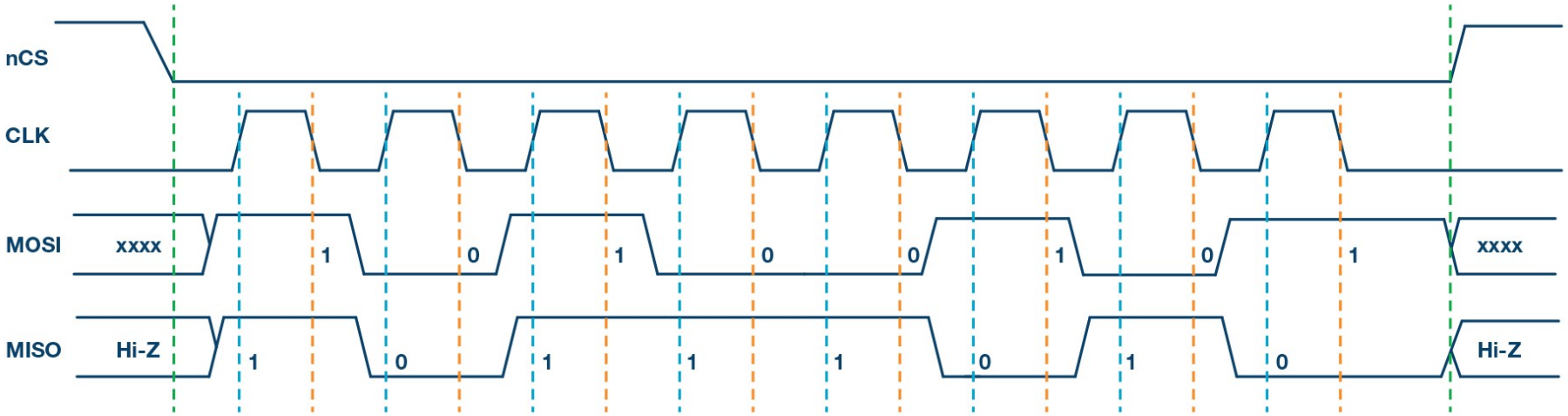
CPOL=0, CPHA=0



Data sampled on rising edge and shifted on falling edge.

MODE 1

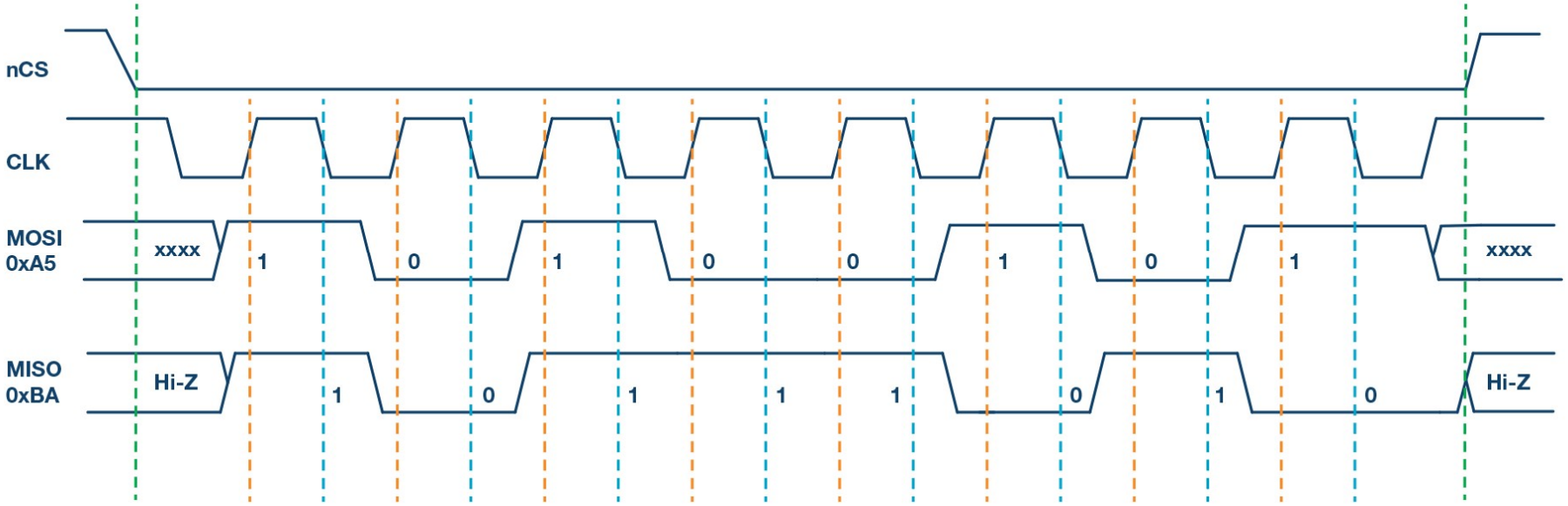
CPOL=0, CPHA=1



Data sampled on the falling edge and shifted on the rising edge.

MODE 2

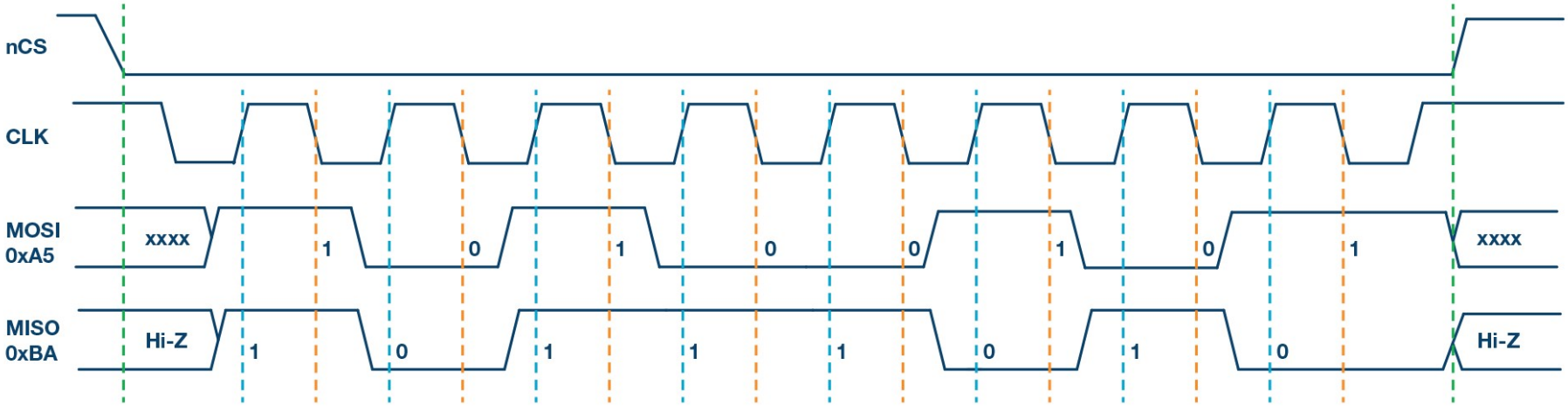
CPOL=1, CPHA=0



Data sampled on the rising edge and shifted on the falling edge.

MODE 3

CPOL=1, CPHA=1



Data sampled on the falling edge and shifted on the rising edge.

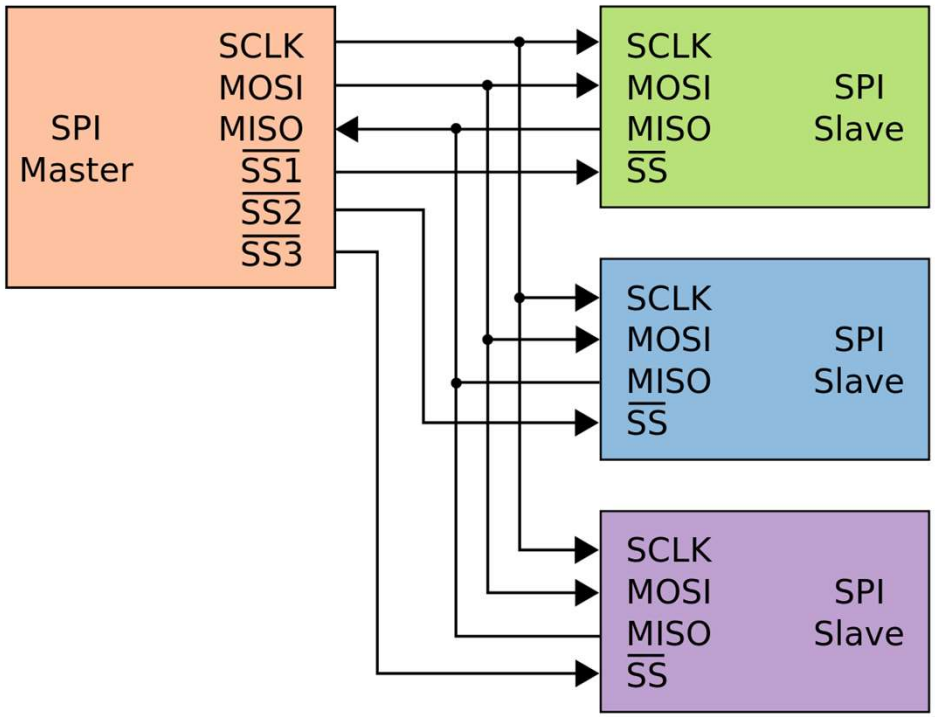
MULTI SLAVE CONFIGURATION:

SPI can be set up to operate with a single master and Multiples slaves.

Two Types

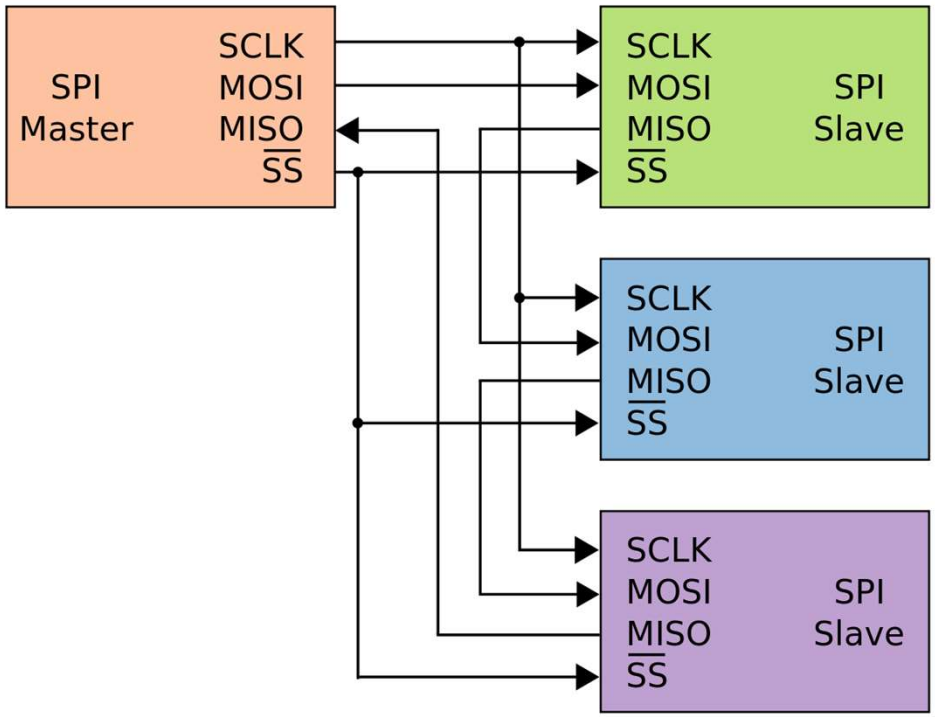
1. Independent slave configuration
2. Daisy chain configuration

INDEPENDENT SLAVE CONFIGURATION



Independent chip select line for each slave.

DAISY CHAIN CONFIGURATION



Requires a single SS line from the master.

PROS

Full duplex communication.

High Speed.

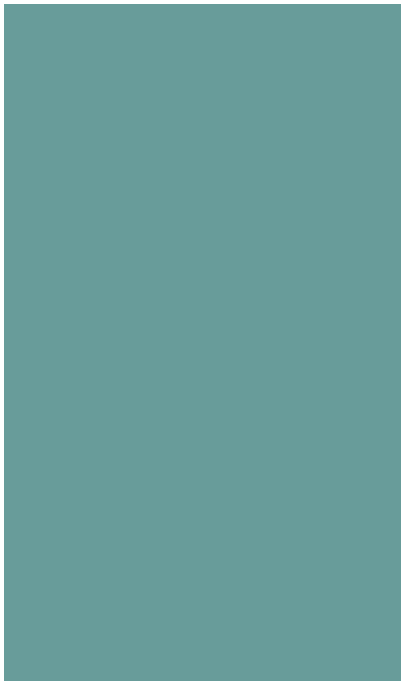
One Unique Signal (SS/CS).

CONS

Requires more pins than I2C.

Supports only one master device.

No error-checking.



USE CASES

Sensors:

- Temperature, Pressure, ADC, touchscreens, etc.,

Memory: Flash and EEPROM

Real-time clocks

Any MMC or SD card (including SDIO variant)

SUMMARY

Wires Used	4
Maximum Speed	Up to 10 Mbps
Synchronous or Asynchronous?	Synchronous
Serial or Parallel?	Serial
Max # of Masters	1
Max # of Slaves	Theoretically unlimited*