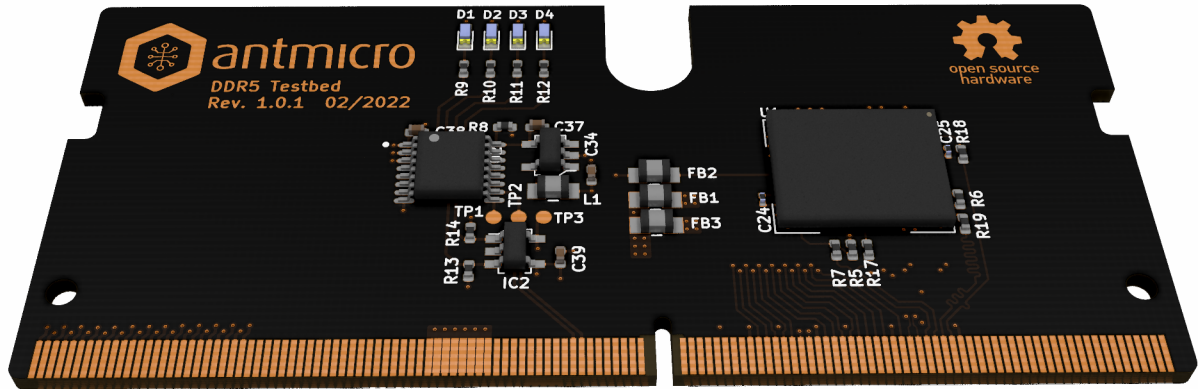


DDR5 testbed

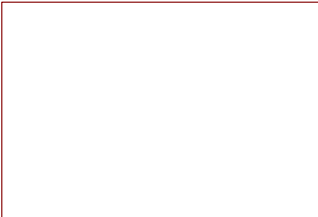


EEPROM



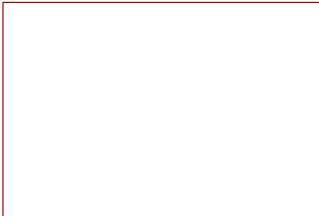
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SODIMM



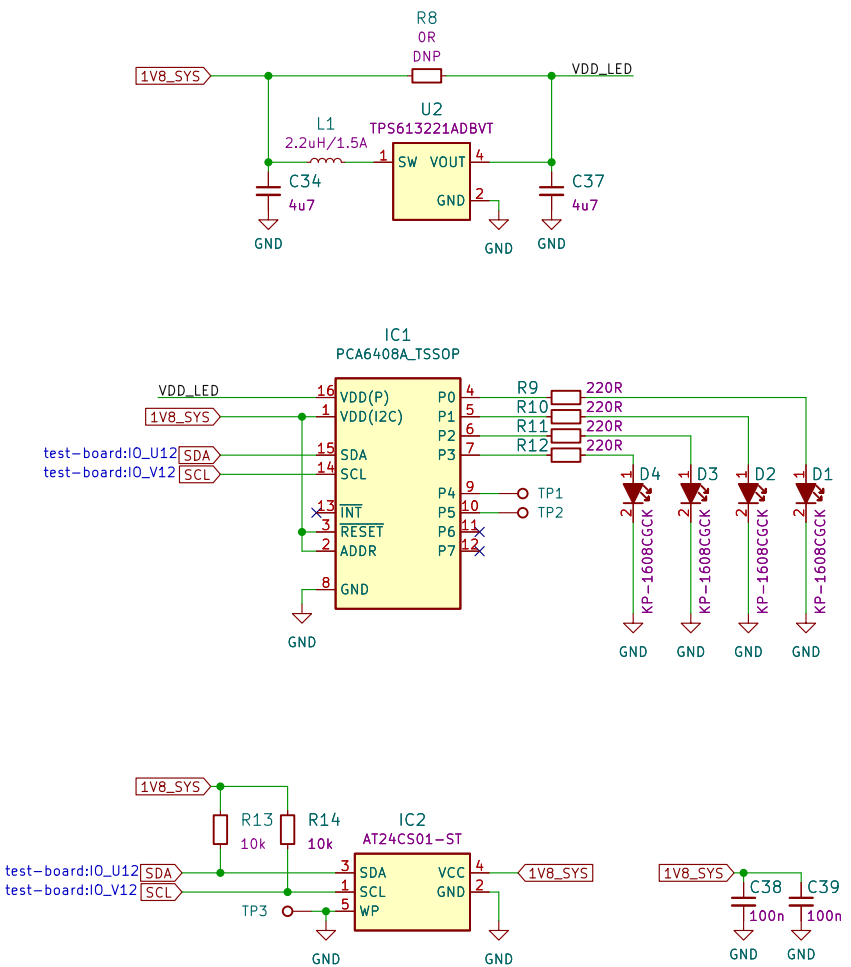
File: sodim.kicad_sch

DDR5



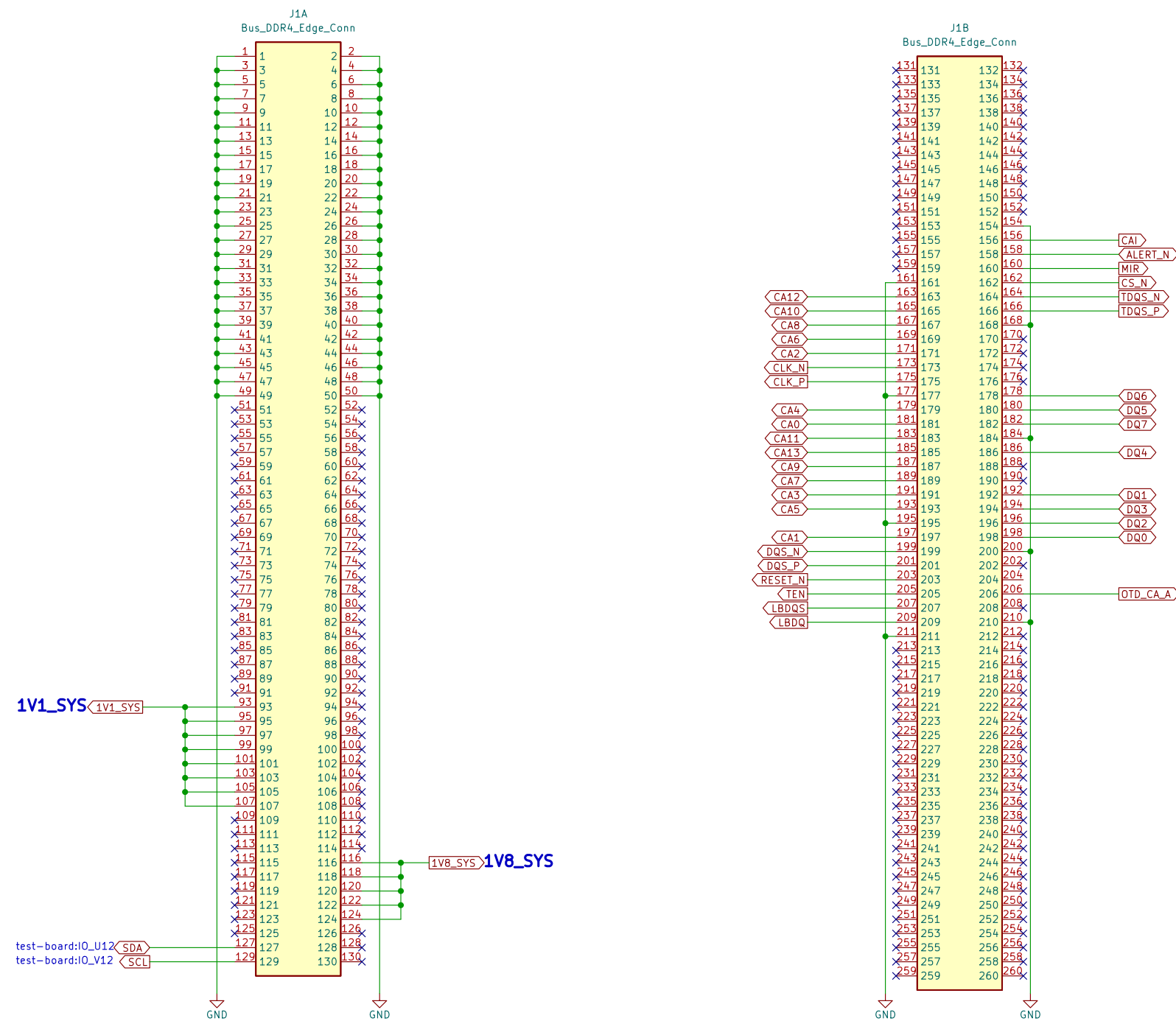
File: ddr5.kicad_sch

I2C peripherals



SODIMM Connector

Note:
The pin assignment for that connector matches
an experimental research platform available at
<https://github.com/antmicro/lpddr4-test-board>



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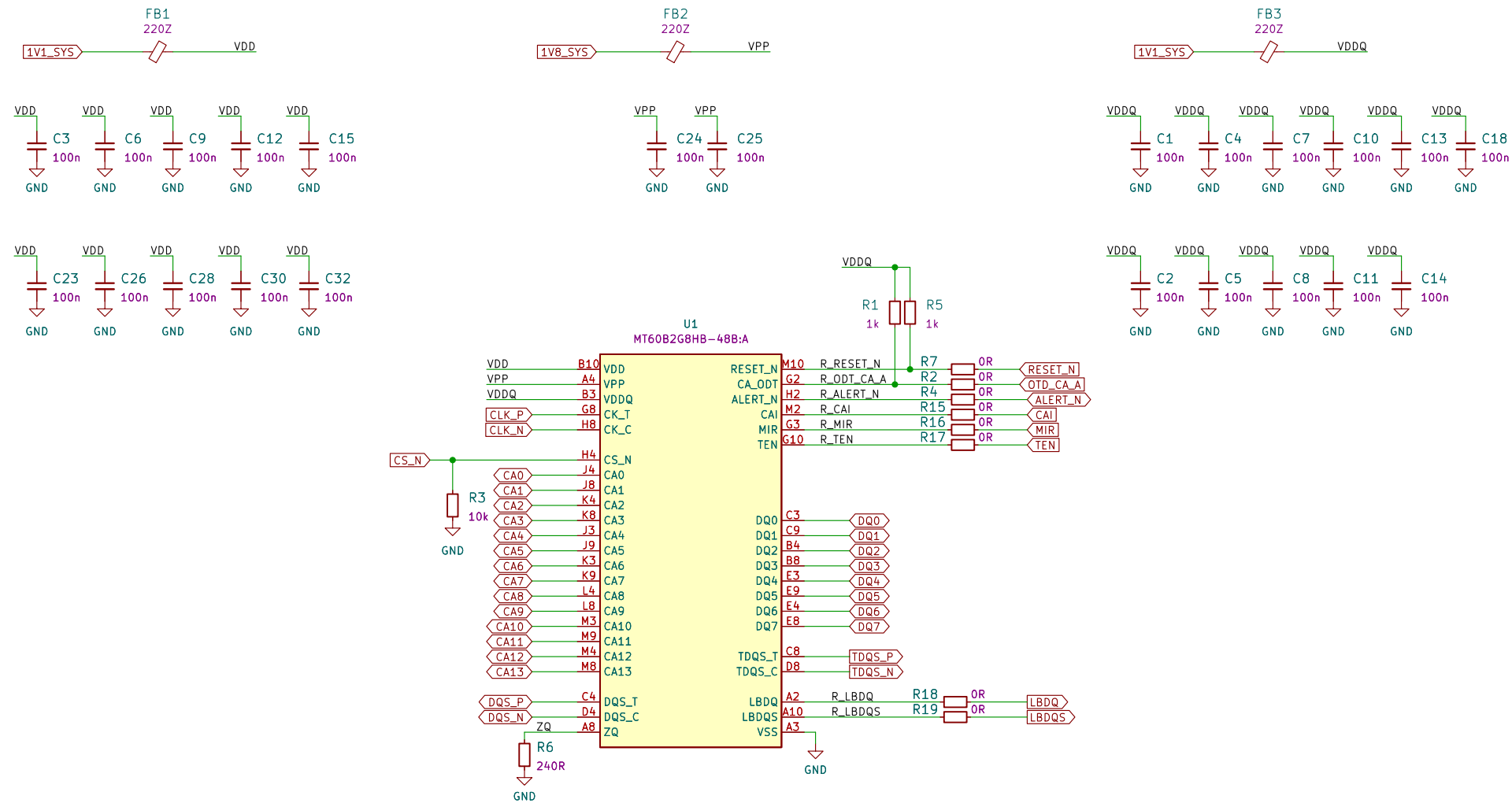
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Title: DDR5 testbed

Size: A3 Date: 2023-01-13
KiCad E.D.A. eeschema 6.0.11+dfsg-1-bpo11+1

Rev: 1.1.1
Id: 3/4

DDR5 DRAM IC



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Sheet: /DDR5/
File: ddr5.kicad_sch

Title: DDR5 testbed

Size: A3	Date: 2023-01-13
KiCad E.D.A. eeschema 6.0.11+dfsg-1~bpo11+1	

Rev: 1.1.1
Id: 4/4