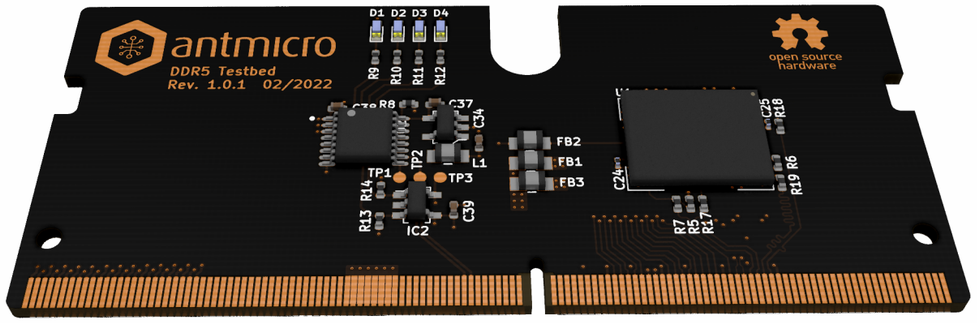
DDR5 testbed



EEPROM

File: EEPROM.kicad_sch

SODIMM

File: sodim.kicad_sch

DDR5

File: ddr5.kicad_sch

Logo N1 antmicro_logo

Logo N2 oshw_logo

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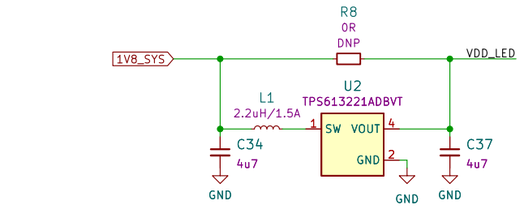
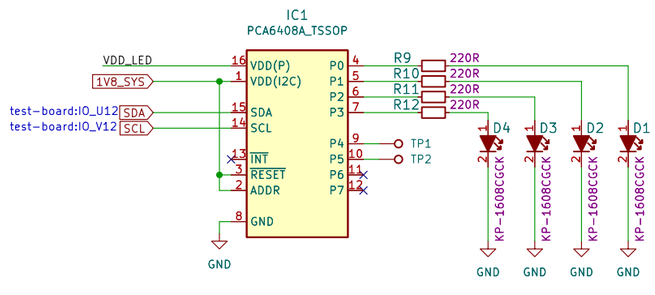
Sheet: /
File: ddr5-testbed.kicad_sch

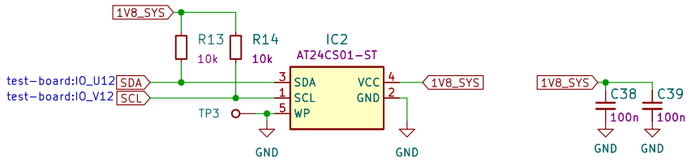
Title: DDR5 testbed

Size: A3	Date: 2023-01-13	**Rev: 1.1.1**
KiCad E.D.A.	eeschema 6.0.11+dfsg-1	Id: 1/4

I2C peripherals







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Sheet: /EEPROM/
File: EEPROM.kicad_sch

Title: DDR5 testbed

Size: A3	Date: 2023-01-13	**Rev: 1.1.1**
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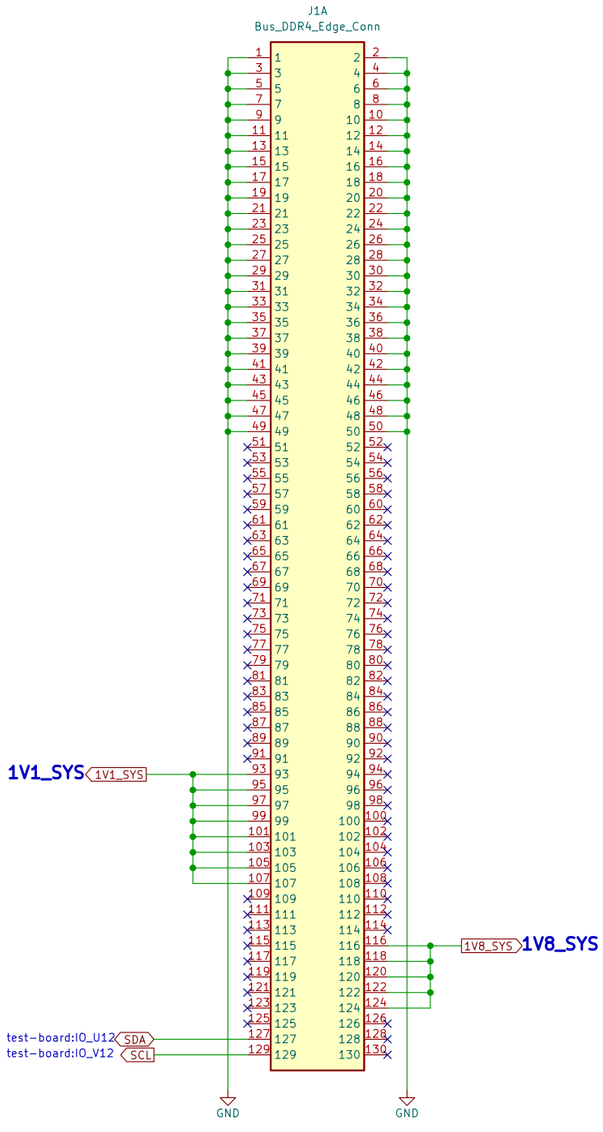
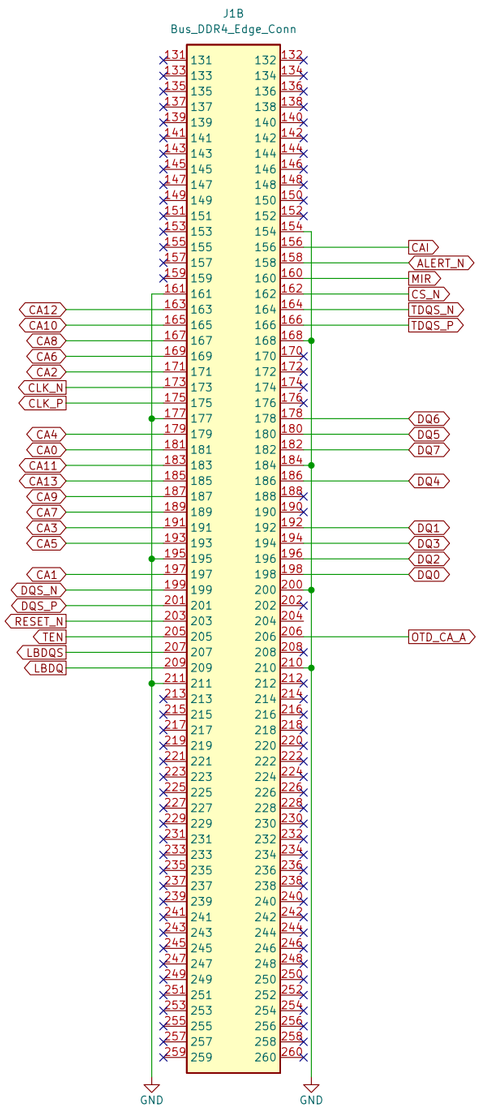
SODIMM Connector

Note:
The pin assignment for that connector matches
an experimental research platform available at
https://github.com/antmicro/lpddr4-test-board





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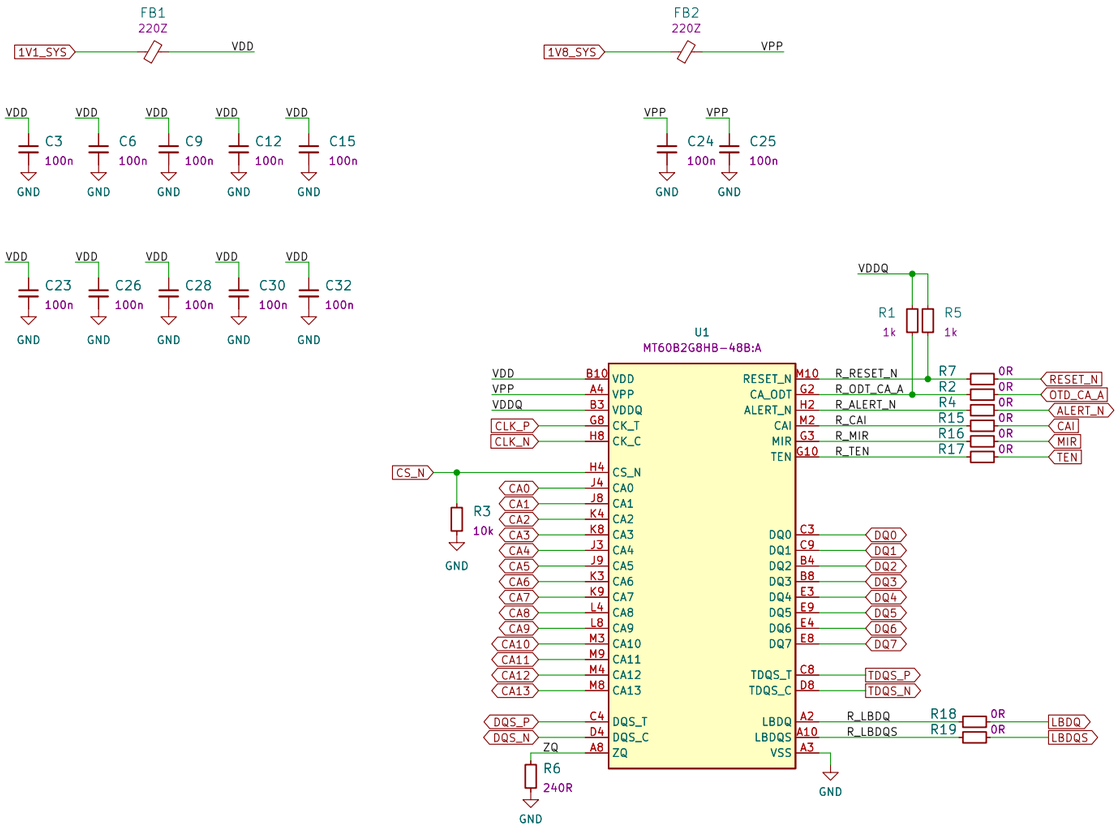
Title: DDR5 testbed

Size: A3	Date: 2023-01-13	**Rev: 1.1.1**
KiCad E.D.A. eeschema 6.0.11+dfsg-1		Id: 3/4

DDR5 DRAM IC



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Title: DDR5 testbed

Size: A3	Date: 2023-01-13	**Rev: 1.1.1**
KiCad E.D.A. eeschema 6.0.11+dfsg-1		Id: 4/4