DDR5 testbed



EEPROM File: EEPROM.kicad\_sch File: sodim.kicad\_sch

File: ddr5.kicad\_sch

open source hardware

Logo N1
antmicro\_logo
N2
Logo oshw\_logo

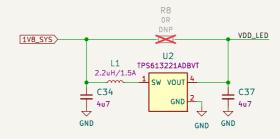
Antmicro Ltd. www.antmicro.com

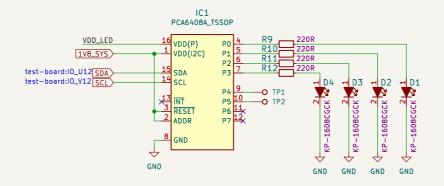
Sheet: / File: ddr5-testbed.kicad\_sch

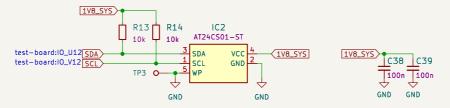
Title: DDR5 testbed

Size: A3 Date: 2024-05-27 KiCad E.D.A. kicad-cli 7.0.11 Rev: 1.1.2:004e8

I2C peripherals







spen source hardware spen source

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Sheet: /EEPROM/ File: EEPROM.kicad\_sch

Title: DDR5 testbed

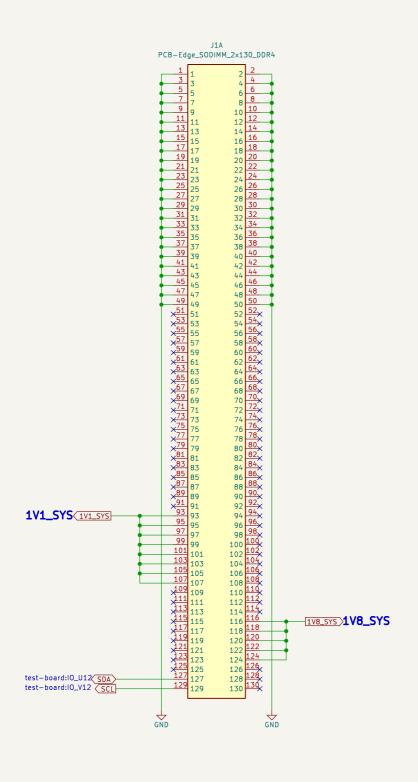
 Size: A3
 Date: 2024-05-27
 Rev: 1.1.2:004e8

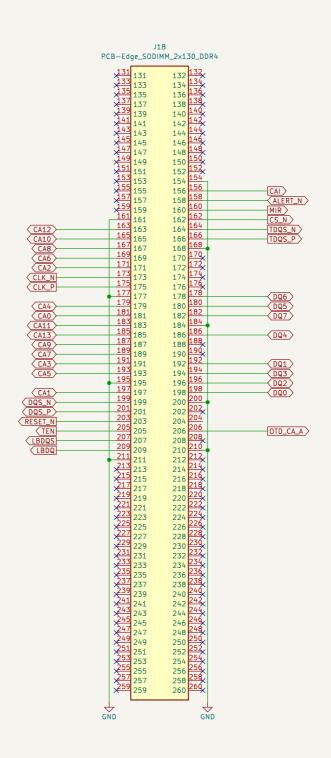
 KiCad E.D.A. kicad-cli 7.0.11
 Id: 2/4

## **SODIMM Connector**

Note

The pin assignment for that connector matches an experimental research platform available at https://github.com/antmicro/lpddr4-test-board







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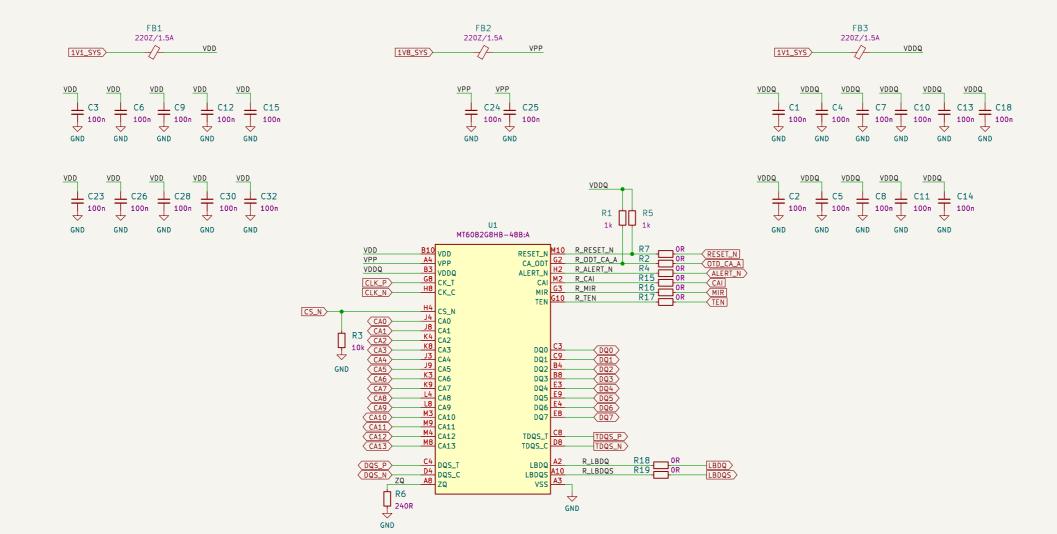
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Sheet: /SODIMM/
File: sodim.kicad\_sch

Title: DDR5 testbed

Size: A3 Date: 2024-05-27 Rev: 1.1.2:004el
KiCad E.D.A. kicad-cli 7.0.11 Id: 3/4

## DDR5 DRAM IC





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Sheet: /DDR5/ File: ddr5.kicad\_sch

Title: DDR5 testbed

Size: A3 Date: 2024-05-27 KiCad E.D.A. kicad-cli 7.0.11

Rev: 1.1.2:004e