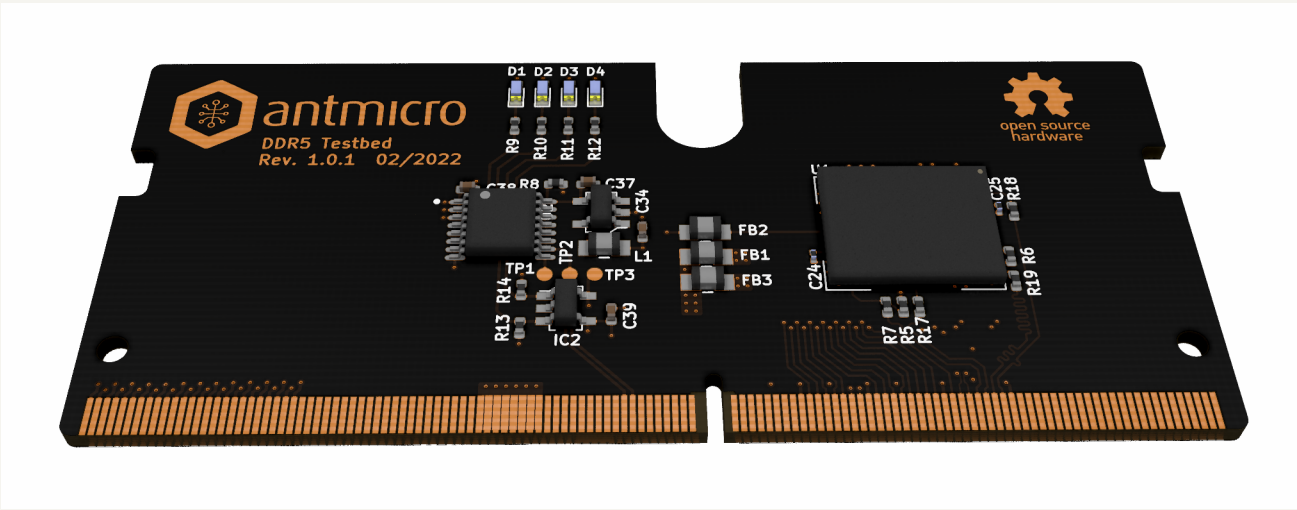


DDR5 testbed



EEPROM



File: EEPROM.kicad_sch

SODIMM



File: sodim.kicad_sch

DDR5



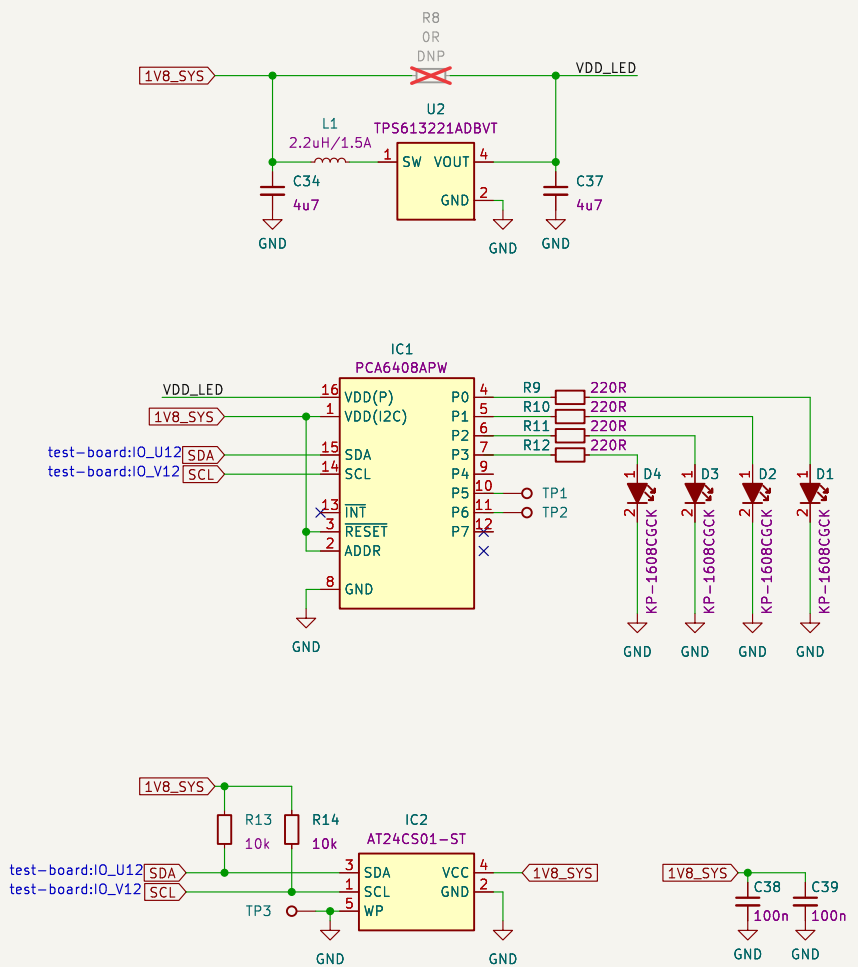
File: ddr5.kicad_sch



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Sheet: / File: ddr5-testbed.kicad_sch		
Title: DDR5 testbed		
Size: A3	Date: 2024-05-27	Rev: 1.1.2:a7365
KiCad E.D.A. kicad-cli 7.0.11	Id: 1/4	

N1
antmicro_logo
N2
oshw_logo

I2C peripherals



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Sheet: /EEPROM/
File: EEPROM.kicad_sch

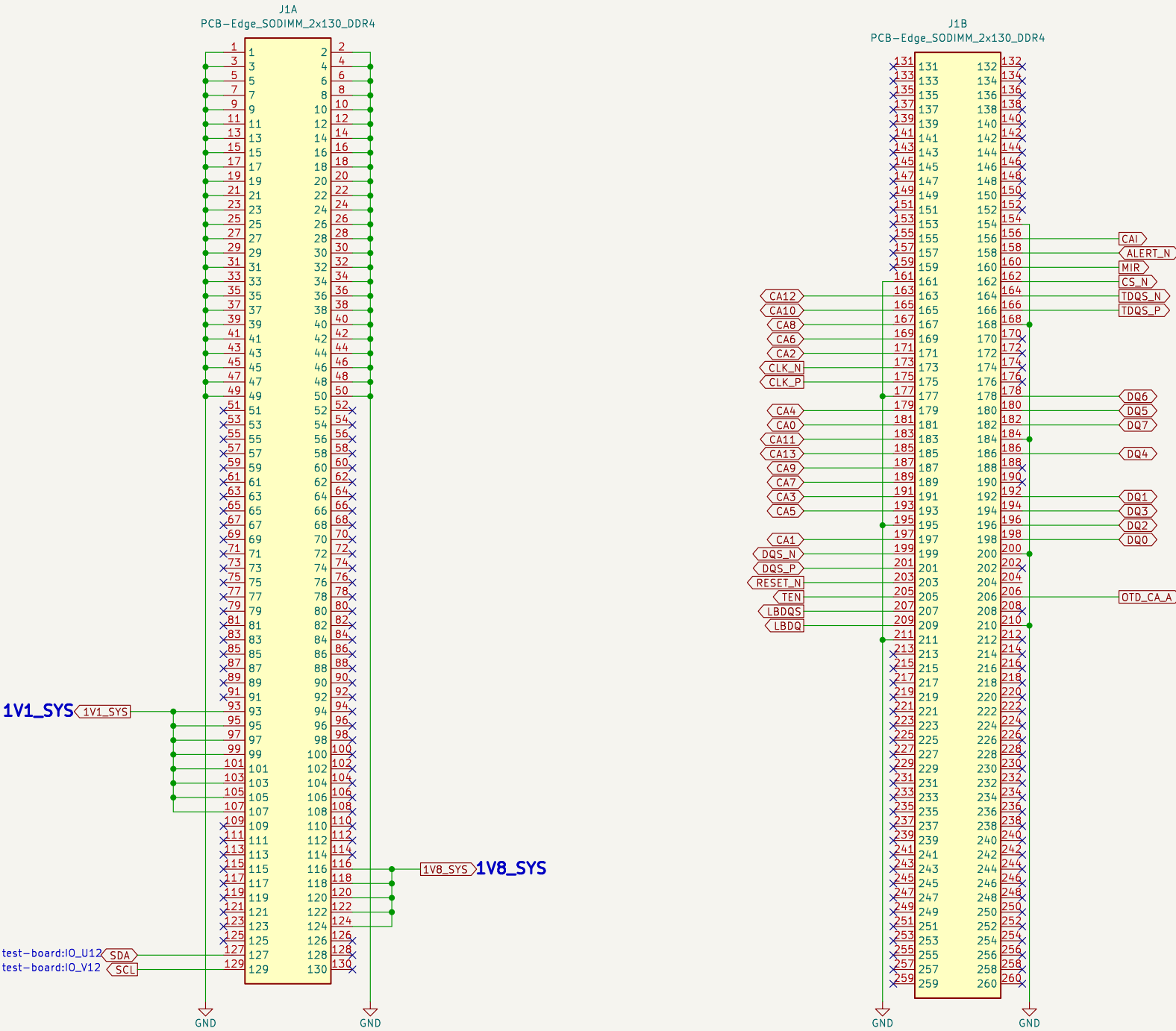
Title: DDR5 testbed

Size: A3 Date: 2024-05-27
KiCad E.D.A. kicad-cli 7.0.11

Rev: 1.1.2:a7365
Id: 2/4

SODIMM Connector

Note:
The pin assignment for that connector matches
an experimental research platform available at
<https://github.com/antmicro/lpddr4-test-board>



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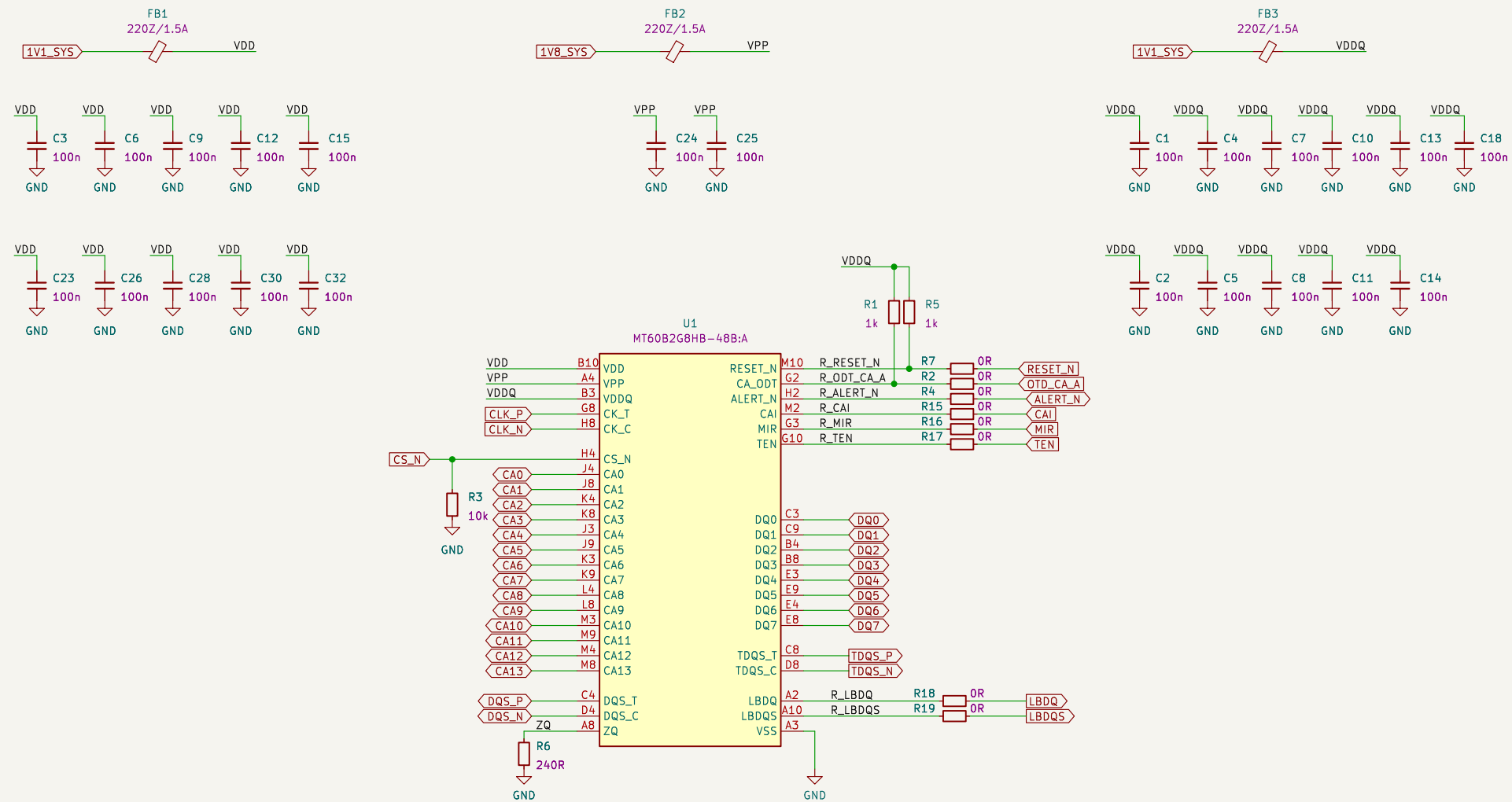
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File: sodim.kicad_sch

Title: DDR5 testbed

Size: A3 Date: 2024-05-27
KiCad E.D.A. kicad-cli 7.0.11

Rev: 1.1.2:a7365
Id: 3/4

DDR5 DRAM IC



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Sheet: /DDR5/
File: ddr5.kicad_sch

Title: DDR5 testbed

Size: A3	Date: 2024-05-27
KiCad E.D.A. kicad-cli 7.0.11	

Rev: 1.1.2:a7365
Id: 4/4