

LPDDR4 testbed

EEPROM



File: EEPROM.kicad_sch

SODIMM



File: sodim.kicad_sch

LPDDR4

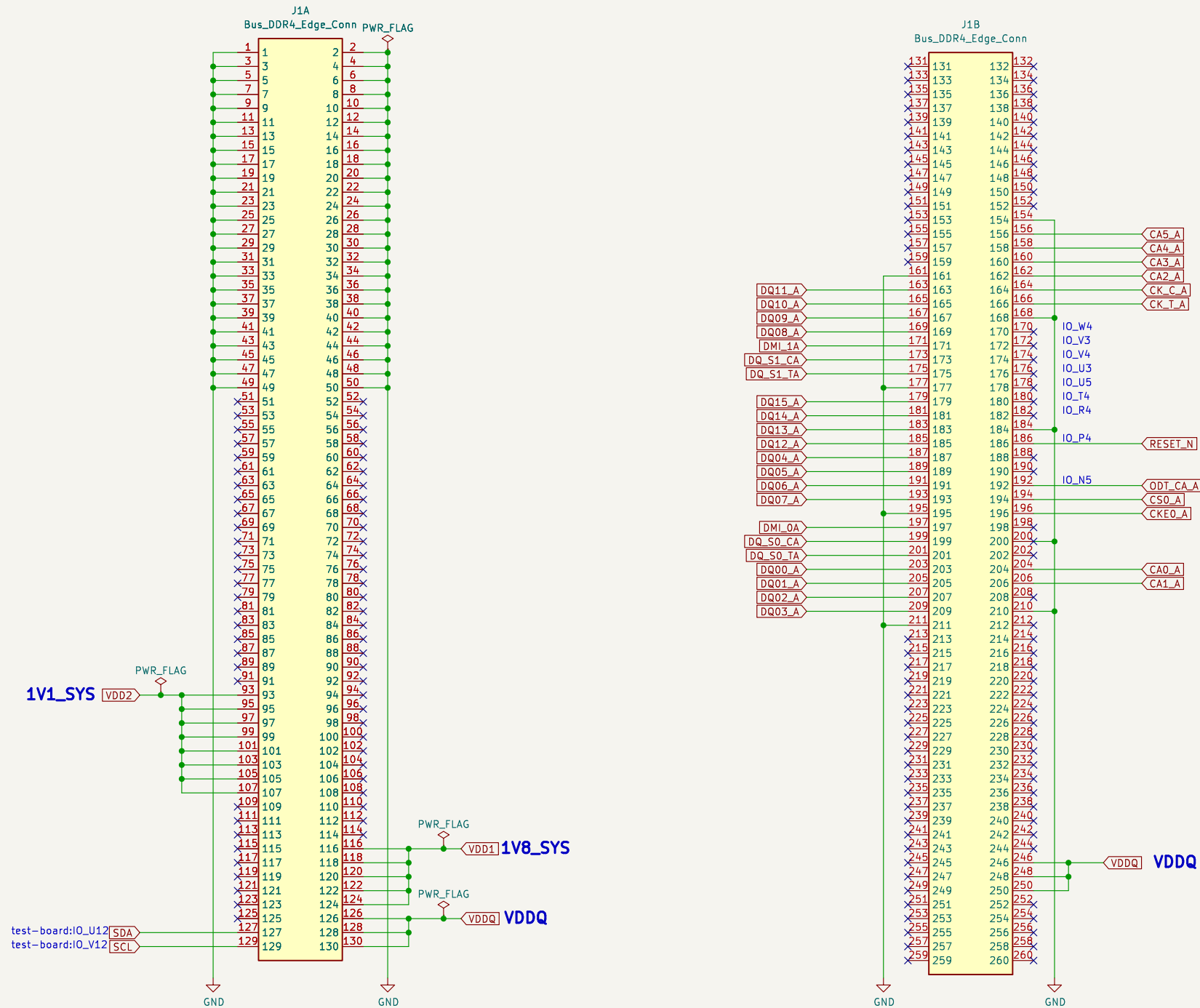


File: lpddr4.kicad_sch



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File: lpddr4-testbed.kicad_sch		
Title: LPDDR4 testbed		
Size: A3	Date: 2024-03-26	Rev: 1.2.2:08675
KiCad E.D.A. kicad-cli 7.0.11		Id: 1/4

SODIMM Connector



LPDDR4

The diagram illustrates the electrical connections for two LPDDR4 memory chips, U1A and U1B, in a testbed configuration. Both chips are MT53E1G32D2NP-046 WT:A.

Chip U1A Connections:

- Power:** VDDQ is connected to pins B10, T11, F1, and A4. VDD1 is connected to pin J8. VDD2 is connected to pins J9 and H4.
- Ground:** Multiple 100nF capacitors (C1-C10, C23-C36, C24-C27) are connected to ground.
- Control Signals:** RESET_N is connected to pin T11. CK_T_A, CK_C_A, and CS0_A are connected to pins J8, J9, and H4 respectively.
- Data Signals:** DQ0_A through DQ15_A are connected to pins B2 through C10. DQS0_T_A, DQS1_T_A, and DMIO_A are connected to pins D3, D10, and C3 respectively.
- Other:** ODT_CA_A is connected to pin G2. ZQ0 is connected to pin A5. VSS is connected to pin A10.

Chip U1B Connections:

- Power:** VDDQ is connected to pins AA10, T4, and AB4. VDD1 is connected to pins P8 and P9. VDD2 is connected to pins R4 and T2.
- Ground:** Multiple 100nF capacitors (C11-C21, C29-C31, C3-C22) are connected to ground.
- Control Signals:** CS0_B is connected to pin R3. CK_T_B, CK_C_B, and CS0_B are connected to pins P8, P9, and R4 respectively.
- Data Signals:** DQ0_B through DQ15_B are connected to pins W3 through Y10. DQS0_T_B, DQS1_T_B, and DMIO_B are connected to pins W3, W10, and Y3 respectively.
- Other:** ODT_CA_B is connected to pin T2. VSS is connected to pin AB10.

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