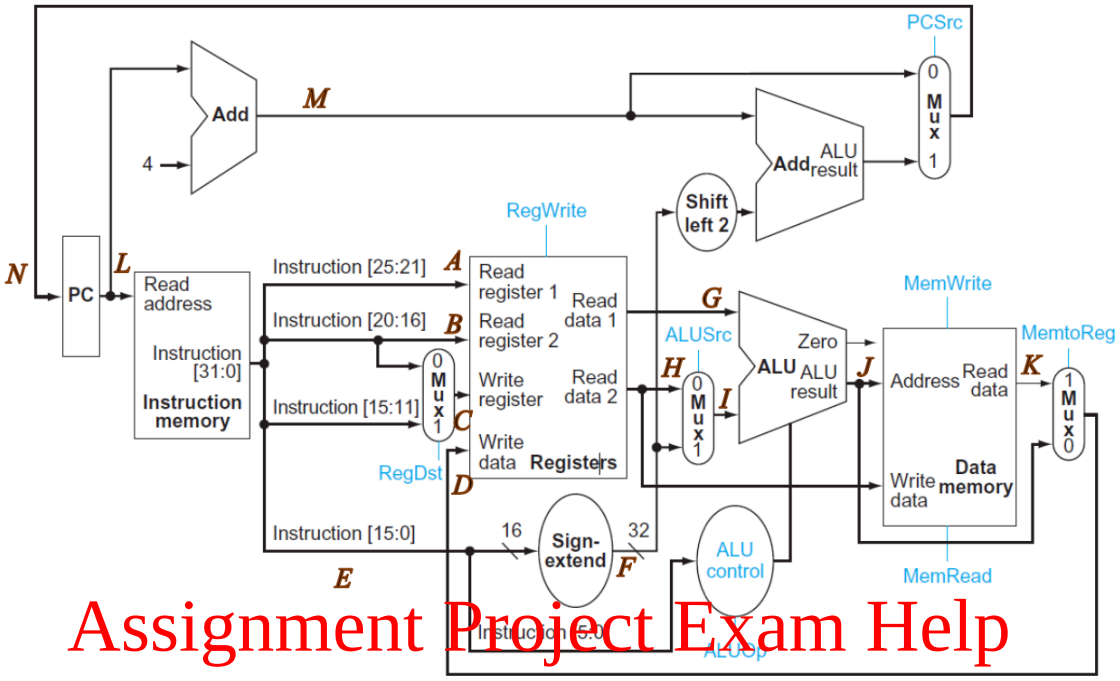
Given the following basic single-cycle CPU model, answer the following questions:



1. Given that: (a) registers **$a0 = -128** and **$s0 = 130**, and (b) the instruction at the input is **add $t0, $s0, $a0**, and (c) the instruction is in memory address **0x00404400**,
   a. what are the values for wires/buses **A** thru **N**? Give all your answers in an appropriately-sized hexadecimal.
   b. what are the values of the controls **RegDst**, **RegWrite**, **ALUSrc**, **Zero**, **MemRead**, **MemWrite**, **MemtoReg**, **PCSrc**?
   c. what operation is the ALU performing (not the code, but the function)?
2. Same as (1) for the next instruction in memory, which is **addi $v0, $a3, 510**, where **$v0** = 3, **$a3** = 2.
3. Same as (2) for the next instruction in memory, which is **sw $t3, 44($t4)**, where **$t3** = 7, **$t4** = 0x70000004.

4. Assume that logic blocks needed to implement a processor's datapath, like the one in the figure above in Question 1, have the following latencies:

   Inst.Mem = 200 ps
   Add = 70 ps
   Mux = 20 ps
   ALU = 90 ps
   Regs = 90 ps
   DataMem. = 250 ps
   Sign-Ext. = 15 ps
   Shift-Left-2 = 10 ps

   a. If the only thing we need to do in a processor is fetch consecutive instructions, what would the cycle time be?
   b. What would the cycle time be for an **add** instruction? for an **andi** instruction? for a **sw** instruction?
   c. Could we utilize a clock whose speed is 2.0 GHz for this design? Why or why not?

5. Assume a single-cycle design CPU fetches the following instruction word: **10101100011000100000000000010100**, which resides in memory address **0x00511234**. Assume that data memory is all zeros and that the processor's registers (as referenced by their MIPS register numbers) have the following values at the beginning of the cycle in which the above instruction word is fetched:

   r0 = 0, r1 = -1, r2 = 2, r3 = 3, r4 = -4, r5 = 10, r6 = 6, r8 = 8, r12 = 2 r31 = -16

   a. What is the MIPS instruction that was fetched?
   b. What function, if any, is the ALU performing for this instruction?
   c. What is the new PC address after this instruction is executed?
   d. What are the values of all 4 data inputs for the "Registers" unit? Give your answer in appropriate-length hexadecimals and use **X** for don't care values.

6. Assume that the individual stages of a MIPS CPU datapath have the following latencies:

   IF = 250 ps, **ID** = 350 ps, **EX** = 150 ps, **MEM** = 300 ps, **WB** = 200 ps

   a. What is the clock cycle time in a pipelined and non-pipelined processor?
   b. What is the approximate clock cycle speed-up from non-pipelined to pipelined?

7. Assume a 5-stage pipelined MIPS datapath that takes the following instructions:

```
add $t5, $t2, $t1
lw $t3, 4($t5)
lw $t2, 0($t2)
or $t3, $t5, $t3
sw $t3, 0($t5)
```

   a. Identify all hazards (all types).
   b. If the hardware does not have hazard or forwarding detection, (manually) insert **nop** instructions to ensure correct execution.
   c. Draw a multiple-clock-cycle diagram like the generalized one shown here (or something like **Figure 4.52**, on **Page 305** in the book) and show all the forwards and stalls, if any, needed to have in order to correctly execute these instructions.