1. What is the die yield of a silicon wafer with 800 dies, if (separate cases below):
    a. 88 of them do not work?
    b. 700 of them do work?
    c. 15% of them fail initial tests and then 15% of the remaining ones fail secondary tests?

2. A CPU runs at ***X***. If you are told that the average CPI is ***Y***, and that the number of instructions in a program is ***Z***, then how fast will this CPU execute this program, given that:
    a. X = 1.0 GHz, Y = 2.2, Z = 1,000
    b. X = 500 MHz, Y = 1.3, Z = 1,000,000
    c. X = 5.0 GHz, Y = 1.0, Z = 1,000,000

3. If you want to improve a partial design within your CPU by a factor of **5**, then by how much do you improve the entire CPU performance? Given that the improved part of your CPU used to provide 80% of your entire CPU performance.

4. What are the MIPS instructions (in hex) for:
    a. `nor $t0, $s1, $s2`
    b. `addi $v0, $t4, -77`
    c. `lw $t1, 4($t2)`

5. What would have to happen to the I-type instructions if the MIPS architecture were re-designed to have 16 registers instead of 32, but the opcodes were kept exactly as they were and the MIPS instructions remained 32 bits long?

6. What is the decimal number expressed in these IEEE-754 single-precision floating point numbers?
    a. 0x43800000
    b. 0xC3002000
    c. 0xBEE00000

4. Assume that logic blocks needed to implement a processor's datapath, like the one in the figure above in Question 1, have the following latencies:

   Inst.Mem = 200 ps
   Add = 70 ps
   Mux = 20 ps
   ALU = 90 ps
   Regs = 90 ps
   DataMem. = 250 ps
   Sign-Ext. = 15 ps
   Shift-Left-2 = 10 ps

   a. If the only thing we need to do in a processor is fetch consecutive instructions, what would the cycle time be?
   b. What would the cycle time be for an **add** instruction? for an **andi** instruction? for a **sw** instruction?
   c. Could we utilize a clock whose speed is 2.0 GHz for this design? Why or why not?

5. Assume a single-cycle design CPU fetches the following instruction word: **10101100011000100000000000010100**, which resides in memory address **0x005f1234**. Assume that data memory is all zeros and that the processor's registers (as referenced by their MIPS register numbers) have the following values at the beginning of the cycle in which the above instruction word is fetched:

   r0 = 0, r1 = -1, r2 = 2, r3 = 3, r4 = -4, r5 = 10, r6 = 6, r8 = 8, r12 = 2 r31 = -16

   a. What is the MIPS instruction that was fetched?
   b. What function, if any, is the ALU performing for this instruction?
   c. What is the new PC address after this instruction is executed?
   d. What are the values of all 4 data inputs for the "Registers" unit? Give your answer in appropriate-length hexadecimals and use **X** for don't care values.

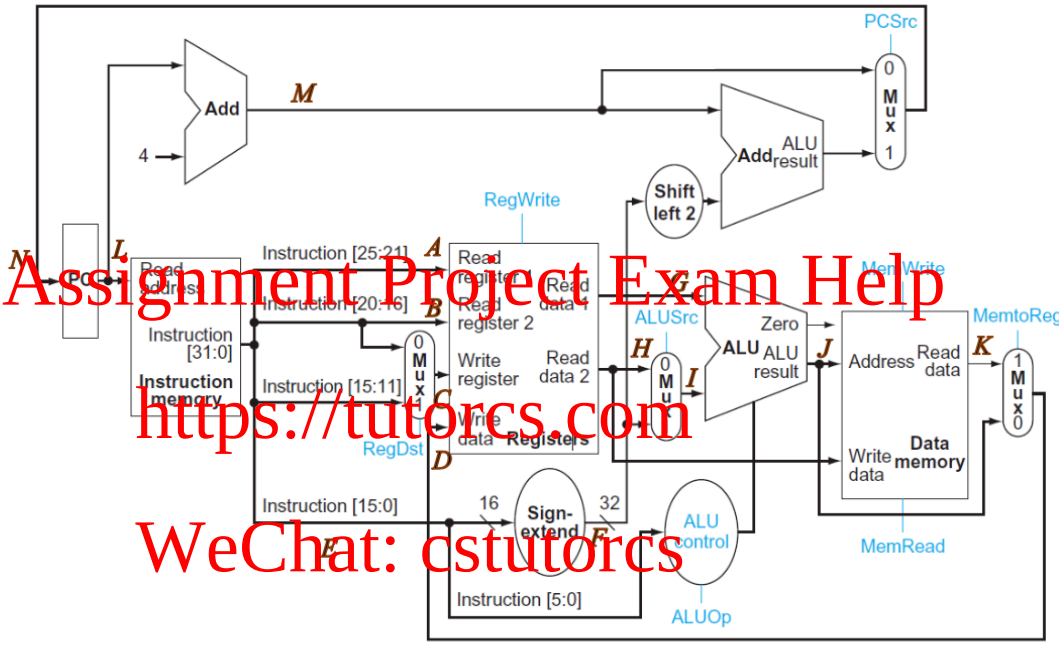
6. Assume that the individual stages of a MIPS CPU datapath have the following latencies:

   IF = 250 ps, **ID** = 350 ps, **EX** = 150 ps, **MEM** = 300 ps, **WB** = 200 ps

   a. What is the clock cycle time in a pipelined and non-pipelined processor?
   b. What is the approximate clock cycle speed-up from non-pipelined to pipelined?

7. Express the IEEE-754 single-precision floating point number for:
   a. 12.25
   b. -0.625
   c. 11.5
   d. 160.5

8. Given the following basic single-cycle CPU model, answer the following questions:



Given that: (a) registers **$a0 = -128** and **$s0 = 130**, and (b) the instruction at the input is **add $t0, $s0, $a0**, and (c) the instruction is in memory address **0x00404400**,
   a. what are the values for wires/buses **A** thru **N**? Give all your answers in an appropriately-sized hexadecimal.
   b. what are the values of the controls **RegDst**, **RegWrite**, **ALUSrc**, **Zero**, **MemRead**, **MemWrite**, **MemtoReg**, **PCSrc**?
   c. what operation is the ALU performing (not the code, but the function)?

9. Same as above for the next instruction in memory, which is **addi $v0, $a3, 510**, where **$v0** = 3, **$a3** = 2.

10. Same as above for the next instruction in memory, which is **sw $t3, 44($t4)**, where **$t3** = 7, **$t4** = 0x70000004.

11. Assume that logic blocks needed to implement a processor's datapath, like the one in the figure above, have the following latencies:

    Inst.Mem = 200 ps
    Add = 70 ps
    Mux = 20 ps
    ALU = 90 ps
    Regs = 90 ps
    DataMem. = 250 ps
    Sign-Ext. = 15 ps
    Shift-Left-2 = 10 ps

    a. What would the cycle time be for an **add** instruction? for an **andi** instruction? for a **sw** instruction?
    b. Could we utilize a clock whose speed is 2.0 GHz for this design? Why or why not?

12. Assume a single-cycle design CPU fetches the following instruction word: **10101100011000100000000000010100**, which resides in memory address **0x00511234**. Assume that data memory is all zeros and that the processor's registers (as referenced by their MIPS register numbers) have the following values at the beginning of the cycle in which the above instruction word is fetched:

    r0 = 0, r1 = -1, r2 = 2, r3 = 3, r4 = -4, r5 = 10, r6 = 6, r8 = 8, r12 = 2, r31 = -16

    a. What is the MIPS instruction that was fetched?
    b. What function, if any, is the ALU performing for this instruction?
    c. What is the new PC address after this instruction is executed?
    d. What are the values of all 4 data inputs for the "Registers" unit? Give your answer in appropriate-length hexadecimals and use **X** for don't care values.

13. Assume that the individual stages of a MIPS CPU datapath have the following latencies:

    IF = 250 ps, **ID** = 350 ps, **EX** = 150 ps, **MEM** = 300 ps, **WB** = 200 ps

    a. What is the clock cycle time in a pipelined and non-pipelined processor?
    b. What is the approximate clock cycle speed-up from non-pipelined to pipelined?