





## Design Rules Verification Report

Filename : U:\dev\distance\_sensor\pcb\distance\_sensor\distance\_sensor.PcbDoc

Warnings 0  
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=6mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ( All )	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=5mil) (Max=100mil) (Preferred=10mil) (All)	0
Routing Layers(All)	0
Routing Via (Templates Used To Check Via: GND_PIN, GND_VIA, PWR_VIA, SIGNAL_VIA) (All)	0
Power Plane Connect Rule(Relief Connect )(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Hole Size Constraint (Min=11.811mil) (Max=137.795mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=3.937mil) (All),(All)	0
Silk To Solder Mask (Clearance=10mil) (False),(All)	0
Silk to Silk (Clearance=10mil) (False),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Board Clearance Constraint (Gap=0mil) ((Not Layer='Top Overlay') And (Not Layer='Bottom Overlay'))	0
Matched Lengths(Delay Tolerance=100ps) (InDifferentialPair('USB_D'))	0
Component Clearance Constraint ( Horizontal Gap = 6mil, Vertical Gap = 10mil ) (All),(All)	0
Height Constraint (Min=0mil) (Max=39370.079mil) (Preferred=500mil) (All)	0
Total	0

Electrical Rules Check Report

Class	Document	Message
		Successful Compile for