







Comment	Description	Designator	Footprint	LibRef	Quantity
10u	MLCC	C1	CAP0805_2012	CAP_CERAMIC	1
2.2u	MLCC	C2, C3	CAP0805_2012	CAP_CERAMIC	2
1u	MLCC	C4	CAP 0603_1608	CAP_CERAMIC	1
100n	MLCC	C5	CAP0805_2012	CAP_CERAMIC	1
100n	MLCC	C6, C7, C8	CAP 0603_1608	CAP_CERAMIC	3
	LED	D1, D2	SMT_LED 0603_RED	LED	2
RCWL-1670		ß	JST_PH_4WAY	RCWL-1670	1
MOSFET-NP	N/P Channel MOSFET	Q1	DMG6601LVT	MOSFET-NP	1
MOSFET-P	P Channel MOSFET. 300mA	Q2	SOT95P230X110-3L	MOSFET-P	1
MOSFET-N	N Channel MOSFET. 300mA	Q3	SOT95P230X110-3L	MOSFET-N	1
20K	Resistor	R1, R2, R4, R5	RES 0603_1608	RESISTOR	4
10K	Resistor	R3, R6, R9, R11, R17, R18	RES 0603_1608	RESISTOR	6
22r	Resistor	R7, R10, R13, R14, R15, R16	RES 0603_1608	RESISTOR	6
4.7K	Resistor	R8, R12	RES 0603_1608	RESISTOR	2
4-1437565-1	6x6mm SMD tactile switch,SPST-NO	S1	FSM-SWTCH	BUTTON	1
LDO	5v LDO, 100mA, LDO SOT23	U1, U2	SOT95P230X110-3L	LDO_5V, LDO	2
CH32V003	MCU	U3	TSOP20-127P600-8N	CH32V003	1
ESP8266 ESP-12-E	WiFi Module	U4	ESP8266 ESP-12-E	ESP8266 ESP-12-E	1
TXB0104	Level shifter	U5	TSOP14-127P600-8N	TXB0104	1

Design Rules Verification Report
Filename: U:\dev\distance_sensor\pcb\distance_sensor\distance_sensor.PcbDo

Warnings 0 Rule Violations 0

Warnings Total

Rule Violations	
Clearance Constraint (Gap=5mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No	0
Width Constraint (Min=5mil) (Max=100mil) (Preferred=10mil) (All	0
Routing Layers(All)	0
Routing Via (Templates Used To Check Via: GND_PIN, GND_VIA, PWR_VIA, SIGNAL_VIA) (All	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4	0
Minimum Annular Ring (Minimum=5.118mil) (All	0
Hole Size Constraint (Min=11.811mil) (Max=137.795mil) (All	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=3.937mil) (All),(All	0
Silk To Solder Mask (Clearance=10mil) (False),(All)	0
Silk to Silk (Clearance=10mil) (False),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Board Clearance Constraint (Gap=0mil) ((Not Layer='Top Overlay') And (Not Layer='Bottom Overlay')	0
Matched Lengths(Delay Tolerance=100ps) (InDifferentialPair('USB_D')	0
Component Clearance Constraint (Horizontal Gap = 6mil, Vertical Gap = 10mil) (All),(All)	0
Height Constraint (Min=0mil) (Max=39370.079mil) (Prefered=500mil) (All	0
Total	0

Electrical Rules Check Report

Class	Document	Message
		Successful Compile for