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BATT

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DS1

ESP\_PROG

EN

VCC

TX

GND

RX

IO0

FACTORY

JLCJLCJLCJLC

## Design Rules Verification Report

Filename : U:\dev\distance\_sensor\pcb\distance\_sensor\_v2\distance\_sensor\_v2.PcbDoc

Warnings 0  
Rule Violations 0

Warnings	
Total	0

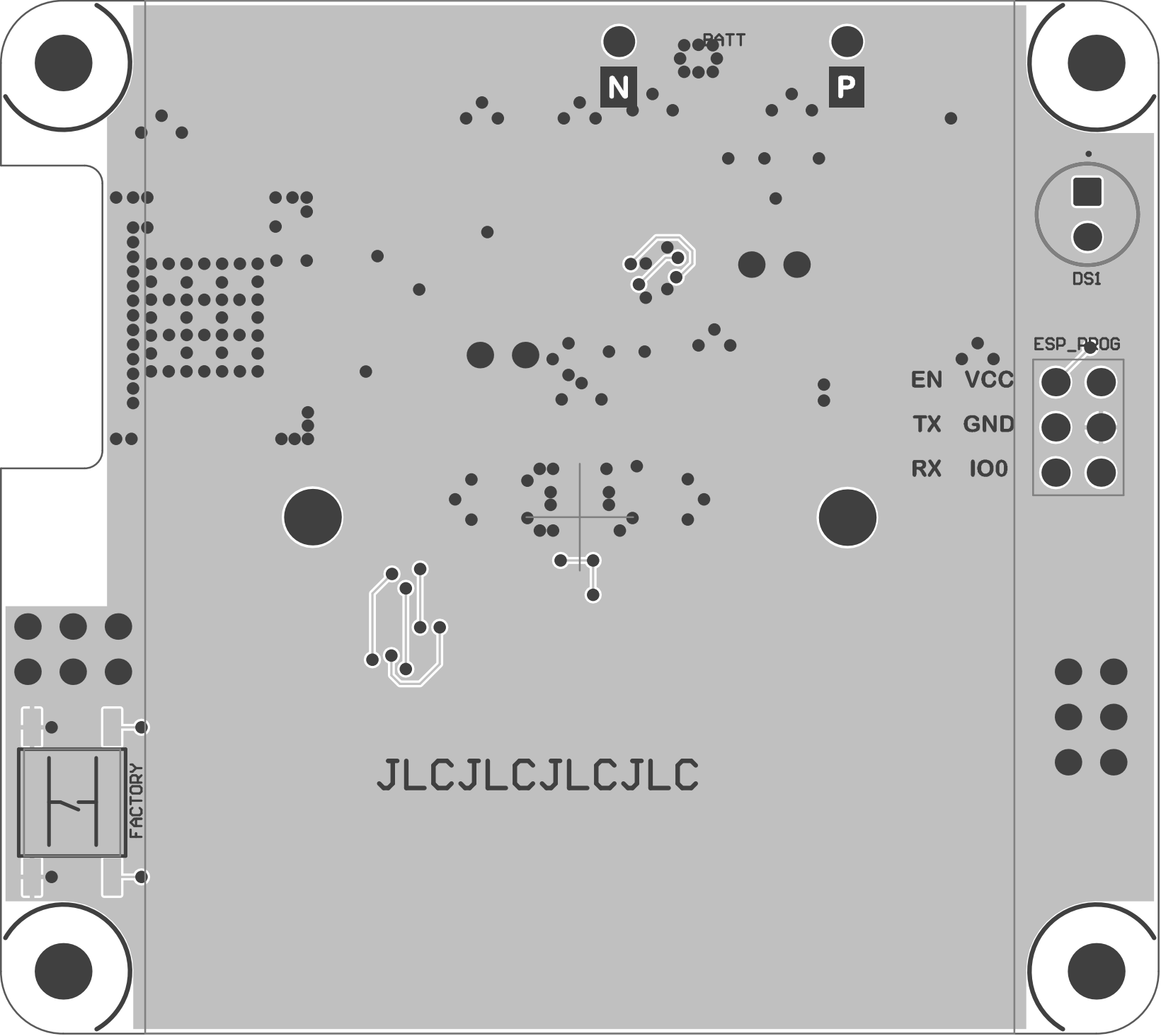
Rule Violations	
Clearance Constraint (Gap=5mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ( All )	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=5mil) (Max=50mil) (Preferred=5mil) (All)	0
Power Plane Connect Rule(Relief Connect )(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4	0
Hole Size Constraint (Min=11.811mil) (Max=196.85mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=3.15mil) (All),(All)	0
Silk To Solder Mask (Clearance=10mil) (False),(All)	0
Silk to Silk (Clearance=0mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Board Clearance Constraint (Gap=0mil) (OnSignal)	0
Height Constraint (Min=0mil) (Max=1000mil) (Preferred=500mil) (All)	0
Total	0

Electrical Rules Check Report

Class	Document	Message
		Successful Compile for







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