STM32
CubeMX

# 1. Description

## 1.1. Project

| | |
|---|---|
| Project Name | pa_ctl |
| Board Name | custom |
| Generated with: | STM32CubeMX 6.15.0 |
| Date | 11/16/2025 |

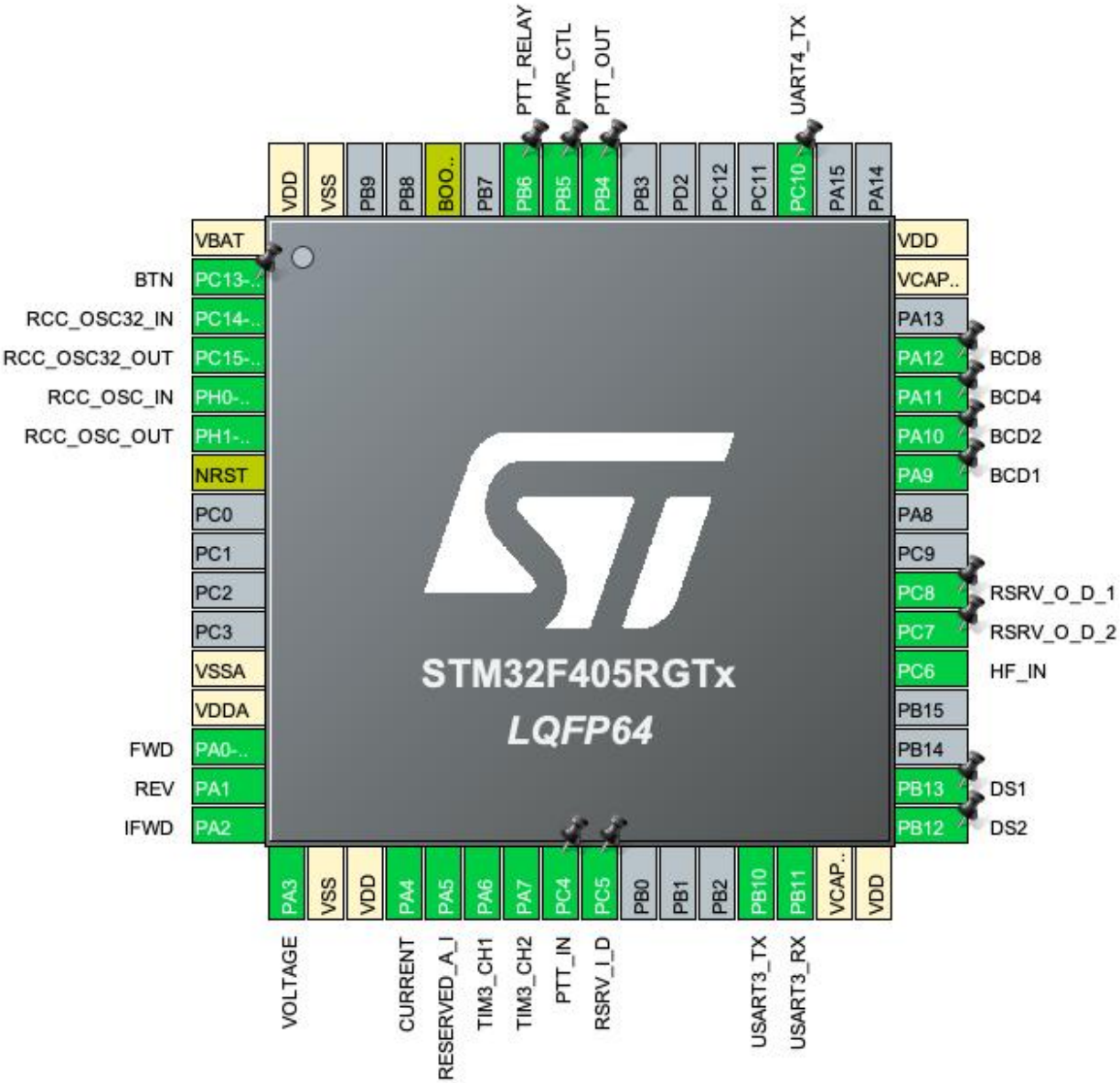
## 1.2. MCU

| | |
|---|---|
| MCU Series | STM32F4 |
| MCU Line | STM32F405/415 |
| MCU name | STM32F405RGTx |
| MCU Package | LQFP64 |
| MCU Pin number | 64 |

## 1.3. Core(s) information

| | |
|---|---|
| Core(s) | Arm Cortex-M4 |

## 2. Pinout Configuration



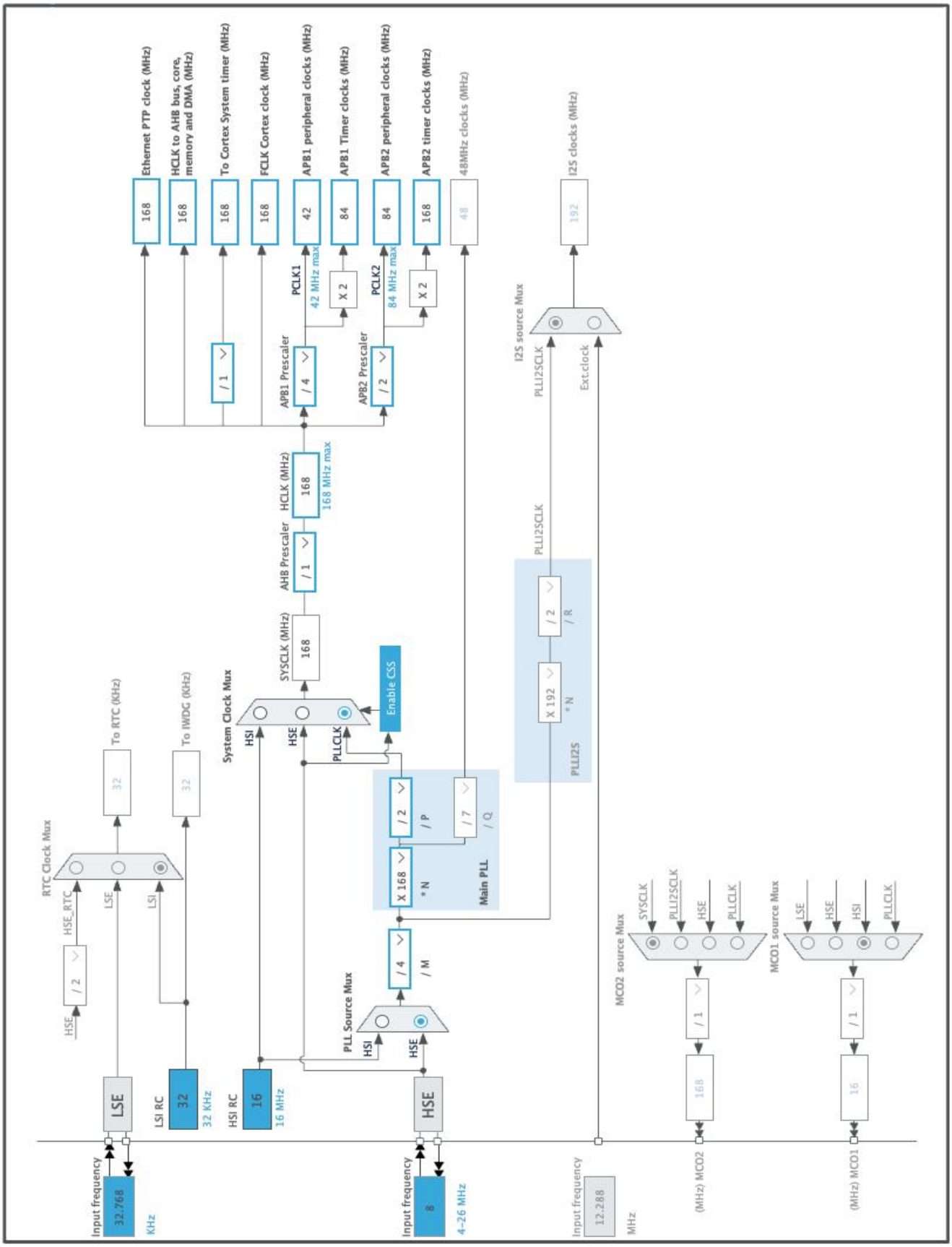
# 3. Pins Configuration

| Pin Number LQFP64 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 1 | VBAT | Power | | |
| 2 | PC13-ANTI_TAMP * | I/O | GPIO_Input | BTN |
| 3 | PC14-OSC32_IN | I/O | RCC_OSC32_IN | |
| 4 | PC15-OSC32_OUT | I/O | RCC_OSC32_OUT | |
| 5 | PH0-OSC_IN | I/O | RCC_OSC_IN | |
| 6 | PH1-OSC_OUT | I/O | RCC_OSC_OUT | |
| 7 | NRST | Reset | | |
| 12 | VSSA | Power | | |
| 13 | VDDA | Power | | |
| 14 | PA0-WKUP | I/O | ADC3_IN0 | FWD |
| 15 | PA1 | I/O | ADC3_IN1 | REV |
| 16 | PA2 | I/O | ADC2_IN2 | IFWD |
| 17 | PA3 | I/O | ADC2_IN3 | VOLTAGE |
| 18 | VSS | Power | | |
| 19 | VDD | Power | | |
| 20 | PA4 | I/O | ADC1_IN4 | CURRENT |
| 21 | PA5 | I/O | ADC1_IN5 | RESERVED_A_I |
| 22 | PA6 | I/O | TIM3_CH1 | |
| 23 | PA7 | I/O | TIM3_CH2 | |
| 24 | PC4 * | I/O | GPIO_Input | PTT_IN |
| 25 | PC5 * | I/O | GPIO_Input | RSRV_I_D |
| 29 | PB10 | I/O | USART3_TX | |
| 30 | PB11 | I/O | USART3_RX | |
| 31 | VCAP_1 | Power | | |
| 32 | VDD | Power | | |
| 33 | PB12 * | I/O | GPIO_Output | DS2 |
| 34 | PB13 * | I/O | GPIO_Output | DS1 |
| 37 | PC6 | I/O | TIM8_CH1 | HF_IN |
| 38 | PC7 * | I/O | GPIO_Output | RSRV_O_D_2 |
| 39 | PC8 * | I/O | GPIO_Output | RSRV_O_D_1 |
| 42 | PA9 * | I/O | GPIO_Output | BCD1 |
| 43 | PA10 * | I/O | GPIO_Output | BCD2 |
| 44 | PA11 * | I/O | GPIO_Output | BCD4 |
| 45 | PA12 * | I/O | GPIO_Output | BCD8 |
| 47 | VCAP_2 | Power | | |
| 48 | VDD | Power | | |

| Pin Number LQFP64 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 51 | PC10 | I/O | UART4_TX | |
| 56 | PB4 * | I/O | GPIO_Output | PTT_OUT |
| 57 | PB5 * | I/O | GPIO_Output | PWR_CTL |
| 58 | PB6 * | I/O | GPIO_Output | PTT_RELAY |
| 60 | BOOT0 | Boot | | |
| 63 | VSS | Power | | |
| 64 | VDD | Power | | |

* The pin is affected with an I/O function

# 4. Clock Tree Configuration



# 1. Power Consumption Calculator report

## 1.1. Microcontroller Selection

| | |
|---|---|
| Series | STM32F4 |
| Line | STM32F405/415 |
| MCU | STM32F405RGTx |
| Datasheet | DS8626_Rev8 |

## 1.2. Parameter Selection

| | |
|---|---|
| Temperature | 25 |
| Vdd | 3.3 |

## 1.3. Battery Selection

| | |
|---|---|
| Battery | Li-SOCL2(A3400) |
| Capacity | 3400.0 mAh |
| Self Discharge | 0.08 %/month |
| Nominal Voltage | 3.6 V |
| Max Cont Current | 100.0 mA |
| Max Pulse Current | 200.0 mA |
| Cells in series | 1 |
| Cells in parallel | 1 |

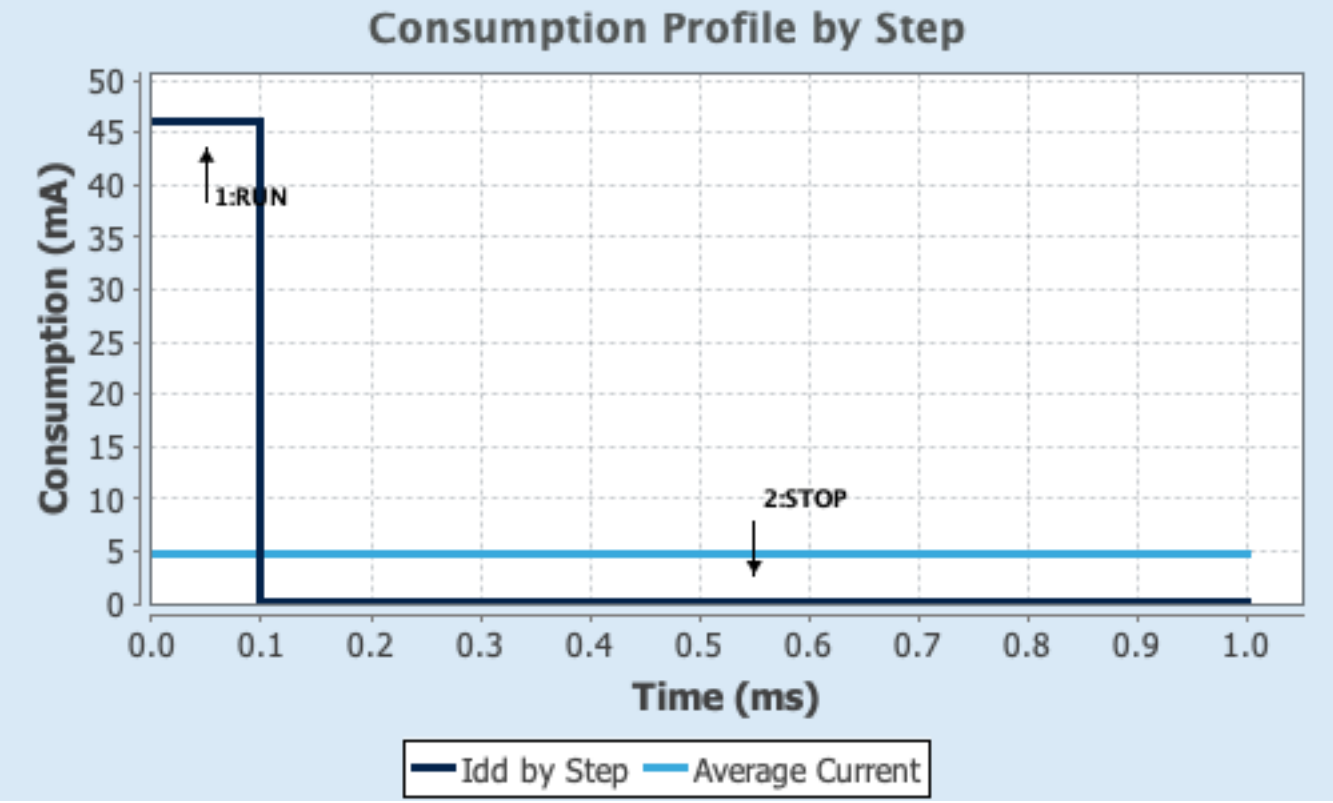
## 1.4. Sequence

| ***Step*** | Step1 | Step2 |
|---|---|---|
| ***Mode*** | RUN | STOP |
| ***Vdd*** | 3.3 | 3.3 |
| ***Voltage Source*** | Battery | Battery |
| ***Range*** | Scale1-High | No Scale |
| ***Fetch Type*** | FLASH | n/a |
| ***CPU Frequency*** | 168 MHz | 0 Hz |
| ***Clock Configuration*** | HSE PLL | Regulator_LP Flash-PwrDwn |
| ***Clock Source Frequency*** | 4 MHz | 0 Hz |
| ***Peripherals*** | | |
| ***Additional Cons.*** | 0 mA | 0 mA |
| ***Average Current*** | 46 mA | 280 µA |
| ***Duration*** | 0.1 ms | 0.9 ms |
| ***DMIPS*** | 210.0 | 0.0 |
| ***Ta Max*** | 98.02 | 104.96 |
| ***Category*** | In DS Table | In DS Table |

## 1.5. Results

| Sequence Time | 1 ms | Average Current | 4.85 mA |
|---|---|---|---|
| Battery Life | 29 days, 4 hours | Average DMIPS | 210.0 DMIPS |

## 1.6. Chart


Consumption Profile by Step
Consumption (mA)
50
45
40
35
30
25
20
15
10
5
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

# 2. Software Project

## 2.1. Project Settings

| Name | Value |
|---|---|
| Project Name | pa_ctl |
| Project Folder | /Users/enthru/STM32CubeIDE/workspace/pa_ctl |
| Toolchain / IDE | STM32CubeIDE |
| Firmware Package Name and Version | STM32Cube FW_F4 V1.28.3 |
| Application Structure | Advanced |
| Generate Under Root | Yes |
| Do not generate the main() | No |
| Minimum Heap Size | 0x200 |
| Minimum Stack Size | 0x400 |

## 2.2. Code Generation Settings

| Name | Value |
|---|---|
| STM32Cube MCU packages and embedded software | Copy only the necessary library files |
| Generate peripheral initialization as a pair of '.c/.h' files | No |
| Backup previously generated files when re-generating | No |
| Keep User Code when re-generating | Yes |
| Delete previously generated files when not re-generated | Yes |
| Set all free pins as analog (to optimize the power consumption) | No |
| Enable Full Assert | No |

## 2.3. Advanced Settings - Generated Function Calls

| Rank | Function Name | Peripheral Instance Name |
|---|---|---|
| 1 | SystemClock_Config | RCC |
| 2 | MX_GPIO_Init | GPIO |
| 3 | MX_DMA_Init | DMA |
| 4 | MX_ADC1_Init | ADC1 |
| 5 | MX_TIM4_Init | TIM4 |
| 6 | MX_USART3_UART_Init | USART3 |
| 7 | MX_UART4_Init | UART4 |
| 8 | MX_TIM5_Init | TIM5 |
| 9 | MX_TIM3_Init | TIM3 |
| 10 | MX_TIM8_Init | TIM8 |
| 11 | MX_TIM2_Init | TIM2 |

| Rank | Function Name | Peripheral Instance Name |
|---|---|---|
| 12 | MX_ADC2_Init | ADC2 |
| 13 | MX_ADC3_Init | ADC3 |

# 3. Peripherals and Middlewares Configuration

## 3.1. ADC1

**mode: IN4**

**mode: IN5**

### 3.1.1. Parameter Settings:

**ADCs_Common_Settings:**

| | |
|---|---|
| Mode | **Triple regular simultaneous mode only *** |
| DMA Access Mode | DMA access mode 1 |
| Delay between 2 sampling phases | 5 Cycles |

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | PCLK2 divided by 4 |
| Resolution | 12 bits (15 ADC Clock cycles) |
| Data Alignment | Right alignment |
| Scan Conversion Mode | Enabled |
| Continuous Conversion Mode | **Enabled *** |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | **Enabled *** |
| End Of Conversion Selection | EOC flag at the end of single channel conversion |

**ADC_Regular_ConversionMode:**

| | |
|---|---|
| Number Of Conversion | **2 *** |
| External Trigger Conversion Source | Regular Conversion launched by software |
| External Trigger Conversion Edge | None |
| Rank | 1 |
| Channel | Channel 4 |
| Sampling Time | **56 Cycles *** |
| Rank | **2 *** |
| Channel | Channel 4 |
| Sampling Time | **56 Cycles *** |

**WatchDog:**

| | |
|---|---|
| Enable Analog WatchDog Mode | false |

## 3.2. ADC2

**mode: IN2**

**mode: IN3**

### 3.2.1. Parameter Settings:

**ADCs_Common_Settings:**

| | |
|---|---|
| Mode | **Triple regular simultaneous mode only *** |
| DMA Access Mode | DMA access mode 1 |
| Delay between 2 sampling phases | 5 Cycles |

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | PCLK2 divided by 4 |
| Resolution | 12 bits (15 ADC Clock cycles) |
| Data Alignment | Right alignment |
| Scan Conversion Mode | Enabled |
| Continuous Conversion Mode | Enabled |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | **Enabled *** |
| End Of Conversion Selection | EOC flag at the end of single channel conversion |

**ADC_Regular_ConversionMode:**

| | |
|---|---|
| Number Of Conversion | **2 *** |
| Rank | 1 |
| Channel | **Channel 3 *** |
| Sampling Time | **56 Cycles *** |
| Rank | **2 *** |
| Channel | Channel 2 |
| Sampling Time | **56 Cycles *** |

**WatchDog:**

| | |
|---|---|
| Enable Analog WatchDog Mode | false |

## 3.3. ADC3

## mode: IN0

## mode: IN1

### 3.3.1. Parameter Settings:

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | PCLK2 divided by 4 |
| Resolution | 12 bits (15 ADC Clock cycles) |
| Data Alignment | Right alignment |
| Scan Conversion Mode | Enabled |
| Continuous Conversion Mode | Enabled |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | **Enabled *** |

| | |
|---|---|
| End Of Conversion Selection | EOC flag at the end of single channel conversion |
| **ADC_Regular_ConversionMode:** | |
| Number Of Conversion | **2 *** |
| Rank | 1 |
| Channel | **Channel 1 *** |
| Sampling Time | **56 Cycles *** |
| Rank | **2 *** |
| Channel | Channel 0 |
| Sampling Time | **56 Cycles *** |
| **WatchDog:** | |
| Enable Analog WatchDog Mode | false |

## 3.4. RCC

**High Speed Clock (HSE): Crystal/Ceramic Resonator**

**Low Speed Clock (LSE) : Crystal/Ceramic Resonator**

### 3.4.1. Parameter Settings:

| | |
|---|---|
| **System Parameters:** | |
| VDD voltage (V) | 3.3 |
| Instruction Cache | Enabled |
| Prefetch Buffer | Enabled |
| Data Cache | Enabled |
| Flash Latency(WS) | 5 WS (6 CPU cycle) |
| **RCC Parameters:** | |
| HSI Calibration Value | 16 |
| HSE Startup Timout Value (ms) | 100 |
| LSE Startup Timout Value (ms) | 5000 |
| **Power Parameters:** | |
| Power Regulator Voltage Scale | Power Regulator Voltage Scale 1 |

## 3.5. SYS

**Timebase Source: SysTick**

## 3.6. TIM2

**Clock Source : Internal Clock**

### 3.6.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **83 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 32 bits value ) | **499 *** |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

## 3.7. TIM3

**Clock Source : Internal Clock**

**Channel1: PWM Generation CH1**

**Channel2: PWM Generation CH2**

### 3.7.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **336 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | 65535 |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

**PWM Generation Channel 1:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 2:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |

| | |
|---|---|
| CH Polarity | High |

## 3.8. TIM4

## mode: Clock Source

### 3.8.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **41999 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | **899 *** |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

## 3.9. TIM5

## mode: Clock Source

### 3.9.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **419 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 32 bits value ) | **1 *** |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

## 3.10. TIM8

## Slave Mode: External Clock Mode 1

## Trigger Source: TI1FP1

### 3.10.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | 65535 |
| Internal Clock Division (CKD) | No Division |
| Repetition Counter (RCR - 8 bits value) | 0 |
| auto-reload preload | Disable |
| Slave Mode Controller | ETR mode 1 |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

**Trigger:**

| | |
|---|---|
| Trigger Polarity | Rising Edge |
| Trigger Filter (4 bits value) | 0 |

## 3.11. UART4

## Mode: Single Wire (Half-Duplex)

### 3.11.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |

## 3.12. USART3

## Mode: Asynchronous

### 3.12.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | 8 Bits (including Parity) |
| Parity | None |

| | |
|---|---|
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |

*** User modified value**

# 4. System Configuration

## 4.1. GPIO configuration

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| ADC1 | PA4 | ADC1_IN4 | Analog mode | No pull-up and no pull-down | n/a | CURRENT |
| | PA5 | ADC1_IN5 | Analog mode | No pull-up and no pull-down | n/a | RESERVED_A_I |
| ADC2 | PA2 | ADC2_IN2 | Analog mode | No pull-up and no pull-down | n/a | IFWD |
| | PA3 | ADC2_IN3 | Analog mode | No pull-up and no pull-down | n/a | VOLTAGE |
| ADC3 | PA0-WKUP | ADC3_IN0 | Analog mode | No pull-up and no pull-down | n/a | FWD |
| | PA1 | ADC3_IN1 | Analog mode | No pull-up and no pull-down | n/a | REV |
| RCC | PC14-OSC32_IN | RCC_OSC32_IN | n/a | n/a | n/a | |
| | PC15-OSC32_OUT | RCC_OSC32_OUT | n/a | n/a | n/a | |
| | PH0-OSC_IN | RCC_OSC_IN | n/a | n/a | n/a | |
| | PH1-OSC_OUT | RCC_OSC_OUT | n/a | n/a | n/a | |
| TIM3 | PA6 | TIM3_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PA7 | TIM3_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| TIM8 | PC6 | TIM8_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | HF_IN |
| UART4 | PC10 | UART4_TX | Alternate Function Open Drain | No pull-up and no pull-down | **Very High *** | |
| USART3 | PB10 | USART3_TX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PB11 | USART3_RX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| GPIO | PC13-ANTI_TAMP | GPIO_Input | Input mode | **Pull-down *** | n/a | BTN |
| | PC4 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | PTT_IN |
| | PC5 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | RSRV_I_D |
| | PB12 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | DS2 |
| | PB13 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | DS1 |
| | PC7 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | RSRV_O_D_2 |
| | PC8 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | RSRV_O_D_1 |
| | PA9 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | BCD1 |
| | PA10 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | BCD2 |
| | PA11 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | BCD4 |
| | PA12 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | BCD8 |
| | PB4 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | PTT_OUT |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| | PB5 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | PWR_CTL |
| | PB6 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | PTT_RELAY |

## 4.2. DMA configuration

| DMA request | Stream | Direction | Priority |
|---|---|---|---|
| ADC1 | DMA2_Stream0 | Peripheral To Memory | **Medium *** |
| USART3_RX | DMA1_Stream1 | Peripheral To Memory | Low |
| ADC3 | DMA2_Stream1 | Peripheral To Memory | **Very High *** |
| ADC2 | DMA2_Stream2 | Peripheral To Memory | **High *** |

*ADC1: DMA2_Stream0 DMA request Settings:*

| | |
|---|---|
| Mode: | **Circular *** |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Half Word |
| Memory Data Width: | Half Word |

*USART3_RX: DMA1_Stream1 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

*ADC3: DMA2_Stream1 DMA request Settings:*

| | |
|---|---|
| Mode: | **Circular *** |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Half Word |
| Memory Data Width: | Half Word |

*ADC2: DMA2_Stream2 DMA request Settings:*

| | |
|---|---|
| Mode: | **Circular *** |

| | |
|---|---|
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Half Word |
| Memory Data Width: | Half Word |

## 4.3. NVIC configuration

### 4.3.1. NVIC

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|---|---|---|
| Non maskable interrupt | true | 0 | 0 |
| Hard fault interrupt | true | 0 | 0 |
| Memory management fault | true | 0 | 0 |
| Pre-fetch fault, memory access fault | true | 0 | 0 |
| Undefined instruction or illegal state | true | 0 | 0 |
| System service call via SWI instruction | true | 0 | 0 |
| Debug monitor | true | 0 | 0 |
| Pendable request for system service | true | 0 | 0 |
| System tick timer | true | 15 | 0 |
| DMA1 stream1 global interrupt | true | 0 | 0 |
| TIM4 global interrupt | true | 0 | 0 |
| USART3 global interrupt | true | 0 | 0 |
| TIM5 global interrupt | true | 0 | 0 |
| DMA2 stream0 global interrupt | true | 0 | 0 |
| DMA2 stream1 global interrupt | true | 0 | 0 |
| DMA2 stream2 global interrupt | true | 0 | 0 |
| PVD interrupt through EXTI line 16 | unused | | |
| Flash global interrupt | unused | | |
| RCC global interrupt | unused | | |
| ADC1, ADC2 and ADC3 global interrupts | unused | | |
| TIM2 global interrupt | unused | | |
| TIM3 global interrupt | unused | | |
| TIM8 break interrupt and TIM12 global interrupt | unused | | |
| TIM8 update interrupt and TIM13 global interrupt | unused | | |
| TIM8 trigger and commutation interrupts and TIM14 global interrupt | unused | | |
| TIM8 capture compare interrupt | unused | | |
| UART4 global interrupt | unused | | |
| FPU global interrupt | unused | | |

### 4.3.2. NVIC Code generation

| Enabled interrupt Table | Select for init sequence ordering | Generate IRQ handler | Call HAL handler |
|---|---|---|---|
| Non maskable interrupt | false | true | false |
| Hard fault interrupt | false | true | false |
| Memory management fault | false | true | false |
| | | | |

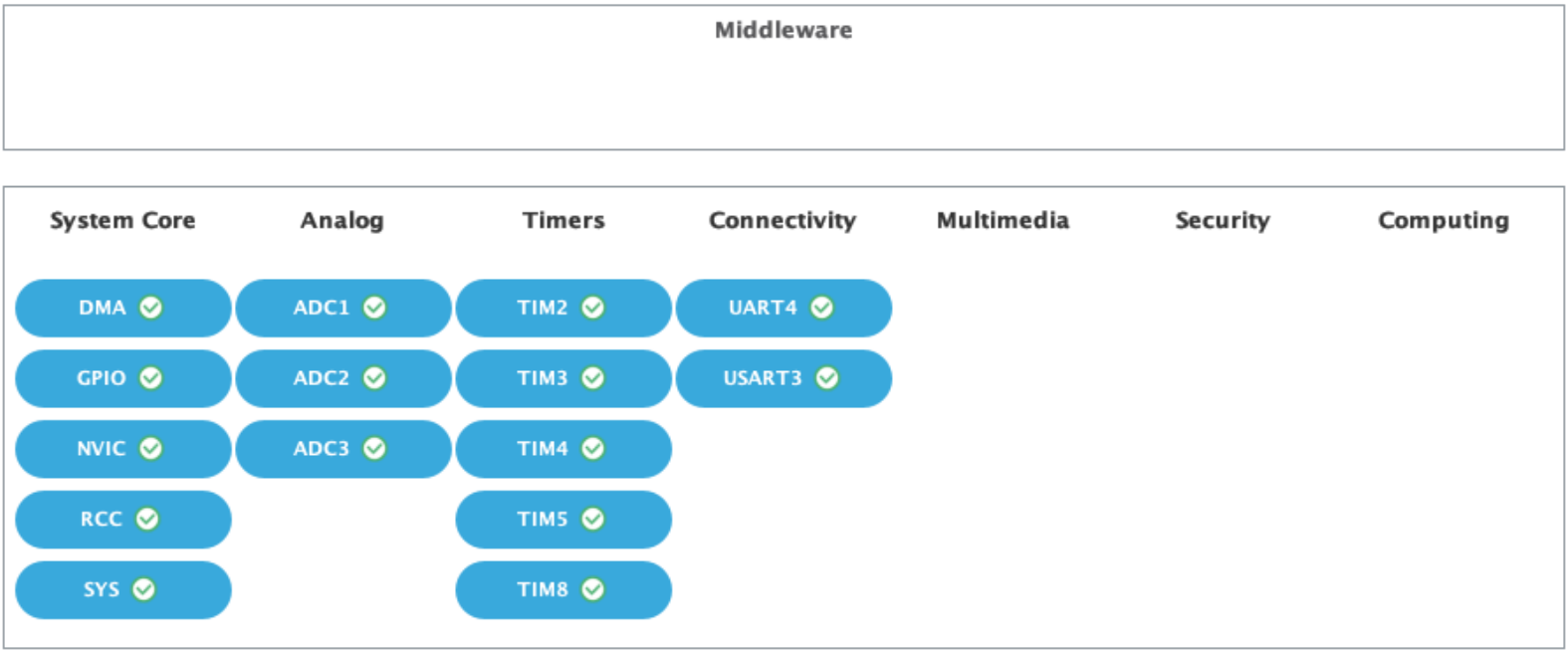
| Enabled interrupt Table | Select for init sequence ordering | Generate IRQ handler | Call HAL handler |
|---|---|---|---|
| Pre-fetch fault, memory access fault | false | true | false |
| Undefined instruction or illegal state | false | true | false |
| System service call via SWI instruction | false | true | false |
| Debug monitor | false | true | false |
| Pendable request for system service | false | true | false |
| System tick timer | false | true | true |
| DMA1 stream1 global interrupt | false | true | true |
| TIM4 global interrupt | false | true | true |
| USART3 global interrupt | false | true | true |
| TIM5 global interrupt | false | true | true |
| DMA2 stream0 global interrupt | false | true | true |
| DMA2 stream1 global interrupt | false | true | true |
| DMA2 stream2 global interrupt | false | true | true |

*** User modified value**

# 5. System Views

5.1. Category view

*5.1.1. Current*



# 6. Docs & Resources

| Type | Link |
|---|---|
| BSDL files | https://www.st.com/resource/en/bsdl_model/stm32f405-415_407-417_bsdl.zip |
| IBIS models | https://www.st.com/resource/en/ibis_model/stm32f405-415_407-417_ibis.zip |
| System View Description | https://www.st.com/resource/en/svd/stm32f4-svd.zip |
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