s_gate_pulses_MLI_3ph_1 (subcircuit)

Attributes

```
inputs: tri
outputs:
e_left_nodes:
e_right_nodes:
e_top_nodes:
e_bottom_nodes:
b_left_nodes:
b_right_nodes: A B C
b_top_nodes:
b_bottom_nodes:
parameters:
  a_sin: 1
  delt_min: 0.1u
  delt_nrml: 1u
  f_ac: 50
```

Description

s_gate_pulses_MLI_3ph_1 is an exntension of s_gate_pulses_MLI_1ph_1 for generating gate pulses for three-phase multi-level inverter circuits. Its input tri should be connected to a triangular waveform source. The input is compared with sinusoids with different phase angles, as shown in the figure. The parameters a_sin and f_ac specify the amplitude and frequency of the sinusoids. The parameters delt_min, delt_nrml are used for controlling the simulator time steps (see documentation for cmpr_2_2).

The gate pulse signals at the output are made available as three bus ports A, B, C.

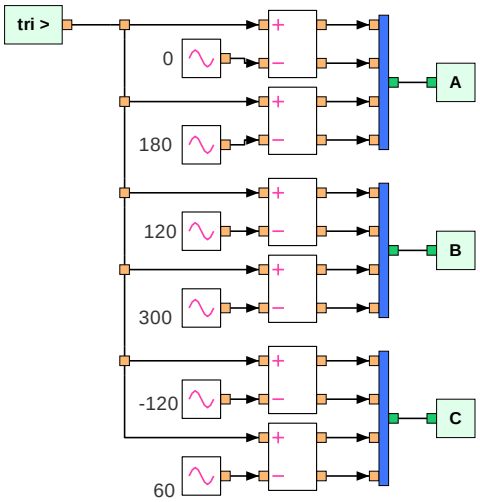

Figure 1: Schematic diagram of s_gate_pulses_MLI_3ph_1.