

# Parallel Programming on Embedded Multicore System ESP32

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WS2019/2020  
October 29, 2019

# Abstract

The following documentation will focus on the principles of parallel programming in general and the mathematical background. In addition to the different parallel programming architectures, the various models for their implementation are also discussed. Moreover, in this thesis the prerequisites for mathematical calculation models, which are suitable for Parallel Programming, are elaborated.

For a practical example, the ESP32 microcontroller was chosen, an embedded multicore system. After a brief introduction to the hardware itself, further details of the project structure and the development of the application will be presented. Therefore, a short example will be explained to focus on the basics of parallel programming.

Finally, the aim of the project and the documentation is an automatic benchmark setup and a webfrontend result overview for visualization purposes, which will be discussed in more detail in the conclusion.

## Declaration

I hereby certify that I have done the final thesis on my own, that I have completely and accurately stated all the aids I have used and identified everything individually, which was taken from the work of others unchanged or with modifications.

*The topic of the submitted work was jointly with Mr. / Mrs. (...) (Bachelor and Master Thesis No. (...)).*

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# Chapter 1

## Introduction

Multicore systems are becoming increasingly popular as part of digitization and Industry 4.0<sup>1</sup> (German/EU) [2] [or 1] - also known as smart manufacturing in the USA [see 29, p1] - and are playing an important role in data processing and process automation [see 33, p294] [or 28, p1]. On the other hand, in addition to efficiency in energy consumption, performance in terms of computation time [see 33, p294] is required in almost every application field of multicore systems.

In fact, multicore hardware is not only expecially for smart manufacturing. Nowadays in almost every smart application like smart phones<sup>2</sup>, wearables<sup>3</sup> or home automation we can find multicore embedded hardware platforms, which garantued high performance [see 4, p7], network connectivity, security and reliability [see 36, p5]. This field of application is also known as Internet of Things (IoT)<sup>4</sup>.

Especially for embedded systems mathematical models as well as numerical solutions, which can be executed both simply and parallel, are suitable. The question arises to what extent parallel execution of different sub-tasks to calculate a problem [see 32, p4] increases the desired cost factor in terms of energy consumption [see 13, chapter 3] and computational efficiency [see 32, p4 Figure 3].

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<sup>1</sup>add.: <https://www.epicor.com/en-ae/resource-center/articles/what-is-industry-4-0/>

<sup>2</sup>e.g. ARM based processors for mobile phones like <https://www.arm.com/solutions/mobile-computing/smartphones>

<sup>3</sup>add. information on ARM based solutions and the current trend in wearables: <https://www.arm.com/solutions/wearables>

<sup>4</sup>for additional information about Internet of Things, please see [20]

# Chapter 2

## Overview

### 2.1 Problem definition

Compared to single-core execution of tasks, multi-core embedded hardware platforms like the ESP32<sup>1</sup> provide the ability to develop advanced parallel computing software applications to reduce execution time and power consumption.

On the one hand, a major problem is choosing the right hardware platform to meet the cost and size factor, and moreover, whether a single-core or multi-core calculation is required. Therefore, context switching time, power consumption and total execution time must be included in the evaluation.

In order to develop an optimal solution, the hardware platform must be included in addition to the mathematical model of the problem itself. So in this case, suitable prerequisites and characteristics can be worked out in order to make an evaluation of "Parallel Computation Tasks on Embedded Multicore Systems" possible.

### 2.2 Objective of the documentation

The main goal of this documentation is to focus on the current parallel programming techniques, depending on the execution time in general and the required mathematical model. For this purpose, an application which can compute different sections of the Mandelbrot fractal [see 19, p11] will be developed to compare single core and multi-core calculations. Before the practical implementation, an investigation based on parallel architectures and programming models will be conducted.

The elaboration is divided into three different chapters: In the first chapter, the results of the general research are presented [see 3]. After that, the second chapter is pointing out the practical implementation of the developed application on the ESP32 [see 4]. In the end, the results including the webfrontend and the automatic benchmark setup [see 5] will be discussed.

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<sup>1</sup>add. information: <https://www.espressif.com/en/products/hardware/socs>

# Chapter 3

## Parallel Programming in General

### 3.1 Basic Concept

Amdahl's law [5]:

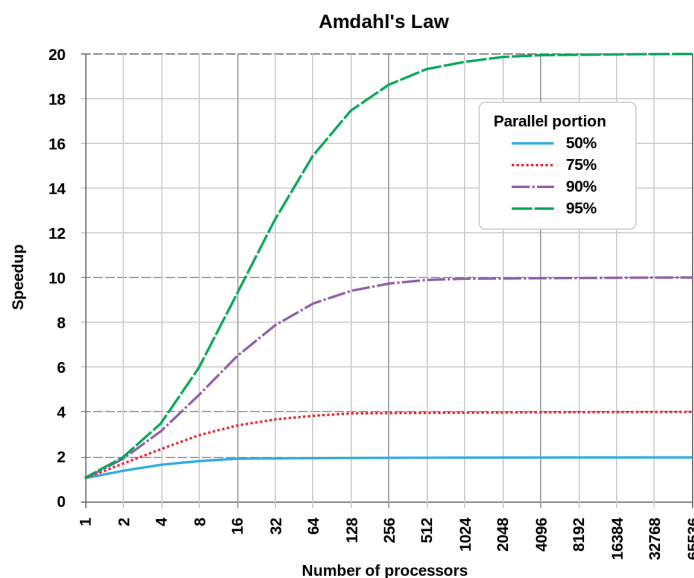


Figure 3.1: ...

- “the contention that the organization of a single computer has reached its limits and that truly significant advances can be made only by interconnection of a multiplicity of computers” [see 8, p80]; can be transferred on single and multi-core processors or even on multithreading, but in fact, like Amdahl claimed too, addressing hardware, and nowadays switching context time was not considered here! Valiant noted in 1990, “no substantial impediments to general-purpose parallel computation” exist [see 8, p85], though there are limits, as shown [see in Sec. 10.8, p85].

- “the fraction of the computational load... associated with data management housekeeping ... accounts for 40% of the executed instructions”, “this overhead appears to be sequential so that it is unlikely to be amenable to parallel processing techniques” [see 8, p80]; amount of overhead (data management and addressing based on hardware restrictions), which can not be parallelized and reduces the factor of speed increase after parallelization. According to Amdahl, this factor can be reduced, but not with “parallel processing techniques”, probably with more precisely and efficient hardware.
- a resisting “upper limit on speedup [exists] and therefore, apart from the sequential fraction (the so called non parallelizable overhead), the remaining computations are perfectly parallelizable” [see 8, p81]
- the law in general: Let  $t_1$  be the time taken by one processor solving a computational problem and  $t_p$  be the time taken by  $p$  processors solving the same problem. Finally let us denote the supposed inherently sequential fraction of instructions by  $f$ . Then, according to Amdahl,  $t_p = t_1 (f + (1-f)/p)$  and the speedup obtainable by  $p$  processors can be expressed as:

$$\frac{t_1}{t_p} = \frac{1}{f + (1-f)/p}$$



### 3.1.1 Principles of Parallel Computing

**Emphasises design:** Amdahl's law highlights the pitfalls of looking for sticking-plaster speed-ups in serial programs – design for concurrency [see 23, p4]

**Aim of concurrency and their effects** on program structure or implementation [see 23, p5]:

- Flexibility: Environments will be more heterogeneous.
- Efficiency: parallel for a speed-up purposes, more pitfalls (memory latency, thread overheads etc.)
- Simplicity: Parallel codes will be more complicated. All the more reason to strive for maintainable, understandable programs.

## **3.2 Definition of parallel mathematical computations**

...

## 3.3 Parallel Computer Architecture

...[see 30, p9]

...examples of parallelism [see 30, p11]

### 3.3.1 Flynn's Taxonomy of Parallel Architectures

...[see 11, p5]

...[see 30, p13]

...[see 10, p4]

...[see 5, p2]

### 3.3.2 Thread Level Parallism

...[see 30, p24]

## 3.4 Parallel Programming Models

Steps to evaluate a proper parallel design [see 23, p6]:

1. Finding Concurrency
2. Algorithm Structure
3. Supporting Structures
4. Implementation Mechanisms

### **3.4.1 Classification of Parallel Programming Models**

#### **3.4.1.1 Process Interaction**

...[see 11, p4]

#### **3.4.1.2 Problem decomposition**

...[see 30, p105 ff.]

# Chapter 4

## Project documentation

### 4.1 Concept development

...

## 4.2 Project structure

...

## **4.3 Simple mathematical computation examples for Parallel Programming**

...

## **4.4 Class diagramm**

...

### **4.4.1 C++ Backend benchmark**

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### **4.4.2 Vuejs Frontend**

...



## 4.5 Benchmark setup

...

# Chapter 5

## Conclusion

...

# Appendix A

## Additional documents

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