

SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA
B. Tech. (ECE/CSE/ME-I) Semester Examination (Minor-I) 2018-19

Entry No: **18 BE CO GG**

Total Number of Pages: [1]

Date: 7th Feb, 2019

Total Number of Questions: [4]

Course Name: Electronic Circuits & Simulation

Course Code: ECL1030

Time Allowed: 1.5 Hours

Max Marks: [20]

Instructions / NOTE

- i. Attempt All Questions.
- ii. Support your answer with diagrams / neat freehand sketches, wherever appropriate.
- iii. Assume any missing data to suit the derivation / answer.

Q1. (a) In practical Common-Emitter (CE) amplifier design, draw the ac-circuit with all components and differentiate it from the dc-circuit of this amplifier. [3] CO1

(b) Draw the 2-port equivalent circuit for the above CE amplifier [2] CO1

Q2. Draw the approximate h-model of an amplifier, with reasons for approximations. Compare the approximate h-model with *re* model. [5] CO1

Q3. The amplifier circuit in Fig. 1, uses a silicon transistor with $\beta=50$, $V_{BE}=0.7V$, $V_{CC}=24V$, $R_C=4.7K$. Find the values of the resistor R_E , R_1 , R_2 so that the Q-point is set at $V_{CE}=12V$, $I_C=1.5mA$. The stability factor, S must be set at ≤ 5.1 . [5] CO1

Q4. In the CE amplifier circuit shown in Fig. 2, draw the equivalent *re* model. Also, find R_{in} , R_{ac} , Voltage gain and power gain. [1+4] CO1

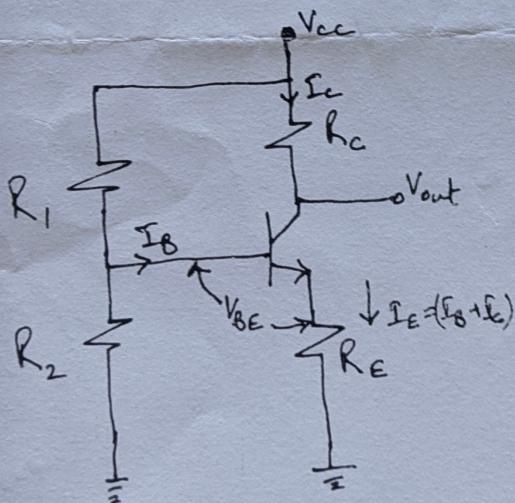


Fig. 1

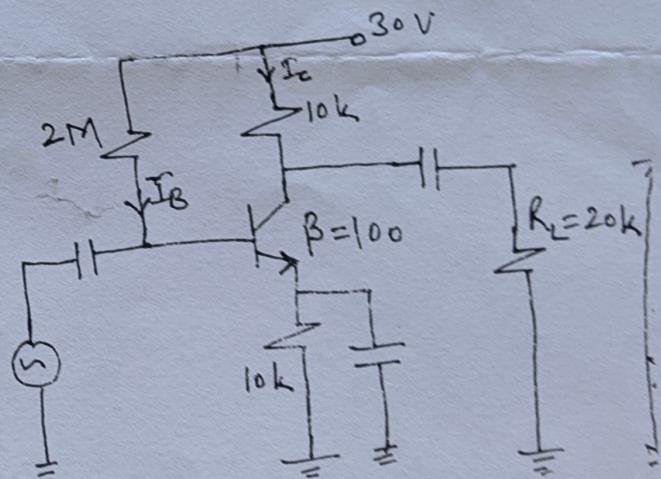


Fig. 2

Course Outcomes (CO):

1. BJT Circuit design, small signal and large signal analysis

SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA
B. Tech. (ECE-II) Semester Examination (Minor-II) 2018-19

Entry No:

Total Number of Pages: [1]

Date: 19th March, 2019

Total Number of Questions: [4]

Course Name: Electronic Circuits & Simulation

Course Code: ECL1030

Time Allowed: 1.5 Hours

Max Marks: [20]

Instructions / NOTE

- i. Attempt All Questions.
- ii. Support your answer with diagrams / neat freehand sketches, wherever appropriate.
- iii. Assume any missing data to suit the derivation / answer.

Q1. Compute the overall voltage gain for the two stage amplifier in Fig. 1. Express the answers in decibel. Assume $V_{BE}=0.7V$, β of both transistors is 100, $V_T=26mV$. [5] CO3

Q2. Calculate the input power, output power and efficiency of the amplifier circuit in Fig. 2 for an input of 17V (peak) and input current of 4.25 A (peak). [5] CO3

Q3. The voltage gain of an amplifier without feedback is 2500. If 40 dB of negative feedback is added: [5] CO4

- (a) what is the gain with feedback.
- (b) For obtaining the same output, how much must be the input increased? *100 times*

Q4. (a) Explain the concept of feedback in electronic circuits? Compare the merits and demerits of negative and positive feedback. [2.5] CO4
(b) Draw the circuits for common-emitter Class A and Class B amplifier and explain the difference between them [2.5] CO3

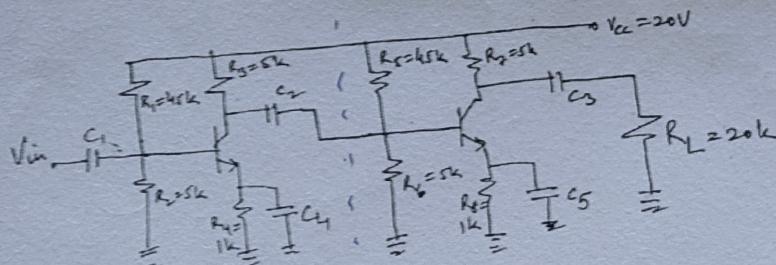


Fig. 1

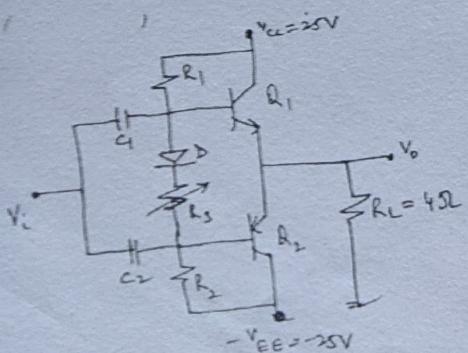


Fig. 2

SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA
B. Tech. (ECE II) Semester Examination (Major) 2018-19

Entry No:

Total Number of Pages: [2]

Date: 15th May, 2019

Total Number of Questions: [5]

Course Name: Electronic Circuits & Simulation

Course Code: ECL1030

Time Allowed: 3 Hours

Max Marks: [50]

Instructions / NOTE

- i. Attempt All Questions.
- ii. Support your answer with diagrams / neat freehand sketches, wherever appropriate.
- iii. Assume any missing data to suit the derivation / answer.

Q1. (a) In a common emitter amplifier circuit shown in Fig. 1, find R_{in} , R_{out} , voltage gain (A_v). Take $\beta = 100$. How will these values change if emitter bypass capacitor is removed. [5] CO1

[5] CO1

(a) Determine using hybrid- π model, the small signal voltage gain, input resistance, output resistance of the circuit shown in Fig. 2. Assume $\beta = 100$, $V_{BE} = 0.7$, $I_B = 9.5\mu A$, $r_o = 105K$.

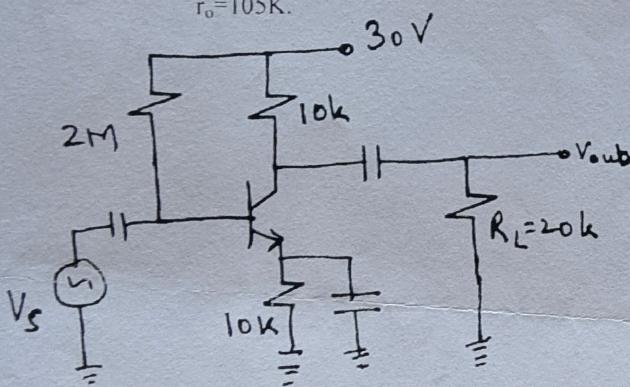


Fig. 1

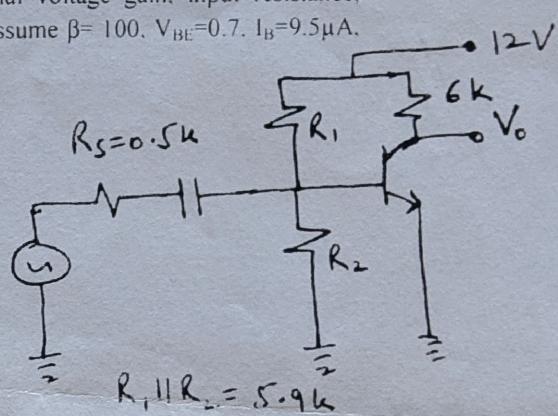


Fig. 2

Q2. (a) The common drain circuit given in Fig. 3 has $R_1 = 4M\Omega$, $R_2 = 2M\Omega$, $R_S = 2.5K$, $R_D = 25K$, $V_{DD} = 25V$, and $g_m = 2500\mu S$. Determine (i) Input and output impedance. (ii) Voltage gain. [5] CO2

(b) In the Common source amplifier in Fig. 4, drain resistance $R_D = 5K$, amplification factor $\mu = 50$, $r_d = 35K$. Evaluate the voltage gain A_v and output resistance R_O . [5] CO2

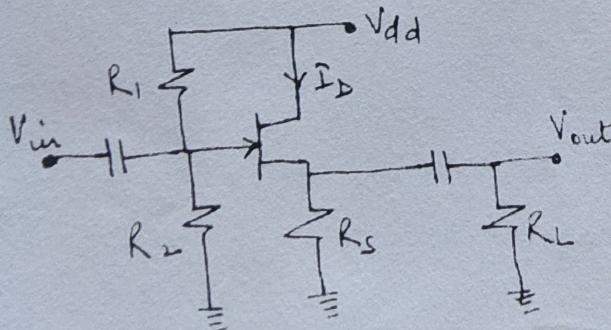


Fig. 3

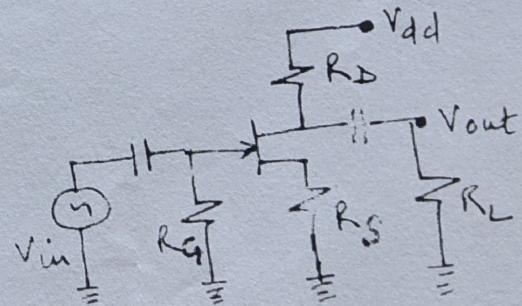


Fig. 4

Q3. (a) Describe cascoded amplifiers, and compare these with cascaded amplifiers. [5] CO3

(b) For the impedance coupled two stage amplifier shown in Fig. 5, compute the value of Voltage gain (A_v) at 4 KHz. Assume ideal BJT with $V_{BE} = 0$, $\beta_1 = \beta_2 = 100$, $V_T = 25mV$. [5] CO3

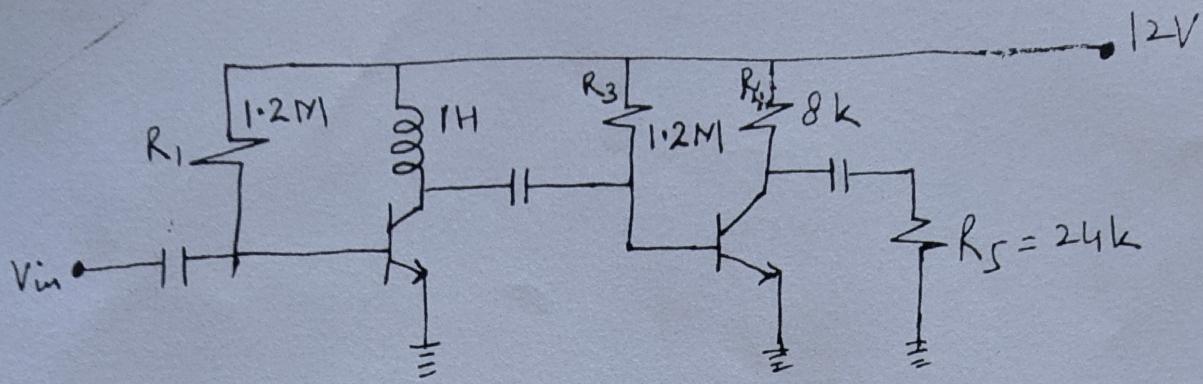


fig.5

- Q4. (a) The voltage gain of an amplifier without feedback is 3000. Calculate the voltage gain of the amplifier with negative feedback. The feedback factor β is 0.01. [5] CO4
(b) Describe a Darlington pair with a circuit diagram. Also mention the main characteristics and parameters of a Darlington pair. [5] CO5
- Q5. (a) Describe a current mirror with a neat circuit diagram. Also mention its limitations, and the method to improve it. [5] CO5
(b) Write notes on (i) linear power supplies and (ii) Digital Integrated Power supplies [5] CO5

Course Outcomes (CO):

1. BJT Circuit design, small signal and large signal analysis
2. FET circuit design, small signal and large signal analysis
3. Large signal amplifiers and multistage amplifiers
4. Frequency response of the amplifiers, feedback analysis
5. Useful analog integrated circuits