

SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA
School of Electronics and Communication Engineering
B. Tech. (CSE) Minor I Examination (Even Summer) 2018-19

Entry No: **18BCS064**

Date:

Course Title: **Digital Electronics**

Total Number of Pages: [01]

Total Number of Questions: [08]

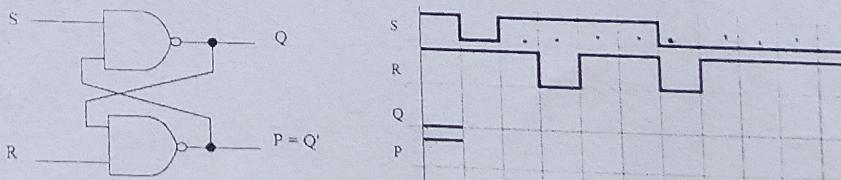
Course Code: **ECL 2070**

Max Marks: [20]

Time Allowed: 1.5 Hours

Instructions / NOTE

- Attempt All Questions.
- Support your answer with neat freehand sketches/diagrams, wherever appropriate.
- Assume any missing data to suit the case / derivation / answer.

Q. No.1.	i.	The value of radix r in expression $\sqrt{(224)_r} = (13)_r$ is a) 10 b) 8 c) 5 d) 6	[1 x 5]	CO1 CO1 CO1 CO1 CO1
	ii.	4-bit 2's complement representation of a decimal number is 1000. The number is: a) +8 b) 0 c) -7 d) -8		
	iii.	A new Binary Coded Pentary (BCP) number system is proposed in which every digit of a base-5 number is represented by its corresponding 3-bit binary code. For example, the base-5 number 24 will be represented by its BCP code 010100. In this number system, the BCP code 100010011001 corresponds to the following number in base-5 system: a) 423 b) 1324 c) 2201 d) 4231		
	iv.	The two numbers represented in signed 2's compliment form are $P = 11101101$ and $Q = 11100110$. If Q is subtracted from P , the value obtained in signed 2's compliment form is: a) 100000111 b) 00000111 c) 11111001 d) 111111001		
	v.	Hexadecimal Equivalent of $(5426.24)_8$ is		
Q. No.2.	Using Boolean Algebra Laws, prove following statements:			
	i.	$ABC + A\bar{B}\bar{C} + \bar{A}BC + \bar{A}\bar{B}C + ABC = BC + \bar{B}\bar{C} + A\bar{B}$	[2.5 x 2]	CO3 CO3
	ii.	$\bar{A}BD + BCD + ABC + \bar{A}\bar{B}D = B\bar{C}\bar{D} + AD + \bar{A}BC$		
Q. No.3.	i.	Convert the following POS expression into SOP: $Y = (A + B + C + \bar{D})(A + B + \bar{C} + D)(A + \bar{B} + C + \bar{D})(A + \bar{B} + \bar{C} + D)$ $(\bar{A} + \bar{B} + \bar{C} + D)(\bar{A} + B + C + \bar{D})(\bar{A} + B + \bar{C} + D)$	[2.5 x 2]	CO3 CO3
	ii.	Complete the timing diagram for the logic diagram shown below:		
				
Q. No.4.	Explain the application of Gray Code with a suitable example.			
			[5]	CO1

Course Outcomes:

- To acquire Knowledge of various number systems and codes from historic point of view.
- To understand the logic families in Digital circuits.
- To obtain the ability to analyze and design Digital circuits.
- To learn the Electrical Circuit interfacing considerations.

CO	Questions Mapping	Total Marks	Total Number of Students (to appear in Exam)
CO1	1 & 4	10	84
CO2		-	84
CO3	2 & 3	10	84
CO4		-	84

SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA
School of Electronics and Communication Engineering
B. Tech. (CSE) Minor II Examination (Even Summer) 2018-19

Entry No: **1 8 B C S O 6 4**

Date:

Course Title: Digital Electronics

Time Allowed: 1.5 Hours

Total Number of Pages: [01]

Total Number of Questions: [04]

Course Code: ECL 2070

Max Marks: [20]

Instructions / NOTE

- i. Attempt All Questions.
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- iii. Assume any missing data to suit the case / derivation / answer.

A logic family has threshold voltage of 2 volts, minimum guaranteed output high voltage $V_{OH} = 4$ volts, minimum accepted input high voltage $V_{IH} = 3$ volts, maximum guaranteed output low voltage $V_{OL} = 1$ volt, and maximum accepted input low voltage $V_{IL} = 1.5$ volts. Determine its Noise Margin

CO2

The inverter 74ALS04 has the following specifications:

i. $I_{OHi\max} = -0.4$ mA, $I_{OLi\max} = 8$ mA, $I_{IHi\max} = 20 \mu\text{A}$, $I_{ILi\max} = -0.1$ mA.

[1 x 3]

CO2

Determine the Fan Out of the above.

iii. Among the digital IC families, ECL, TTL and CMOS, which family has the least propagation delay?

CO2

A bulb in a staircase has two switches, one switch being at the ground floor and the other one at the first floor. The bulb can be turned ON and also can be turned OFF by any one of the switches irrespective of the state of the other switch. Implement this logic using only 2-input NOR gates only

[3 x 2] CO3

ii. Using 4:1 Multiplexer, implement 1 bit full adder.

Determine the reduced SOP for min terms using K map

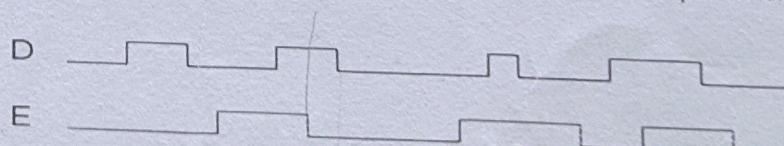
$$\sum m(0,2,4,7,8,10,12,16,18,20,23,24,25,26,27,28)$$

[3 x 2] CO3

ii. Design a BCD to single digit 7-Segment numeric display Decoder using NAND gates only.

Explain the working of D Latch and also draw the output Q for the input conditions given below:

Q. No.4.



[5] CO3

Course Outcomes:

- CO1. To acquire Knowledge of various number systems and codes from historic point of view.
- CO2. To understand the logic families in Digital circuits.
- CO3. To obtain the ability to analyze and design Digital circuits.
- CO4. To learn the Electrical Circuit interfacing considerations.

CO	Questions Mapping	Total Marks	Total Number of Students (to appear in Exam)
CO1	-	-	84
CO2	1	3	84
CO3	2, 3 & 4	17	84
CO4	-	-	84

SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA
School of Electronics and Communication Engineering
B. Tech. (CSE) Major Examination (Even Summer) 2018-19

Entry No: 1 8 B c S O 6 4

Total Number of Pages: [02]

Date:

Total Number of Questions: [07]

Course Title: Digital Electronics

Course Code: ECL 2070

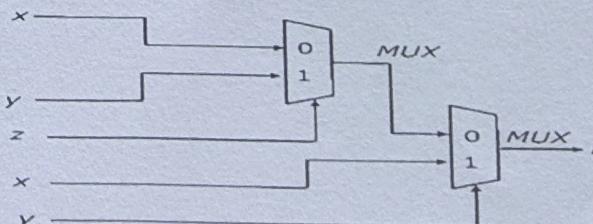
Time Allowed: ~~2~~ Hours

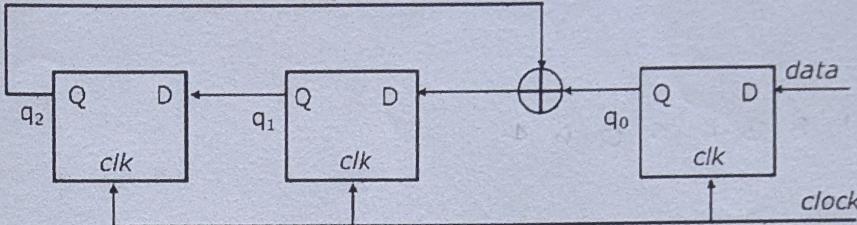
Max Marks: [50]

3

Instructions / NOTE

- Attempt All Questions.
- Support your answer with neat freehand sketches/diagrams, wherever appropriate.
- Assume any missing data to suit the case / derivation / answer.

Q. No.1.	i.	Which of the following option is correct regarding number conversion from a base to another base? a) If a number has k digits in hex, then k/4 digits (bits) can have in binary. b) If a number has k digits in decimal, then roughly k/2 digits can have in binary. c) If a number has k digits base a, then roughly $k * \log_a(b)$ digits can have in base b? d) None of the above	[1 x 5]	CO1 CO2 CO1 CO1 CO3
	ii.	The inverter 74ALS04 has the following specifications: $I_{O\text{Hmax}} = -0.4 \text{ mA}$, $I_{OL\text{max}} = 8 \text{ mA}$, $I_{IH\text{max}} = 20 \mu\text{A}$, $I_{IL\text{max}} = -0.1 \text{ mA}$. Determine the Fan Out of the above.		
	iii.	Let $m=(313)_4$ and $n=(322)_4$. Find the base 4 expansion of $m+n$.		
	iv.	What is the result of addition of 4-bit, two's complement, binary numbers 1101 and 0100?		
	v.	Consider the following Boolean function of four variables: $f(w,x,y,z) = \sum(1,3,4,6,9,11,12,14)$ The function is: a) independent of one variables. b) independent of two variables. c) independent of three variables. d) dependent on all the variables.		
Q. No.2.	i.	Let X denote the Exclusive OR (XOR) operation. Let '1' and '0' denote the binary constants. Consider the following Boolean expression for F over two variables P and Q : $F(P, Q) = ((1 X P) X (P X Q)) X ((P X Q) X (Q X 0))$ Determine the simplified expression for F in terms of P and Q .	[3]	CO3
	ii.	For the circuit shown in the figure right, determine the minimized Boolean expression for f	 [3]	CO3

Q. No.3.	i.	Consider the circuit in the diagram. The \oplus operator represents Ex-OR.	[3]	CO3
				
Q. No.4.	ii.	Initially o/p of all flip flops is zero. The following data: 100110000 is supplied to the "data" terminal in nine clock cycles. Determine the values of $q_2 q_1 q_0$ at 10 th clock pulse.	[3]	CO2
	i.	A 3 bit ripple counter uses J K flip flops. If the propagation delay of each flip flop is 50 nsec, determine the maximum clock frequency that can be used in the counter.	[3]	CO4
Q. No.5.	i.	Two resistor of 20k Ω and 50 k Ω are at room temperature (290K). For a bandwidth of 100kHz, calculate the thermal noise voltage generated if two resistors are in series and if two resistor are in parallel	[3]	CO4
	ii.	A 5-bit D/A converter produces $V_{OUT} = 0.2$ V for a digital input of 0001. Find the value of V_{OUT} for an input of 1111.	[3]	CO4
Q. No.6.	i.	Using Quine-McCluskey method, minimize the following logic	[5]	CO4
		$F(A, B, C, D) = \sum m(0,3,5,6,7,10,12,13) + d(2,9,15)$		
Q. No.7.	ii.	Design a code converter circuit for BCD-to-Excess-3 code using PROM	[4]	CO3
	i.	Design synchronous counter to count the sequence 0-1-2-3-4-5-0. The counter should return to reset state if any unwanted state is encountered.	[5]	CO3
	ii.	Explain the working of binary weighted resistor Digital to Analog Converter (DAC). What are its limitations and how are those limitations overcome in R/2R ladder N/W DAC?	[4]	CO4
	i.	What are the different sources of noise in Digital circuits? Explain any one in detail.	[4]	CO4
	ii.	Explain the working of 2 input TTL NAND gate.	[5]	CO2

Course Outcomes:

- CO1. To acquire Knowledge of various number systems and codes from historic point of view.
 CO2. To understand the logic families in Digital circuits.
 CO3. To obtain the ability to analyze and design Digital circuits.
 CO4. To learn the Electrical Circuit interfacing considerations.

CO	Questions Mapping	Total Marks	Total Number of Students (to appear in Exam)
CO1	1(i), 1(iii), 1(iv)	3	84
CO2	1(ii), 3(ii), 7(ii)	9	84
CO3	1(v), 2, 3(i), 5(ii), 6(i)	19	84
CO4	4, 5(i), 6(ii), 7(i)	19	84

SRI MATA VAISHNO DEVI UNIVERSITY, KATRA
School of Electronics & Communication Engineering
B. Tech. ECE 3rd Semester Minor Examination (Odd Summer) 2019-20

Entry No: **18SEC066**

Total Number of Pages: [02]

Date:

Total Number of Questions: [07]

Course Title: Digital Electronics

Course Code: ECL 2070

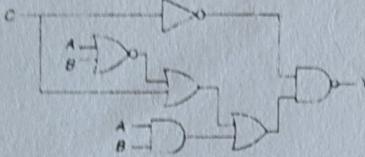
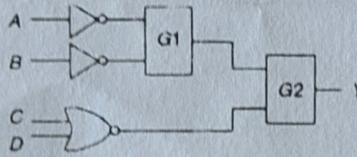
Time Allowed: 1.5 Hours

Max Marks: [30]

Instructions / NOTE

- iv. Attempt All Questions.
- v. Support your answer with neat freehand sketches/diagrams, wherever appropriate.
- vi. Assume an appropriate data / information, wherever necessary / missing.

Section - A

Q1.	(a) In the circuit shown in Figure below find the expression for output Y :  b) In the circuit shown below which gates are to be used in place of G1 and G2 to obtain the output $Y = AB + \overline{C} \overline{D}$.  c) The number of bytes required to represent the decimal number 1856357 in packed BCD ((Binary Coded Decimal)) form is _____. d) P is a 16-bit signed integer. The 2's complement representation of P is (F87B) ₁₆ . The 2's complement representation of 8*P is _____. e) i) For an n – variable Boolean function, the maximum number of prime Implicants is _____. ii) 2's compliment representation of a 16-bit number (one sign bit and 15 magnitude bits) is FFFF. Its magnitude in decimal representation is _____.	[2*5] =Marks 10	CO1, CO2
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Section - B

Q2.	In a certain application, four inputs A, B, C, D (both true and complement forms available) are fed to logic circuit, producing an output F which operates a relay. The relay turns on when $F(ABCD) = 1$ for the following states of the inputs (ABCD): '0000', '0010', '0101', '0110', '1101' and '1110'. States '1000' and '1001' do not occur, and for the remaining states, the relay is off. Minimize F with the help of a Karnaugh map and realize it using a minimum number of 3 input NAND gates are required to realize this function.	Marks 3	CO2
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	number of 3 input NAND gates are required to realize this function <i>Minimum no. of gates</i>		
Q3.	The circuit shown in figure is which type of converter _____	Marks 3	CO2
Q4.	If the input to the digital circuit (in the figure) consisting of a cascade of 20 XOR gates is X , then the output Y is equal to _____	Marks 3	CO1
Q5.	Convert the following number to Hexadecimal, Gray Code and Excess 3 Code a) 127 b) 256	Marks 3	CO2
Q6.	Solve the following using k map a) $y = \Sigma(0,1,3,5,9,12) + \Sigma d(2,4,6,7)$ b) $f(wxyz) = \Sigma(3,5,6,7) + \Sigma d(10,11,12,13,14,15)$	Marks 2,2 = 4	CO3
Q7.	Design a 1-bit Full Adder and implement it using NAND Gates only.	Marks 3, 1 = 4 Marks	CO3

Course Outcomes

1. To provide the skills to efficiently acquire knowledge on digital electronic circuit analysis and design.
2. To acquire Knowledge of various number systems and codes from historic point of view and to understand the logic families in digital circuits.
3. To obtain the ability to analyze various aspects of combinational circuit design.
4. To obtain the ability to analyze various aspects of sequential circuit design.
5. To learn the design procedure for Sequential Circuits and data converters.

SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA
School of Electronics & Communication Engineering
B. Tech. 3rd Sem ECE Minor -I (Odd/Even/Summer) 2019-20

Entry No: **1 8 B E C O 6 6** Total Number of Pages: [02]

Date: **11th December 2019** Total Number of Questions: [08]

Course Title: **Digital Electronics**

Course Code: **ECL 2070**

Time Allowed: 3 Hours

Max Marks: [50]

Instructions / NOTE

- i. Attempt All Questions.
- ii. Support your answers with neat freehand sketches/diagrams, wherever appropriate.
- iii. Assume an appropriate data / information, wherever necessary / missing.

Q1.	a) Convert the $(153.7)_{10}$ to Binary, BCD and hexadecimal format?	CO1, CO2, CO3 CO4 CO5	Marks 1 *15 = 15
	b) Excess 3 subtraction of $(23-13)_{10}$.		
	c) Logic Family with lowest power dissipation _____, lowest delay _____.		
	d) Expand TTL (term used in Logic Families) _____, ECL _____.		
	e) Implement 3:8 decoder using 2:4 decoder.		
	f) Explain the functioning of Clear, Reset and Preset pin used in ICs.		
	g) How active high is different from Active Low in digital Logic based IC's ?		
	h) _____ Latch is also called transparent latch.		
	i) Total delay of a digital system is function of _____.		
	j) Give one Advantage of 2's complement over 1's complement in terms of bit utilization.		
	k) Give XOR implementation using NOR gate. 5		
	l) _____ is used in Cache memory of the processor.		
	m) Expand the terms for memory EEPROM, EPROM, SRAM and DRAM.		
	n) R-2R type DAC is better than weighted resistor type DAC because of _____.		
	o) The fastest ADC amongst all types of ADC's is _____.		
Q2.	Design a combinational circuit of full subtractor and involve all the steps write from designing to K-map and implementation using logic gates.	CO 1, CO 3	Marks 5
Q3.	Describe the working of three input TTL NAND gate. Following points need to be included in your explanation Circuit diagram, atleast 3 cases for proper explanation.	Marks 5	CO 2
Q4.	What is the significance of race around condition in JK flip flop? What are the possible methods to eliminate it? Description of the methods is expected with clock diagram and other related details.	Marks 5	CO 4
Q5.	Design 4 bit asynchronous counter for up counting sequence. How can the counter be modified to count the truncated sequence say a decade counter?	Marks 5	CO 4

Q6.	How Memory is important in present technology revolution? Give the various classifications of the memory. Discuss in detail the memory organization for particular cell that includes read and write operation.	Marks 5	CO 4
Q7.	Discuss the working of Counter type ADC. What are the problems with counter type ADC and how they can be improved?	Marks 5	CO 5
Q8.	Design a 3 bit synchronous up counter. Illustrate various steps in the design process that includes truth table, State Table, Excitation table and implementation using the selected Flip Flop.	Marks 5	CO 5

Course Outcomes

CO1. To provide the skills to efficiently acquire knowledge on digital electronic circuit analysis and design.

CO2. To acquire Knowledge of various number systems and codes from historic point of view and to understand the logic families in digital circuits.

CO3. To obtain the ability to analyze various aspects of combinational circuit design.

CO4. To obtain the ability to analyze various aspects of sequential circuit design.

CO5. To learn the design procedure for Sequential Circuits and data converters.

CO	Questions Mapping	Total Marks	Total Number of Students (to be appeared in Exam)
CO1	1a,b,c , 2	5	77
CO2	3 d,e,f,g	8	77
CO3	2 ,1 (h),i	6	77
CO4	4,5,6, j,k	17	77
CO5	1(l),(m),(n),(o) , 7, 8	14	77

SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA
School of Electronics & Communication Engineering
B. Tech. EE Minor -I (Odd/Even/Summer) 2019-20

Entry No: **1 8 B E E 0 2 1**

Total Number of Pages: **[02]**

Date:

Total Number of Questions: **[05]**

Course Title: **Digital Electronics**

Course Code: **ECL 2070**

Time Allowed: **1.5 Hours**

Max Marks: **[30]**

Instructions / NOTE

- i. Attempt All Questions.
- ii. Support your answer with neat freehand sketches/diagrams, wherever appropriate.
- iii. Assume an appropriate data / information, wherever necessary / missing.

Section - A

- Q1** ✓ a) What is meant by the Phrase Digital Electronics and what is the significance of word Digital in this phrase? [02]
 b) How Digital Electronics differs from Analog Electronics? [01]
 c) What are the key electronic components used in digital electronics and what kind of biasing is required for these components? [02]
 d) Draw a simple 2-input OR gate using Diodes and Resistors. [01]
- Q2.** a) What is the advantage of Two's complement over One's complement and signed magnitude representation of the binary numbers? Explain with example [01]
 b) ✓ Perform following operations [01]
 - i. Addition of $(01101)_2 + (01110)_2$. [01]
 - ii. Convert the binary number $(11)_2$ into decimal number if only 2 bit locations are available. [01]
 - iii. Subtract using 2's complement method $(10011)_2 - (11100)_2$ [01]
 - iv. Decimal value of the octal fraction $(0.325)_8$. [01]
 - v. Add the following numbers $(DF)_{16} + (AC)_{16}$. [01]

Section - B

- Q3.** ✓ a) List 4-bit GRAY code? Also explain how it is different from the regular binary representation of a number. [02]
 b) Simplify the Boolean Expression

$$\overline{A} \overline{B} C + A \overline{B} \overline{C} + \overline{A} B C + A \overline{B} C$$

 c) Simplify the Boolean Expression [02]

$$(A+B)\overline{[A(\overline{B} + \overline{C})]} + \overline{A} \overline{B} + \overline{A} \overline{C}$$
- Q4.** ✓ Design a combinational circuit for Full Adder using K-Map technique. [06]
- Q5.** a) Minimize using K-map technique.
 $F(A,B,C,D) = \sum m(0,1,2,5,7,8,9,10,11,13,15)$ [04]
 b) Also draw the truth table for function above [02]

SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA
School of Electronics & Communication Engineering
B. Tech. EE Minor -I (Odd/Even/Summer) 2019-20

Course Outcomes

1. To provide the skills to efficiently acquire knowledge on digital electronic circuit analysis and design.
2. To acquire knowledge of various number systems and codes from historic point of view and to understand the logic families in digital circuits.
3. To obtain the ability to analyze various aspects of combinational circuit design.
4. To obtain the ability to analyze various aspects of sequential circuit design.
5. To learn the design procedure for Sequential Circuits and data converters.

CO	Questions Mapping	Total Marks	Total Number of Students (to be appeared in Exam)
CO1	1	6	35
CO2	2, 3(a), 5	14	35
CO3	3(b) 3(c), 4	10	35

SHRI MATA VAISHNO DEVI UNIVERSITY, ROURKELA
School of Electronics & Communication Engineering
B. Tech. 3rd Sem EE Major (Odd Semester) 2019-20

Entry No: 18BEE021
Date: 11th December 2019
Course Title: Digital Electronics

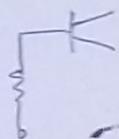
Total Number of Pages: [02]
Total Number of Questions: [08]
Course Code: ECL 2070

Time Allowed: 3 Hours

Instructions / NOTE

Max Marks: [50]

- i. Attempt All Questions.
- ii. Support your answer with neat freehand sketches/diagrams, wherever appropriate.
- iii. Assume an appropriate data / information, wherever necessary / missing.



(Q1) Q1.	i. Convert the $(153)_{10}$ to Binary, BCD and hexadecimal format. ii. Hexadecimal subtraction of $(23-13)_{10}$. iii. Logic Family with lowest power dissipation _____, lowest delay _____. iv. Expand HTL (term used in Logic Families) _____, ECL _____. v. Implement 3:8 decoder using 2:4 decoder. vi. Explain the functioning of Clear, Reset and Preset pin used in ICs. vii. How active high is different from Active Low in digital Logic based IC's? viii. Give one Advantage of 2's complement over 1's complement in terms of bit utilization. ix. Give XOR implementation using NOR gate. x. _____ is used in Cache memory of the processor. xi. Expand the terms for memory EEPROM, EPROM, SRAM and DRAM. xii. Why a 4 variable K-Map use 00, 01, 11 and 10 sequence instead of an ordered 00, 01, 10 and 11 sequence? xiii. A two-bit binary number is given as $10_{(2)}$. What is the corresponding decimal number? xiv. Convert $168f_{(16)}$ to octal. xv. Convert $25_{(4)}$ into decimal.	15	CO1 CO2 CO3 CO4 CO5
	Q2. Design a combinational circuit of full subtractor and involve all the steps write from designing to K-map and implementation using logic gates.	5	CO 1 CO 3
	Q3. Describe the working of three input OR gate and AND gate. Following points need to be included in your explanation circuit diagram, at least 2 cases for proper explanation.	5	CO 2
	Q4. What is the significance of race around condition in JK flip flop? What are the possible methods to eliminate it? Description of the methods is expected with clock diagram and other related details.	5	CO 4
	Q5. Design a ring counter using Flip-Flops.	5	CO 4
	Q6. Explain the working of a 4 input demultiplexer with help of circuit diagram and corresponding truth table. How the demultiplexer could be used as a decoder?	5	CO 4
	Q7. Design a binary to BCD encoder. Illustrate various steps in the design process that includes truth table, K-Map and implementation using the NAND Gates	10	CO 5

SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA
School of Electronics & Communication Engineering
B. Tech. 3rd Sem EE Major (Odd Semester) 2019-20

Course Outcomes

- CO1. To provide the skills to efficiently acquire knowledge on digital electronic circuit analysis and design.
- CO2. To acquire Knowledge of various number systems and codes from historic point of view and to understand the logic families in digital circuits.
- CO3. To obtain the ability to analyze various aspects of combinational circuit design.
- CO4. To obtain the ability to analyze various aspects of sequential circuit design.
- CO5. To learn the design procedure for Sequential Circuits and data converters.

CO	Questions Mapping	Total Marks	Total Number of Students (to be appeared in Exam)
CO1	1a,b,c, 2	5	35
CO2	3 d,e,f,g	8	35
CO3	2 ,1 (h),i	6	35
CO4	4,5,6, j,k	17	35
CO5	1(l),(m),(n),(o) , 7	14	35