

SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA

Entry No:

17BCS045

Minor-I (Summer Semester) - 2017-18

Total number of pages: [02]

Total number of questions: 04

B.Tech. || CSE Sem III & V

Microprocessors and Interfacing [ECL 3061]

Time allowed: 1.5 Hr

Max Marks: 20

Important Instructions:

- All questions are compulsory
- Assume any missing data

High during 1st clock cycle

Data & address bus demultiplex

Q. 1. (a) Describe the function of following pins in 8085?

- (a) SID (b) ALE (c) RESET IN

reset mpu to itself.

[3+3]

(b) Explain the following instructions.

- (ii) SHLD (iii) SUB M (iv) CMA

See,

300

72751

Q. 2. (a) How many chip of 512×8 bit is required to assemble $10K \times 32$ bit memory? How many no of address and data lines are there in the newly designed memory.

(b) Explain working of the following parts of 8085 microprocessor -

- (i) Stack pointer (ii) Flag register

- (iii) Temporary registers

1

Q. 3. (a) Specify the content of register A, B, C and flags after execution of the following program by 8085 microprocessor. Also calculate the time required to complete the execution of the program.

[2+1]

LXI B, 0506 H

06 06
A 188H

59 X 0.38

MVI A, 88 H

*1000 1000
1000 1000
1000 1000*

LOOP1: ORA A

*0000 0100
1000 1000
1000 1100*

*14
11*

RLC

0001 0001

JNC LOOP1

8CH

ADD B

STAX B

HLT

(b) Specify the content of Accumulator after the execution of the program. How many times loop 1 will be executed during the program?

[3]

LXI D, 0030 H

00 30

BC

XRA A

[0030] son.

Acc to zero

LOOP1: ADD D H

A - 8CH

LOOP2: DCR B

B - 05

JNZ LOOP1

C - 06

DCR C

JNZ LOOP2

30K add

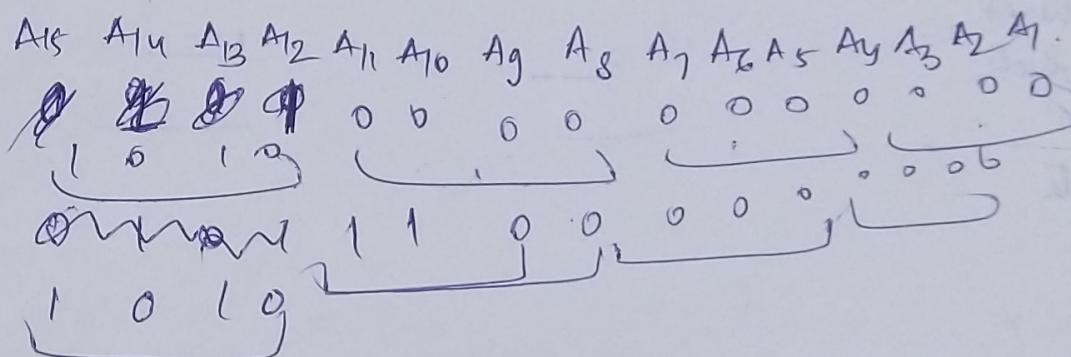
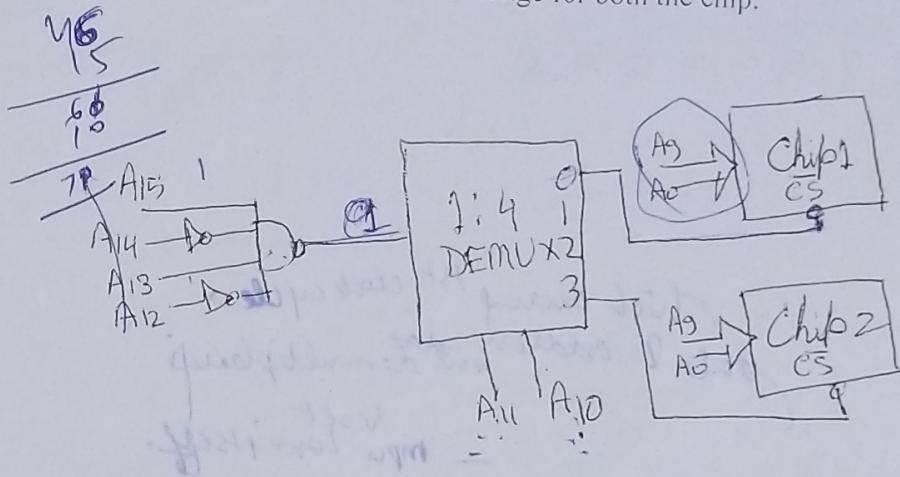
HLT

30K PF

30K add

Q4.

Two IC chips are connected with the microprocessor as per the following arrangement. Find the address range for both the chip. [3]



Now

AC @

A3 PP
A_{C,ff}

1010 00 1111 111111

1010 1100 1111 1111

1008	30277
1000	-4
20	-0
30	-0

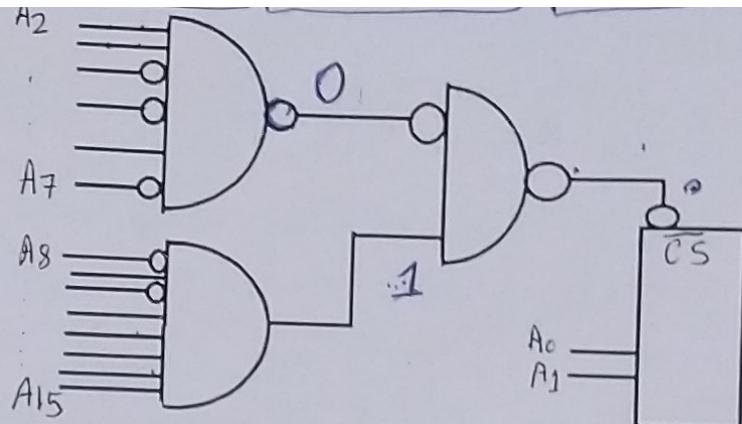


Fig. 1

11
11 10
11 11 11
0

PART-B

- (a) (i) In 8086 the overflow flag is set when [1]
a) the sum is more than 16 bits. b) subtraction c) carry and sign flags are set.
d) signed numbers go out of their range after an arithmetic operation.
- (ii) If CS register contains 23BCH and IP register contains BC23H then physical address will be $23BC0 + BC23$
- (b) Explain the addressing modes of 8086. [3]
- (c) What is memory segmentation? Why it is needed for 8086? What is the purpose of Queue in 8086? [3]
CS, DS *Increase Execution speed*
- (a) Justify the name of 8237 peripheral as DMA controller. [1]
- (b) How many registers are there in DMA controller? How to select each of them? [1]
- (c) Explain the master mode operation of DMA controller. [3]
Chip select
- (d) Explain the operation of 8255 in Mode 1 when the port set as output port. [2]
4 channels

SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA

Minor-II (Odd Semester) – 2018-19

Entry No:

17 BCS 045

Total number of pages:[02]

Total number of questions: [05]

B.Tech. || CSE Sem III & V

Microprocessors and Interfacing [ECL 3061]

Time allowed: 3 Hr

Max Marks: 50

Important Instructions:

- Attempt all questions
- Assume any missing data

Q1. (i) Show the status of the flag registers Z, CY, AC and P, after the execution of [1×10
following program. =10]
MOV A, 9Ch
ADI 64H

(ii) 8237 IC is worked as _____ and 8255 IC is worked as _____

(iii) Microprocessor pins that are used to request and acknowledge a DMA transfer are _____ and _____.

(iv) The maximum memory that can be supported by 8085 MPU is _____ and by 8086 MPU is _____.

(v) Frequency of operation for 8085 microprocessor is _____ and for 8086 microprocessor, it is _____.

(vi) Explain the operational difference between following pairs of instructions
(i) SPHL and XTHL (ii) XRA A and SUB A

(vii) Explain the difference between MOVSB AND MOVSW with an illustrative example?

(viii) Suppose that DS=1100H, BX=0200H and SI=0500H. Then the address accessed by MOV CH, [BX+SI] is _____.

(ix) Design a control word to configure port A and port B as input port and port C as output port when 8255 is connected as I/O mapped I/O mode.

(x) List all the control signals available in 8255 for its mode operation execution.

Q2. (a) Draw the timing diagram of SHLD instruction (Assume necessary Data)

[4+3+
3=10]

(b) Find the output of the following program. Also find the time required to execute the program.

MVI A, 07H
ADI 01H
RAL
JPE SKIP
SBI 01H
STA 2345H
HLT

SKIP: STA 2345H
HLT

(c) Write a program to convert a 8-bit Binary number to its equivalent BCD Number.

Q3. (a) Explain the following instructions with examples:
(i) NEG (ii) SAR (iii) LOOPNZ (iv) AAA [4+4=2=10]

(b) Explain the working of following pins in 8086:

(i) LOCK (ii) BHE (iii) TEST

(iv) RQ/GT₁

(iv) RQ/GT₀ and

(c) Briefly discuss about the flag registers available in 8086 microprocessor.

Q4. (a) What do you mean by masking and Interrupting? List out the Interrupt lines available in the 8086 microprocessor and briefly explain their operation. [4+4=2=10]

(b) What is the difference between I/O mapped I/O and memory mapped I/O? Also discuss the different options available in a microprocessor for I/O mapping.

(c) Explain the concept of multiprocessor operation in 8086 microprocessor?

Q5. (a) Write an 8085 assembly language program to exchange 10 bytes of data stored in memory location x with 10 bytes of data stored from memory location y. [5+5=10]

(b) Write a program using 8086 to search 35H from a string of 10 bytes data. If 35H found in the string, then store FFH at 2000H:3000H otherwise store 00H.

SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA
School of Electronics & Communication Engineering
B. Tech. (CSE), Minor Examination (Odd) 2019-20

Entry No:

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Total Number of Pages: [02]

Date: 01/10/2019

Total Number of Questions: [07]

Course Title: Microprocessor & Interfacing

Course Code: ECE 3061

Time Allowed: 1.30 Hours

Max Marks: [30]

Instructions / NOTE

- i. Attempt All Questions.
- ii. Support your answer with neat freehand sketches/diagrams, wherever appropriate.
- iii. Assume any missing data to suit the case / derivation / answer.
- iv. Use of IS Code (IS 456: 2000) is permissible in examination.

Section - A

Q1. Answer the following:

07X01= [07]

- A. The control bus and memories share a bidirectional bus in a typical microprocessor system.
A. True, B. False
- B. Address line for TRAP is?
A. 0023H, B. 0024H, C. 0033H, D. 0099H
- C. Which of the following represents the fastest data transmission speed?
A. Gbps, B. Kbps, C. Bps, D. Bandwidth
- D. The contents of the PC, when the microprocessor is reading from 2FFFH memory location, will be
A. 2FFE^H, B. 2FFF^H, C. 3000H, D. 3001H
- E. Which stack is used in 8085?
A. FIFO, B. LIFO, C. FILO, D. FCFS
- F. What is the clock frequency of 8085?
- G. What is the difference between a mnemonic code and machine code?
A. There is no difference.
B. Machine codes are in binary, mnemonic codes are in shorthand English.
C. Machine codes are in shorthand English, mnemonic codes are in binary.
D. None of these

Q2. Answer the following:

4.0X1.5= [06]

- A. Define the machine cycle and T-state.
- B. What is chip?
- C. Microcontroller versus microprocessor.
- D. Explain control & status signal in 8085.

Section - B

- Q3. What are the types of buses in 8085? Explain it. [02]
- Q4. Briefly explain the internal architecture of 8085 microprocessor with its net schematic diagram. [06]
- Q5. Explain various addressing modes of 8085. [03]
- Q6. Do a comparative study of the historical development of various μ P (year wise). [04]
- Q7. Consider the following instructions of 8085 μ P:
1. MOV M, A 2. ADC 3. MVI A, FF 4. CMP M
Which of these cause change in the status of flags?
a. 1 & 2, b. 1, 2, & 3 c. 3 & 4 d 2 & 4

Course Outcomes

1. To be able to understand about microprocessor based automated systems.
2. To understand the basic knowledge about 8085 microprocessor.
3. To be able to perform the Assembly Language programming of 8085 microprocessor.

SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA
School of Electronics & Communication Engineering
B. Tech (CSE), Major Examination (Odd) 2019-20

Entry No:

Total Number of Pages: [02]

Total Number of Questions: [08]

Course Title: **Microprocessor & Interfacing**
Course Code: **ECE 3061**

Time Allowed: 3.00 Hours

Max Marks: [50]

Instructions / NOTE

- i. Attempt All Questions.
- ii. Support your answer with neat freehand sketches/diagrams, wherever appropriate.
- iii. Assume any missing data to suit the case / derivation / answer.
- iv. Use of IS Code (IS 456: 2000) is permissible in examination.

Section - A

Q. 1. Answer the following:

01X10= [10]

1. INTR is a vectored or non-vectored interrupt?
2. How many numbers of T-states are needed for INX instruction?
3. The 8086 is a _____ bit processor having _____ address lines.
4. In context of 8086, NMI stands for?
5. What are the operating clock frequencies of 8086 microprocessor?
6. The term PSW Program Status word refers
 - A. Accumulator & Flag register.
 - B. H and L register.
 - C. Accumulator & Instruction register.
 - D. B and C register.
7. TRAP iswhereas RST 7.5, RST 6.5, RST 5.5 are....
 - A. Maskable, Non-maskable
 - B. Maskable, Maskable
 - C. Non-maskable, Non-maskable
 - D. Non-maskable, Maskable
8. Which of the following statements for Intel 8085 is correct?
 - A. Program Counter (PC) specifies the address of the instruction last executed.
 - B. PC specifies the address of the instruction being executed.
 - C. PC specifies the address of the instruction to be executed.
 - D. PC specifies the number of instructions executed so far.
9. The device address of I/O mapped I/O scheme is _____ bit?
10. What is the specified memory location of vectored interrupt RST 4.5?

Section - B

- Q. 2. Discuss the function of each and every pin of the 8085 processor. [5]
- Q. 3. Briefly explain the internal architecture of 8086 microprocessor with its net schematic diagram. [5]
- Q. 4. Classify 8085 instructions in various group. Give examples of instructions for each group. Also, explain various addressing modes of the 8085 processor. [4]

- Q. 5. Explain what operation is performed when the following instructions are executed: [03]
DAD r_p, DAA, CMP r, CMP M, RAL, SHLD, CMA, PUSH r_p & POP r_p
- Q. 6. Do the comparative study between Memory mapped I/O & I/O mapped I/O [05]
Interfacing scheme. Differentiate between 8085 & 8086.
- Q. 7. Write the assembly language program of the following: 02X08 = [16]
- Find the 2's complement of the number stored at memory location 4200H and store the complemented number at memory location 4300H.
 - Calculate the sum of series of even numbers from the given list of numbers. The length of the list is in memory location 2200H and the series begins from memory location 2201H. Result will store at memory location 2210H.
 - Write a program to perform the division of two 8 bits number using 8085.
 - Write a program to add 2-BCD numbers where starting address is 2000 and the numbers is stored at 2500 and 2501 memory addresses and store sum into 2502 and carry into 2503 memory address.
 - Find the square of the given numbers from memory location 6100H and store the result from memory location 7000H.
 - Write a program to arrange an array of data in ascending order.
 - How many times instruction NOP will be executed in a given 8085 assembly language program:
MVI A, 10H
MVI B, 10H
BACK: NOP
ADD B
RLC
JNC BACK
HLT
- In an 8085 the SP is 2010 and that of DE register pair is 1234H before the following code is executed:
- LXI H, 0000H
PUSH H
PUSH H
POP B
DAD SP
XCHG
- What is the content of DE register after execution of the above program?

- Q. 8. Draw and explain the timing diagram for opcode fetch operation. [2]

Course Outcomes

- To be able to understand about microprocessor based automated systems.
- To understand the basic knowledge about 8085 microprocessor.
- To be able to perform the Assembly Language programming of 8085 microprocessor.
- To understand the memory interfacing concept for microprocessors.
- To have knowledge about various peripheral devices used for special applications.
- To understand the basic knowledge about 8086 microprocessor.
- To be able to perform the Assembly Language programming of 8086 microprocessor.