

SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA
Minor-I (Odd Semester) – 2018

Entry No:

1 7 B C S O 4 5

Total number of pages: [2]

Total number of questions: 8

B.Tech. || CSE || Sem III

Computer Organization & Architecture

Subject Code: CSL2061

Time allowed: 11hr

Max Marks: 20

Instructions

- i. Attempt All Questions.
- ii. Support your answer with neat freehand sketches/diagrams, wherever appropriate.
- iii. Assume any missing data to suit the case / derivation / answer.
- iv. Figures to right indicate full marks

- 1) Consider the following sequence of micro-operations.

MBR \leftarrow PC
MAR \leftarrow X
PC \leftarrow Y
Memory \leftarrow MBR

Which one of the following is a possible operation performed by this sequence?

- | | |
|--------------------------|------------------------------------|
| i. A Instruction fetch | B. Operand fetch |
| ii. C Conditional branch | D. Initiation of interrupt service |

- 2) The program below uses six temporary variables a, b, c, d, e, f

- a. a = 1
- b. b = 10
- c. c = 20
- d. d = a+b
- e. e = c+d
- f. f = c+e
- g. b = c+f
- h. c = b+f
- i. d = 5+c

Assuming that all operations take their operands from register, what is the minimum number of registers needed to execute this program without spilling?

- (A) 2 (B) 3 (C) 4 (D) 1

- 3) The operation executed on data stored in registers is called

- | | |
|--------------------|--------------------|
| a. Macro-operation | b. Micro-operation |
| c. Bit-operation | d. Byte-operation |

- 4) The BSA instruction is

- | | |
|---------------------------------|-----------------------------------|
| a. Branch and store accumulator | b. Branch and save return address |
| c. Branch and shift address | d. Branch and show accumulator |

- 5) Explain the following with an example

- (a) Selective Set (b) Selective Complement (c) Selective Clear (d) Mask (e) Clear Op

4

- 6) With the help of Block Diagram, Show the micro operations involved in fetching, decoding and executing the instruction ISZ 4
- 7) The content of PC in the basic computer is 3AF (all numbers are in hexadecimal). The content of AC is 7EC3. The content of memory at address 3AF is 932E. The content of memory at address 32E is 09AC. The content of memory at address 9AC is 8B9F.
- What is the instruction that will be fetched and executed next?
 - Show the binary operation that will be performed in the AC when the instruction is executed
 - Give the contents of registers PC, AR, DR, AC and IR in hexadecimal and the values of E, I and the sequence counter SC in binary at the end of the instruction cycle. 4
- 8) Consider the following register transfer statements for two 4-bit registers R1 and R2.

$xT: R1 \leftarrow R1 + R2$

$x'T: R1 \leftarrow R2$

Every time that variable T=1, either the content of R2 is added to the content of R1 if $x=1$, or the content of R2 is transferred to R1 if $x=0$. Draw a diagram showing the hardware implementation of the two statements. Use block diagrams for the two 4-bit registers, a 4-bit adder, and a quadruple 2-to-1 line multiplexer that selects the inputs to R1. In the diagram, show how the control variables x and T select the inputs of the multiplexer and the load input of register R1. 4

SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA
Minor-II (Odd Semester) – 2018

Entry No: **17BCS045** Total number of pages:[2]
Total number of questions: 10

B.Tech. || CSE || Sem III

Computer Organization & Architecture

Subject Code: CSL2061

Time allowed: 1.5Hr's **Max Marks: 20**

Instructions

- i. Attempt All Questions.
- ii. Support your answer with neat freehand sketches/diagrams, wherever appropriate.
- iii. Assume any missing data to suit the case / derivation / answer.
- iv. Figures to right indicate full marks

Q1. A CPU has 24-bit instructions. A program starts at address 300 (in decimal). Which one of the following is a legal program counter (all values in decimal)?

- (A) 400 (B) 500 (C) 600 (D) 700 1

Q2. Suppose a processor does not have any stack pointer register. Which of the following statements is true?

- (A) It cannot have subroutine call instruction
(B) It can have subroutine call instruction, but no nested subroutine calls.
(C) Nested subroutine calls are possible, but interrupts are not.
(D) All sequences of subroutine calls and also interrupts are possible 1

Q3. The performance of a pipelined processor suffers if

- (A) The pipelined stages have different delays
(B) Consecutive instructions are dependent on each other
(C) The pipeline stages share hardware resources
(D) All the above 1

Q4. A CPU generally handles are interrupt by executing an interrupt service routine

- (A) As soon as an interrupt is raised
(B) By checking the interrupt register at the end of fetch cycle
(C) By checking the interrupt register after finishing the execution of the current instruction
(D) By checking the interrupt register at fixed time intervals 1

Q5. The instruction “add R0, R1” has the register transfer interpretation $R0 \leftarrow R0 + R1$. The minimum number of clock cycles needed for execution cycle of this instruction is

- (A) 2 (B) 3 (C) 4 (D) 5 1

Q6. An instruction is stored at location 300 with its address field at location 301. The address field has a value 400. A processor Register R1 contains the number 200. Evaluate the

effective address if the addressing mode of the instruction is (a) direct (b) immediate
(c) relative (d) register direct (e) index with R1 as the index register.

3

Q7. The content of the top of the memory stack is 5320. The content of the stack pointer SP is 3560. A two word call subroutine instruction is located in memory address at address 1120 followed by the address field of 6720 at location 1121. What are the content of PC, SP, and top of stack?

- (A) Before the call instruction is fetched from memory?
- (B) After the call instruction is executed?
- (C) After the return from subroutine?

3

Q8. Consider that the 30% of the code of a program can be parallelized to run ideally on multiple processors. The rest 70% of the code is inherently sequential and cannot be parallelized. What would be the speedup achieved by running the program on a two processor computer and also a three processor computer.

2

Q9. Consider a case where k -segment pipeline with clock cycles time t_p is used to execute n tasks. The non-pipeline unit that performs the same operation takes time equal to t_n . Find the speed up ratio. How the ratio reduces to number of segments in the pipeline?

3

Q10 Explain the Concept of Vector processing and pipeline Hazards?

4

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SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA
School of Computer Science & Engineering
B. Tech. (CSE) Major Examination (Odd Semester) 2018-19

Entry No: **17 B C S O 4 5** Total Number of Pages: [2]
 Date: 28th of November 2018 Total Number of Questions: [7]
 Course Title: Computer Organization and Architecture
 Course Code: CSL 2061

Time Allowed: 3 Hours

Max Marks: [50]

Instructions / NOTE

Attempt All Questions.

- i. Support your answer with neat freehand sketches/diagrams, wherever appropriate.
- ii. Assume any missing data to suit the case / derivation / answer.

Section - A				
Q1.	(a) How many 32K x 1 RAM chips are needed to provide a memory capacity of 256K-bytes? (b) Which one of the following is true for a CPU having a single interrupt request line and a single interrupt grant line? A. Neither vectored interrupt nor multiple interrupting devices are possible. B. Vectored interrupts are not possible but multiple interrupting devices are possible. C. Vectored interrupts and multiple interrupting devices are both possible. D. Vectored interrupt is possible but multiple interrupting devices are not possible (c) The search concept used in associative memory is A. Parallel search B. Sequential search C. Binary search D. Selection search (d) The search concept used in associative memory is A. Parallel search B. Sequential search C. Binary search D. Selection search (e) Assume that for a certain processor, a read request takes 50 nanoseconds on a Cache miss and 5 nanoseconds on a cache hit. Suppose while running a program, it was observed that 80% of the processor's read requests result in a Cache hit. The average read access time in nanoseconds is	[02]	CO4	
		[01]	CO3	
		[02]	CO4	
		[01]	CO4	
Q2.	What are Tri state buffers? Explain the working of Bus system for four registers using tri state buffers?	[06]	CO1	
Q3	Draw the flow chart for Interrupt Cycle. What <u>register transfer statement</u> sets the <u>flip flop R to 1</u> ?	[06]	CO1	
Section - B				
Q4.	Explain Daisy Chaining Interrupt Priority? Draw the logic circuit for one stage of Daisy chain priority arrangement.	[06]	CO2	
Q5	A Two Word Instruction is stored in Memory at an address designated by symbol W. The address field of the instruction (stored at W+1) is designated by symbol Y. The operand used during the execution of the instruction is stored at an address symbolized by Z. An index register contains the value X. State how Z is calculated from the other addresses if the addressing mode of the instruction is direct, indirect, relative and indexed.	[06]	CO2	

Q6.	(a) Explain the Floating Point addition and Subtraction algorithm with the help of a flow chart (b) Explain Booths Multiplication algorithm for two signed numbers with the help of an Example	[06]	C03
	[05]	C03	
Q7.	(a) What is Associative memory? Write the match logic for the word of associative memory expressed by the Boolean function (b) Give at least six status conditions for the setting of individual bits in the status register of an asynchronous communication interface	[05]	C04
	[03]	C04	

CO1: To Learn basic micro operations and organization of a basic digital computer

CO2: To Learn Overall organization of CPU, pipelining and vector processing

CO3: To understand various arithmetic algorithms and communication techniques with Input/output devices.

CO4: To understand the organization and operation of various memory.

CO	Questions Mapping	Total Marks	Total Number of Students (to appear in Exam)
CO1	Q2, Q3	12	54
CO2	Q4, Q5	12	54
CO3	6(a), 6(b), Q1(b)	12	54
CO4	Q7(a), Q7(b), Q1(a), Q1(c), Q1(d), Q1(e)	14	54

SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA
Minor-I&II (Odd Semester) – 2019

Entry No: Total number of pages:[2]
Total number of questions: 13

B.Tech. || CSE || Sem III
Computer Organization & Architecture
Subject Code: CSL2061

Time allowed: 1.5Hr's

Max Marks: 30

Instructions

- i. Attempt All Questions.
- ii. Support your answer with neat freehand sketches/diagrams, wherever appropriate.
- iii. Assume any missing data to suit the case / derivation / answer.
- iv. Figures to right indicate full marks

Q1. A CPU has 24-bit instructions. A program starts at address 300 (in decimal). Which one of the following is a legal program counter (all values in decimal)?

(A) 400 (B) 500 (C) 600 (D) 700 1

Q2. Which one of the following Expressions does not represent Exclusive NOR of x and y
(A) $xy+x'y'$ (B) $X \text{ exor } y$ (C) $x' \text{ exor } y$ (D) $X' \text{ exor } y$ 1

Q3. Consider the following sequence of micro-operations.
 $MBR \leftarrow PC$ $MAR \leftarrow X$ $PC \leftarrow Y$ $Memory \leftarrow MBR$
Which one of the following is a possible operation performed by this sequence?
A Instruction fetch B Operand fetch
C Conditional branch D Initiation of interrupt service 1

Q4. A stack organized computer has
(A) Three-address Instruction. (C) Two-address Instruction.
(B) One-address Instruction. (D) Zero-address Instruction 1

Q5. Computer uses addressing mode technique for
(a) giving program versatility to user by providing facilities as a pointer to memory
Counters for loop control
(b) Reducing number of bits in the field of instruction
(c) Specifying rules for modifying or interpreting address field of the instruction
(d) All of the above 1

Q6. A computer has 32-bit instruction and 9-bit address. If there are 400 two address instructions then how many one address instructions can be formulated?
(a) 214 (b) $232 - 200$ (c) $214 - 400$ (d) $(214 - 400) \times 29$ 1

Q7. Suppose a processor does not have any stack pointer register. Which of the following Statements is true?
(A) It cannot have subroutine call instruction
(B) It can have subroutine call instruction, but no nested subroutine calls.
(C) Nested subroutine calls are possible, but interrupts are not.
(D) All sequences of subroutine calls and also interrupts are possible 1

Q8. Consider the following register transfer statements for two 4 bit registers R1 and R2.

$$\begin{array}{ll} xT: & R1 \leftarrow R1 + R2 \\ x'T: & R1 \leftarrow R2 \end{array}$$

Every time that variable T = 1, either the content of R2 is added to the content of R1 if x=0. Draw a diagram showing the hardware implementation of the two statements. Use block diagrams for the two 4 bit registers, a 4 bit adder, and a quadruple 2 to 1 line multiplexer that selects the inputs to R1. In the diagram, show how the control variables x and T select the inputs of the multiplexer and the load input of register R1. 3

Q9. Draw the block diagram of Status register bits? Explain the bits that are set or cleared as a result of an operation performed in ALU. 4

Q10. Draw the flow chart for Memory reference instruction BUN? 4

Q11. The register transfer statements for a register R and memory in a computer are as follows
(The X's are control functions that occur at random)

X3' X1: R \leftarrow M [AR] read memory word into R
X1'X2: R \leftarrow AC Transfer AC to R
X1'X3: M [AR] \leftarrow R Write R to Memory

The memory has data inputs, data outputs, address inputs and control inputs to read and write. Draw the hardware block diagram implementation of R and memory. Show how the control functions x1 through x3 select the load control input of R, the select inputs of multiplexer and read and write inputs of memory. 4

Q12. Draw the block diagram of a bidirectional shift register with parallel loading? Explain its Operation. 5

Q13. Consider the following program segment. Here R1, R2 and R3 are the general purpose Registers.

Instruction	Operation	Instruction size (no.of words)
MOV R1, (3000)	R1 \leftarrow m[3000]	2
LOOP: MOV R2, (R3)	R2 \leftarrow M[R3]	1
ADD R2, R1	R2 \leftarrow R1 + R2	1
MOV (R3), R2	M[R3] \leftarrow R2	1
INC R3	R3 \leftarrow R3 + 1	1
DEC R1	R1 \leftarrow R1 - 1	1
BNZ LOOP	Branch on not zero	2
HALT	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal. Assume that the memory is word addressable. Find the number of memory references for accessing the data in executing the program completely. 3

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SHRI MATA VAISHNO DEVI UNIVERSITY, KATRA
School of Computer Science & Engineering
B. Tech. (CSE) Major Examination (Odd Semester) 2020

Entry No:

Total Number of Pages: [2]

Date: 10th of December 2019

Total Number of Questions: [7]

Course Title: Computer Organization and Architecture

Course Code: CSL 2061

Time Allowed: 3 Hours

Max Marks: [50]

Instructions / NOTE

Attempt All Questions.

- i. Support your answer with neat freehand sketches/diagrams, wherever appropriate.
- ii. Assume any missing data to suit the case / derivation / answer.

Section - A			
Q1.	<p>(a) The Immediate addressing mode of instruction provides the operand in memory location a) Pointed by the PC b) Next to Opcode c) Pointed by PC+1 d) None of these</p> <p>(b) Suppose a processor does not have any stack pointer register. Which of the following statements is true? (A) It cannot have subroutine call instruction (B) It can have subroutine call instruction, but no nested subroutine calls. (C) Nested subroutine calls are possible, but interrupts are not. (D) All sequences of subroutine calls and also interrupts are possible</p> <p>c) The performance of a pipelined processor suffers if (A) The pipelined stages have different delays (B) Consecutive instructions are dependent on each other (C) The pipeline stages share hardware resources (D) All the above</p> <p>d) A CPU generally handles an interrupt by executing an interrupt service routine (A) As soon as an interrupt is raised (B) By checking the interrupt register at the end of fetch cycle (C) By checking the interrupt register after finishing the execution of the current instruction (D) By checking the interrupt register at fixed time intervals</p> <p>e) An output program resides in memory starting from address 2300. It is executed after the computer recognizes an interrupt when FGO becomes 1 (while IEN = 1). i) What instruction must be placed at address 1 ii) What must be the last two instructions of the output program?</p>	[01] [01] [01] [01]	CO1 CO1 CO2 CO3 CO4
Q2.	a) Draw a 4 Bit Arithmetic Circuit? Explain its function table	[06]	CO1
Q3	<p>b) A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register Code part to specify one of the 64 registers, and an address part. i) How many bits are there in the operation code, the register code part, and the address part? ii) Draw the instruction word format and indicate the number of bits in each part. iii) How many bits are there in the data and the address inputs of the memory</p>	[06]	CO1
Section - B			

Q4.	What is an instruction cycle? Draw and explain the flow chart for interrupt cycle.	[06]	CO2
Q5	Show how you can evaluate $X = A + (B * C) / (D - E * F)$ Using a zero address machine.	[06]	CO2
Q6.	(a) How do you arrive at the mathematical equation for the ratio between speedup of a pipeline processing over an equivalent non pipeline processing? Explain? (b) Explain Booths Multiplication algorithm for two signed numbers with the help of an Example	[06]	CO2
Q7.	(a) What is DMA? Elaborate how DMA transfer takes place in a computer system. (b) Draw and explain the flow chart for add and subtract operations	[05]	CO4
		[04]	CO3

CO1: To Learn basic micro operations and organization of a basic digital computer

CO2: To Learn Overall organization of CPU, pipelining and vector processing

CO3: To understand various arithmetic algorithms and communication techniques with Input/output devices.

CO4: To understand the organization and operation of various memory.

CO	Questions Mapping	Total Marks	Total Number of Students (to appear in Exam)
CO1	Q1(a), Q1(b), Q2(a), Q2(b)	14	86
CO2	Q1(c), Q4, Q5, Q6(a)	19	86
CO3	Q1(d), Q6(b)	10	86
CO4	Q1(e), Q7(a)	7	86