school of | Computer Science & Statistics

Reverse Engineering Branch Predictors

Student: Don Browne **Supervisor:** Dr. David Gregg

Background

•Determining the target and outcome of a branch causes a pipeline stall in a CPU.

•Modern CPUs are equipped with predictor structures to allow the CPU to speculatively execute a branch path while waiting on definitive information.

•Writing code that makes optimal use of branch predictor is highly desirable from a performance viewpoint, but manufacturers do not publish information on the predictor structure.

•Project aims to reverse engineer the predictor structures used, in order to gain an insight into how they are organized, and how they work.

Approach

•Write benchmarks in C and assembly to stress the branch prediction units, using a disassembler to ensure that code is correctly generated, and aligned on the desired memory addresses.

•Use the processor's hardware performance counting registers to monitor the number of executed branches, and the amount that were mispredicted.

•Measurements subject to error – so benchmarks are run a large number of times to find consistent results.

•Vary parameters such as number of branches, distance between them, the address bits and the behavior of nearby branches to determine properties.

Branch Predictor Structures

•A Branch Target Buffer (BTB) maps a portion of a branch's address to the target it branched to last.

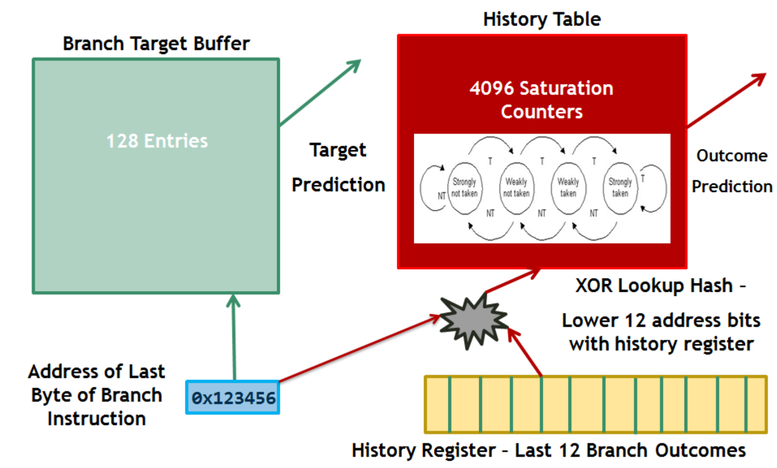
•An Outcome Predictor predicts whether a branch is taken or not, usually using a combination of prior behaviour of the branch, and the behaviour of branches before it, stored in a history register.

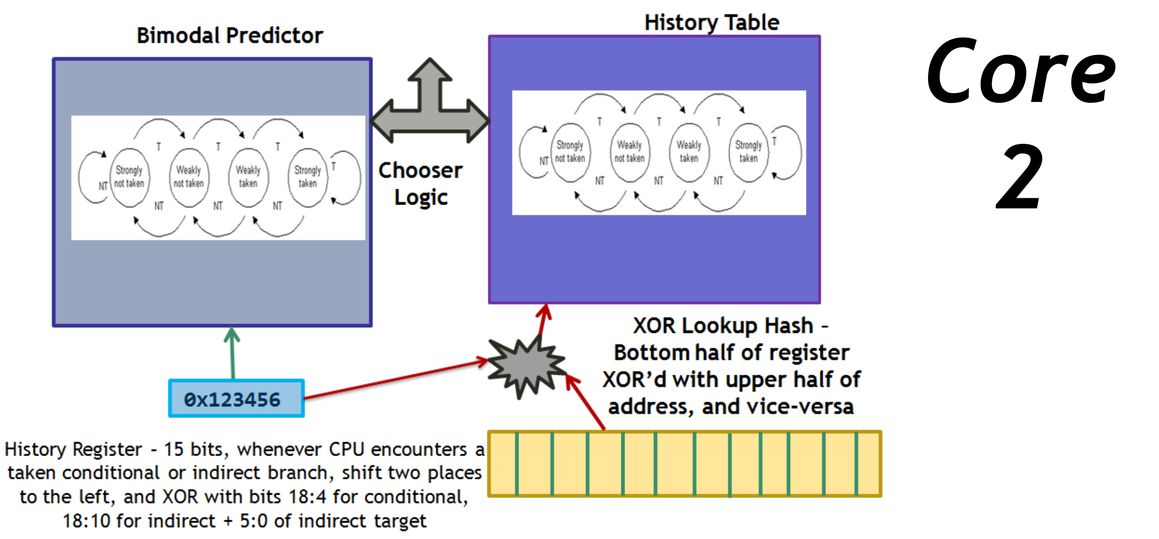
1. A Local Predictor has multiple history registers, to keep track of the past behaviour of each branch.
2. A Global Predictor uses a single register for all branches, which exploits correlations in the behaviour of nearby branches.

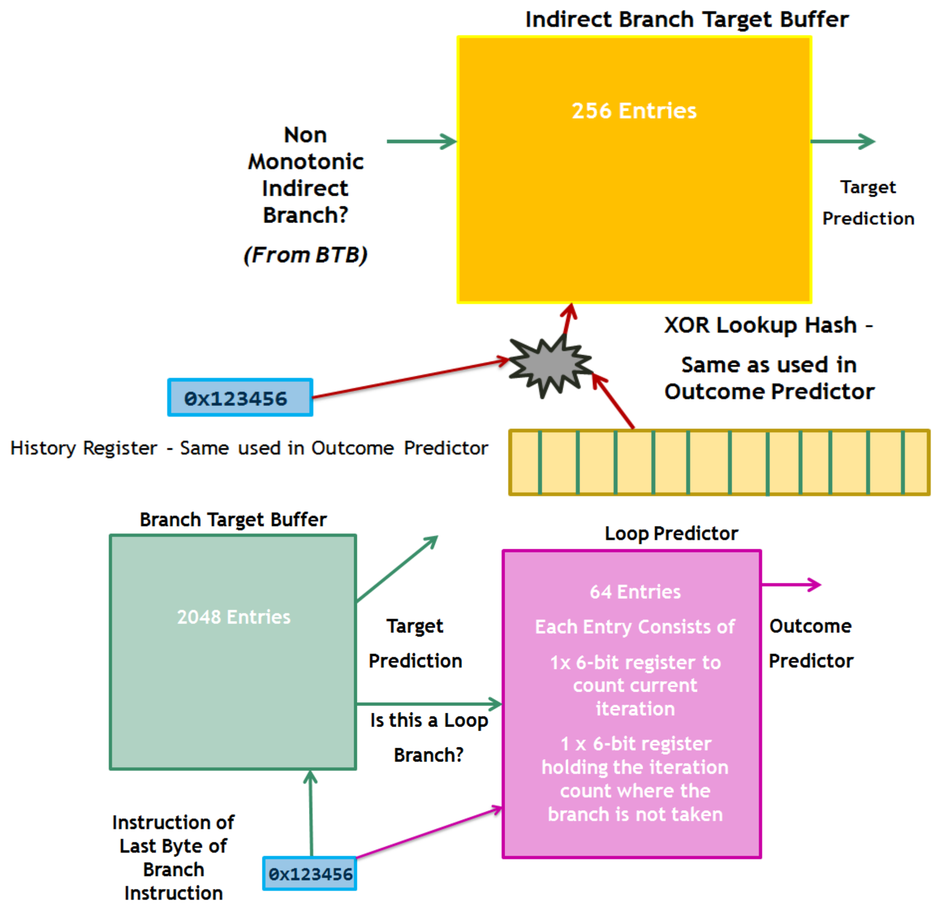
•A Loop Predictor is a specialized outcome predictor that detects branches with loop behavior, and then determines at which point the loop branch should not be taken.

•An Indirect Branch Target Buffer is used to predict the target of an indirect branch that changes its target. It consists of a table that is looked up using a hash of the indirect branch address, and the history register from the outcome predictor.

Intel Atom and Core 2







Conclusion

• The project was successful in developing experiments that could provide information on the branch predictor units in modern Intel CPUs.

•Results have applications in code optimization, and compiler design.

• Benchmarks required a lot of hand tweaking. Future work could investigate ways of automating them.

•May be applicable to non-Intel CPUs to varying degrees.

Don Browne - dobrowne@tcd.ie – 087 617 9755