Redesign Quantum Circuits on Quantum Hardware Device

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In the process of exploring quantum algorithms, researchers often need to conduct equivalence checking of quantum circuits with different structures or to reconstruct a circuit in a variational manner, aiming to reduce the depth of the target circuit. Whereas the exponential resource overhead for describing quantum systems classically makes the existing methods not amenable to serving large-scale quantum circuits. Grounded in the entangling quantum generative adversarial network (EQ-GAN), we present in this article a new architecture which enables one to redesign large-scale quantum circuits on quantum hardware. For concreteness, we apply this architecture to three crucial applications in circuit optimization, including the equivalence checking of (non-) parameterized circuits, as well as the variational reconstruction of quantum circuits. The feasibility of our approach is demonstrated by the excellent results of these applications, which are implemented both in classical computers and current NISQ hardware. We believe our work should facilitate the implementation and validation of the advantages of quantum algorithms.

Quantum algorithms can provide super-polynomial or even exponential speedups compared to their classical counterparts in solving certain important problems [1, 2]. Prominent examples include the Shor's algorithm [3] for factoring integers into their constituent primes, the Grover's algorithm [4, 5] for searching marked items in an unstructured database, and the HHL algorithm [6, 7] for solving linear systems, etc.

Quantum algorithms are commonly programmed using a quantum circuit model of quantum computation, i.e., a quantum algorithm is represented as a certain quantum circuit comprised of a series of quantum However, in the initial stage of quantum gates. circuit design, researchers tend to focus on functional specification, without giving significant consideration to actual implementation. Hence the resultant draft circuits may contain some logic operations, whose corresponding unitaries are known but whose implementations are not explicitly defined, such as the Oracles raised in the Deutsch-Jozsa [8] and Grover's [4, 5] algorithms. Therefore, it is necessary to convert these high-level logic operations into available quantum gates, and this process is known as the quantum logic circuit synthesis [9]. Besides performing it manually, which is a rather labor-intensive and expertise-demanding task in practice, some established techniques can also automatically offer workable results, such as the unitary decomposition [10, 11], genetic algorithm [12], evolutionary algorithm [13], deep reinforcement learning [14], and variational quantum algorithm [15, 16].

Once the explicit quantum circuit has been created through the aforementioned synthesis, further optimization can be applied to reduce its complexity.

Because what a circuit with shallower depth or smaller gate count brings is not only higher efficiency but also lower error rate, it is crucial to refine the circuit as much as possible, especially during the current NISQ era which provides hardware subjected to severely limited qubit coherence time and rather restricted number of reliable operations. Current popular quantum circuit optimization techniques are primarily based on directed acyclic graph [17], ZX calculus [18, 19]. Meanwhile, some jobs [15, 16] suggest the usage of variational quantum algorithm for constructing more compact and even hardware-specific quantum circuits. For example, the Ref. [15] nearly reaches the theoretical limit in 3 -5-qubit circuits optimization.

Depending on their performance, various approaches might yield different results, resulting in the necessity of equivalence checking between their outputs. There are several algorithms that can do this, such as the decision graph [20] for non-parameterized circuits and the ZX calculus [19] for parameterized circuits. However, their chief innovations might fail to work in certain cases, leaving the classical simulation to become the last resort. Suffering from the inefficient classical simulation of quantum systems these approaches scale very poorly with respect to the system's size, and turn impractical as the number of qubits gets large. Thus it is highly desirable to establish an algorithm to manage realistic-scale quantum circuits, that do not suffer performance degradation as the involved qubits increase.

These problems are classically hard but quantumly easy. The Ref. [21] proposes the entangling quantum generative adversarial algorithm (EQ-GAN) to reproduce a given reference quantum state based on quantum hardware [22]. It circumvents the classical simulation of quantum systems, and thereby can be applied to a large scale. The EQ-GAN could always converge to a provably optimal Nash equilibrium and hence avoid

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the mode collapse which may occur in traditional Q-GAN proposals. [23, 24]. In addition, the EQ-GAN permits mitigating uncharacterized coherent error due to miscalibrated gate parameters. However, it cannot be directly used to optimize quantum circuits, because it actually only learns the first column of the corresponding unitary matrix. In our requirements, it is necessary to learn all the elements of the matrix.

In this article, we present a novel approach which permits researchers to redesign large-scale quantum circuits on quantum hardware. We refer to this approach as the RH (Redesign circuits on quantum Hardware) architecture for simplicity. Our RH architecture is established based on the EQ-GAN [21, 22]. Specifically, by introducing an additional random quantum circuit module, the RH architecture can be directly applied to checking the equivalence between different circuits, whether they are parameterized or non-parameterized. Moreover, it is also valid for variationally learning the functionality of a reference circuit by a parameterized one in a different structure, owing to its natural compatibility with the quantum machine learning [25]. The completeness of this architecture has been proven and a shallow random circuit has been suggested. To validate our RH architecture, we exemplarily implement three applications both in classical simulation and Collectively these applications quantum hardware. highlight the utilization scope of the RH architecture.

Our work opens a venue for redesigning quantum circuits using quantum hardware, permitting wide applications such as large-scale quantum circuit optimization, equivalence checking, etc. It is important to highlight that our RH architecture can also be incorporated into other algorithms for further advanced applications. For instance, it can be used to replace the classical simulation which is taken as the last resort in algorithms such as ZX [19] and decision diagram [20] for circuit simplification or optimization. We expect our RH architecture facilitate the implementation and validation of advanced quantum algorithms.

Results

Several important problems fall naturally into the domain of quantum circuit redesign. For the sake of concreteness, we apply our RH architecture to three applications, i.e., non-parameterized (and parameterized) quantum circuit equivalence checking, and quantum circuit variational reconstruction, which capture the core of quantum circuit redesign and simultaneously are limited to be simple enough to be performable by current quantum devices, even if they are also tractable by classical alternatives.

To assess the performance of the RH architecture, we conduct these applications both in numerical simulation and in current NISQ hardware devices. The numerical simulation is performed using the MindSpore Quantum [26], a nascent while rapidly maturing high-performance software package for quantum computation. The

hardware experiments are carried out on the Zuchongzhi-2 quantum processor, a 66-qubit superconducting quantum platform which was used to demonstrate quantum advantage in 2022 [27] and is free publicly accessible via the cloud [28].

Discriminator and Random circuits

Before implementing these applications, we first construct the discriminator circuit and the random circuits, which are depicted in Fig 1 (a) and (b) respectively. The circuits and results obtained herein will be reused in following applications.

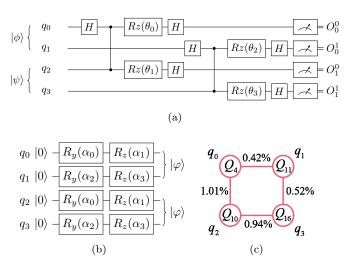


FIG. 1: (a) The discriminator circuit and (b) the random circuits used in this section. (c) The mapping schematic between the logical qubits and the physical qubits arranged in a two-by-two sub-grid within the Zuchongzhi-2 quantum processor. The hardware was calibrated on December 11th, 2024.

The discriminator circuit is a 4-qubit parameterized version of the destructive swap test circuit [29], and is believed to outperform the latter in the presence of coherent error [21, 22]. The discriminator circuit takes two states as input, i.e. $|\phi\rangle$ and $|\psi\rangle$, which are encoded in the first and last two qubits respectively. When $|\phi\rangle$ equals $|\psi\rangle$ to the up to an innocuous global phase, the probability of test failure p_{failure} (i.e., the sum of the probabilities for '0111', '1011', '1101', '1110', '1010', and '0101' to appear in the measurement results $O_0^0 O_0^1 O_1^0 O_1^1$ will be zero. For training the discriminator, we feed it two zero states, i.e. $|\psi\rangle = |\phi\rangle = |\varphi\rangle = |0\rangle^{\otimes 2}$ with reasons explained in section Methods, and update its parameters θ to minimize the p_{failure} , allowing it to eventually act as an effective destructive swap test circuit in a noisy environment.

To explore whether this parameterized discriminator can really mitigate error, in classical simulation, we impose two additional R_z gates (without presenting in figure) after each CZ gate in the discriminator circuit to account for the impact of coherent error [21]. The parameters of these R_z gates are randomly sampled from

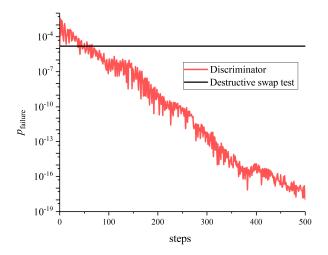


FIG. 2: The probabilities of test failure as functions of training steps.

a normal distribution with $\mu=0$ and $\sigma=0.02$. We initialize the discriminator's trainable parameters $\boldsymbol{\theta}$ with all zeros and update them using the Adam optimizer with an initial learning rate 0.1. When all the parameters $\boldsymbol{\theta}=\mathbf{0}$, the parameterized discriminator degenerates to the original destructive swap test. The loss function is set as the p_{failure} and the batch size is 4.

In Fig. 2, we depict the evolution of the p_{failure} with respect to the training steps. We can see that within 500 training steps the probability of test failure gradually decreases, from the initial value of 1.574×10^{-5} to a minimum of 1.116×10^{-18} . To access results from quantum hardware, we map the utilized 4 logical qubits q_i onto physical qubits Q_i in a 2×2 sub-grid of the 66-qubit Zuchongzhi-2 quantum processor for accommodating the experimental realities. The mapping diagram is illustrated in Fig. 1 (c), where the label of line between physical qubits signifies the error rate in executing the CZ gate. The error rates of single-qubit native gates are between 0.11% and 0.21%. Within 50 training steps, the probability of test failure on the hardware decreases from the initial 4.700×10^{-2} to a minimum of 2.575×10^{-2} (without presenting in figure). The number of shots in experiment is 1000 throughout this article.

In Tab. I, we record the performance comparison of the discriminator before and after training, as well as the specific values of its parameters. The notation θ refers to the result of classical simulations, while θ^* refers to that from hardware experiments. Referring to Tab. I, after training, not only the discriminator reduces the probability of test failure from 6.457×10^{-4} to 6.107×10^{-10} in simulation, but also its parameters perfectly cancel out the instantiated coherent error which is captured in the last row, i.e. $\theta_i = -\text{noise}_i$. These

results indicate that the discriminator actually acquires remarkable error robustness by training.

We emphasize here that during the training process, the $p_{\rm failure}$ is calculated for zero states, while in the final performance evaluation in Tab. I, the $p_{\rm failure}$ is averaged over 100 random quantum states. Their specific values might vary, yet the main conclusion holds.

The random circuits used here, as depicted in Fig. 1 (b), are composed of 4 groups of single-qubit rotation gates with 4 free parameters, i.e. from α_0 to α_3 . By randomly assigning values to the parameters α , these random circuits can create two identical random quantum states $|\varphi\rangle$ in the first two and last two qubits respectively.

Application 1: Non-Parameterized quantum circuit equivalence checking

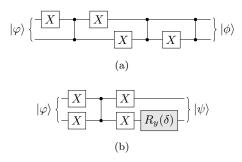


FIG. 3: (a) A two-qubit phase-flipper circuit for basis states $|01\rangle$, $|10\rangle$ and $|11\rangle$. (b) A two-qubit phase-flipper circuit for basis states $|00\rangle$. The gate $R_y(\delta)$ gate in gray is added to introduce a certain amount of difference between two circuits.

The first application to be outlined is checking the equivalence between two non-parameterized circuits. In this subsection, we take the circuits shown in Fig. 3 (a) and (b) as the reference circuit and the generator circuit in the RH architecture respectively. Ignoring the R_y gate in gray, these two circuits are phase-flippers for some computational basis states and therefore have important applications in oracle-based quantum algorithms, such as the Grover's searching algorithm [4]. The reference circuit flips the phases of $|01\rangle$, $|10\rangle$ and $|11\rangle$, while the generator circuit does that of $|00\rangle$.

Attracted by its smaller circuit depth, someone may wonder if the second circuit can be an alternate to the first circuit in practice. The necessity of carrying out an equivalence checking on them naturally arises. To achieve this, we take 100 random states $|\varphi\rangle$ as inputs and study the averaged probability of test failure as the parameter δ of the R_y gate in gray alters. Actually, disregarding the global phase -1, these two circuits are equivalent when $\delta=2k\pi$, where k is an integer, and vice versa.

From Fig. 4, we see that as the δ increases within the interval $[0, 2\pi]$, the probability of test failure first rises from 0 and then falls back, which precisely conforms to the theoretical expectations. Similar conclusion can also be drawn according to the hardware results, whose values

TABLE I: The comparison of the discriminator's performance before and after training, along with the values of its parameters. The notation θ refers to the results from classical simulation while θ^* refers to the results from hardware experiment. The probabilities of test failure p_{failure} in the first column are averaged over 100 random states. The instantiated coherent error in the last row is sampled from a norm distribution with $\mu = 0$ and $\sigma = 0.02$.

$p_{ m failure}$	\i	0	1	2	3
6.457×10^{-4}	θ	0.0	0.0	0.0	0.0
6.107×10^{-10}	$\boldsymbol{\theta}$	4.981×10^{-3}	-1.088×10^{-2}	6.910×10^{-3}	-8.094×10^{-3}
4.552×10^{-2}	$oldsymbol{ heta}^*$	0.0	0.0	0.0	0.0
3.931×10^{-2}	$oldsymbol{ heta}^*$	1.692×10^{-2}	1.618×10^{-2}	-1.114×10^{-2}	5.916×10^{-2}
	error	-4.981×10^{-3}	1.088×10^{-2}	-6.910×10^{-3}	8.093×10^{-3}

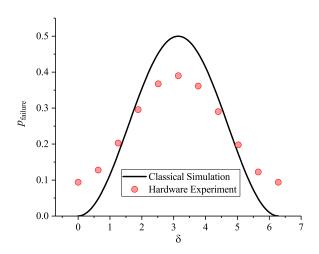


FIG. 4: The averaged probabilities of test failure vary with the value of parameter δ in the circuit shown in Fig. 3 (b).

are very close to those in classical simulation.

Application 2: Parameterized circuit equivalence checking

Owing to the current prevalence of quantum machine learning, checking the equivalence of parameterized circuits is a highly important but simultaneously intractable problem, and there is a lack of universal and effective solutions [19].

In this sub-section, as a representative example, we consider the equivalence checking between two decomposition circuits of the $CR_y(\beta)$ gate, which are shown in Fig 5 (a) and (b), respectively. These two parameterized circuits are equivalent for any β when the parameter of the $R_y(\delta)$ gate in gray satisfies $\delta = 2k\pi$, where k is an integer, and deviates from each other in other cases.

Fig. 6 describes the averaged probabilities of test failure in classical simulation and hardware experiment over 10 random states and 10 random β in terms of

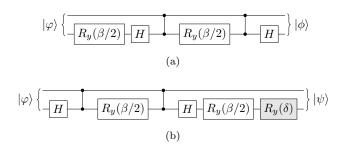


FIG. 5: There are two decomposition circuits which are frequently employed for implementing the $CR_y(\theta)$ gate. The $R_y(\delta)$ gate in gray arises for introducing a certain amount of difference between two quantum circuits.

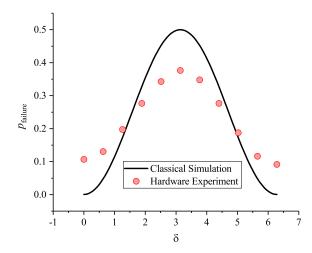


FIG. 6: The averaged probabilities of test failure as functions of the value of parameter δ in the circuit shown in Fig. 5 (b).

the value of δ in the interval $[0, 2\pi]$. The feasibility of checking equivalence between parameterized circuits with random free parameters, i.e., the β herein, has been proven in Ref. [19]. It can be concluded from Fig. 6 that the probabilities of test failure nicely reflect the amount

of deviation between the two circuits as the δ varies.

Application 3: Quantum circuit variationally optimization

The circuit optimization is to construct a new circuit, which is equivalent to the target one but is equipped with less quantum gates or shallower depth. More often than not, in optimizing certain complex circuits, the employment of variational algorithm tends to offer greater accessibility compared to relying solely on the developer's knowledge [30]. The example we present here is to reduce the depth of a particular circuit, which has been illustrated in Fig. 7 (a) in a variational manner. This circuit is the same as that shown in Fig. 3 (a), with a circuit depth of 3. A potential alternate is portrayed in Fig. 7 (b), which comprises two single-qubit R_z gates with trainable parameters β_0 and β_1 , as well as a single CZ gate, and thus its circuit depth amounts to 1.

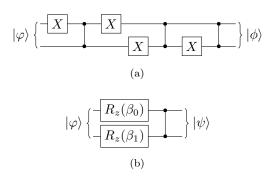


FIG. 7: (a) A phase-flipper circuit composed of 3 CZ gates and 4 single-qubit gates, and its a potential alternative (b) using a single CZ gate and two single-qubit rotation gates.

Within the RH architecture, we designate these two circuits as the reference circuit and the generator circuit respectively. In this example, the settings of the hyperparameters are aligned with those in the previous training of the discriminator, such as the parameters initialization, learning rate, loss function and so on.

Fig. 8 displays how the probability of test failure evolves in relation to the training steps. Fig. 8 reveals that as the training proceeds, the probability of test failure in classical simulation steadily decreases from an initial value of 3.327×10^{-1} and converges to around 1×10^{-14} after about 300 steps. The results from hardware experiment show that the probability of test failure has declined from the initial value of 4.33×10^{-1} to a minimum of 5.495×10^{-2} during a 50-step training procedure (without presenting in figure). The probabilities of test failure during the training are dynamically calculated with respect to a batch of random states sized 4.

The values of the parameters β_0 and β_1 before and after training, as well as the averaged probability of test failure over 100 random quantum states, are listed in Tab. II, where the symbol $\boldsymbol{\beta}$ indicates the results are

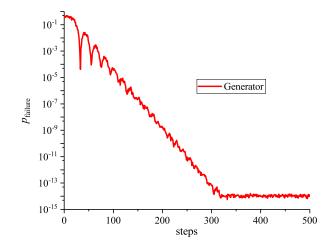


FIG. 8: The averaged probability of test failure evolve with respect to the training steps.

TABLE II: The comparison of the generator's performance before and after training, along with the specific values of the parameters. The notations β and β^* refer to the results from classical simulation and hardware experiment, respectively. The probabilities of test failure in the first column are averaged over 100 random states.

$p_{ m failure}$	i	0	1
4.231×10^{-1}	$\boldsymbol{\beta}$	0.0	0.0
1.020×10^{-14}	$\boldsymbol{\beta}$	-3.1416	-3.1416
3.972×10^{-1}	$oldsymbol{eta}^*$	0.0	0.0
7.491×10^{-2}	$oldsymbol{eta}^*$	-2.847	-3.029

from classical simulation, while $\boldsymbol{\beta}^*$ indicates the results are from hardware experiment.

These observations imply that the RH architecture works well in this application, and the resultant generator circuit can be a competent alternative to the reference circuit in experiment after training.

Methods

Our RH architecture is derived from the EQ-GAN [21], and primarily comprises five sub-circuits as shown in Fig. 9: two identical random circuits, one reference circuit U, one generator circuit U' as well as one discriminator circuit.

The heart of quantum circuit redesign lies in reproducing the functionality of a given n-qubit reference circuit by a n-qubit generator circuit with a new structure. To accomplish this, we need a 2n-qubit quantum system, where the reference circuit is deployed in the first n qubits while the generator circuit is located in the last n qubits. They transform the input random states $|\varphi\rangle$ created by two identical random circuits into

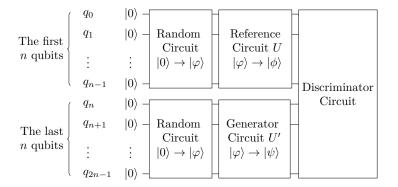


FIG. 9: The schematic diagram of the RH architecture.

the states $|\phi\rangle$ and $|\psi\rangle$ respectively, and then feed them to the discriminator circuit. The discriminator circuit [21] used here is a parameterized version of the destructive SWAP test [29], which can quantify the overlap between its input states $|\phi\rangle$ and $|\psi\rangle$. Specifically, the probability of test failure p_{failure} (obtaining even results of $\sum_i O_i^0 \wedge O_i^1$ on measurement outcomes) equals to the infidelity $1-|\langle\phi|\psi\rangle|^2$ between $|\phi\rangle$ and $|\psi\rangle$, with symbol \wedge referring to the AND operation. Thus, the input states $|\phi\rangle$ and $|\psi\rangle$ are equal up to a phase factor if $p_{\text{failure}}=0$. At this time, we say that the test of the discriminator has been passed, and vice versa.

Ideally, the destructive SWAP test can provide a perfect metric for checking the equivalence between $|\phi\rangle$ and $|\psi\rangle$. Whereas in actual experiment, the two-qubit CZ gate suffers from unstable coherent error due to miscalibrated gate parameters, which oscillate over the timescale of O(10) minutes [31]. This error can be effectively corrected by the following single-qubit R_z gates, whose parameters θ_i will be variationally trained [32].

Our RH architecture starts by training the discriminator's parameters $\boldsymbol{\theta}$ with two identical input states, i.e., $|\phi\rangle = |\psi\rangle$, aiming at minimizing the cost function $p_{\rm failure}$. When $p_{\rm failure} = 0$ the discriminator could act as a perfect destructive swap test even under the influence of coherent error. Considering that the exclusive global optimum of the discriminator is to utterly eliminate the coherent error [21] and any input states will lead to the same result, the zero state $|0\rangle^{\otimes n}$ is suitable for employment as the input states in training to reduce overhead. In other words, the random circuits, the reference circuit and the generator circuit can be ignored temporarily.

Once a discriminator with well performance has been obtained after training, we can employ it to evaluate the overlap between the states $|\phi\rangle$ and $|\psi\rangle$ delivered by the reference and the generator circuits respectively. If the generator circuit is equivalent to the reference circuit, for any identical input $|\varphi\rangle$, their outputs should also be equivalent, and then pass the discriminator's test with

 $p_{\text{failure}} = 0$, namely,

$$p_{\text{failure}} = 1 - \left| \langle \phi | \psi \rangle \right|^2 = 1 - \left| \langle \varphi | U^{\dagger} U' | \varphi \rangle \right|^2 = 1 - \left| \langle \varphi | \varphi \rangle \right|^2 = 0. \tag{1}$$

In practice, as the last resort, researchers often turn to the classical simulation with a limited number of randomly sampled computational basis states to draw an approximate conclusion, when their chief innovation fails to work in equivalence checking. However, using such an approach, realistic sized problems can run for hours and even days without producing deterministic results. Representative works include the ZX calculus [19] and the decision diagram [20], etc.

Moreover, in the worst cases, false negative could still arise [20]. To explain this, we define the difference matrix to capture the error of the new circuit U' with respect to the target circuit U, which takes the form $V = U^{\dagger}U'$. The matrix V is also an unitary matrix and can be implemented by a finite number of primary quantum operations. If U = U', i.e., these two circuits are equivalent, V will be an identity matrix \mathbb{I} , leaving $\left|\langle i|U^{\dagger}U'|i\rangle\right|^{2}=\left|\langle i|V|i\rangle\right|^{2}=\left|\langle i|\mathbb{I}|i\rangle\right|^{2}=\left|\langle i|i\rangle\right|^{2}=1, \text{ for } i\in$ $\{0,\cdots,2^n-1\}$, where $|i\rangle$ refers to the i^{th} computational basis state. Now the problem is transformed into the probability of generating false negative for a nonidentity matrix V during a single test with a random computational basis state. Assuming V includes only one non-trivial operation U_s , one of the most favorable cases is that this operation acts independently on the first of n qubit. Then the matrix of V reads:

$$V = \mathbb{I}_{2^{n-1}} \otimes U_s = \begin{pmatrix} U_s & & \\ & \ddots & \\ & & U_s \end{pmatrix}. \tag{2}$$

In this case, the error is bound to be detected within a single test as none of the elements on the diagonal is 1. By contrast, if the operation acts on the first qubit and controlled by the remaining n-1 qubits, the matrix of

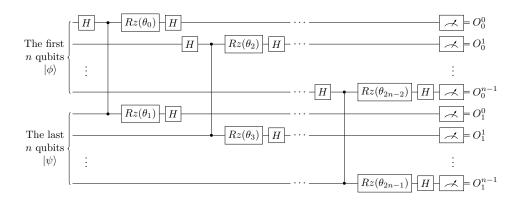


FIG. 10: The construction of the discriminator circuit [21, 22]. The rotation gates $R_z(\theta_i)$ with trainable parameters are utilized to mitigate the coherent error that occurs in the preceding two-qubit CZ gates.

V reads:

$$V = \begin{pmatrix} \mathbb{I}_2 & & \\ & \mathbb{I}_2 & \\ & & \ddots & \\ & & & U_s \end{pmatrix}. \tag{3}$$

The error can be detected with probability of only $1/2^{n-1}$, and the false negative arises with probability of $1-1/2^{n-1}$, representing a worst case. As for other cases, the probability of generating false negative will lie in the interval $[0, 1-1/2^{n-1}]$.

In this work, we employ random quantum states $|\varphi\rangle$ to conduct tests which involve all computational basis states simultaneously. For several random states $|\varphi\rangle$, if the tests always yield the conclusion of equivalence between two circuits, i.e.,

$$1 = \left| \langle \varphi | U^{\dagger} U' | \varphi \rangle \right|^2 = \left| \langle \varphi | V | \varphi \rangle \right|^2, \tag{4}$$

or

$$\sum_{j} V_{i,j} |\varphi\rangle_j = |\varphi\rangle_i \tag{5}$$

up to a global phase, the probability of that they are non-equivalence is statistically zero, and vice versa.

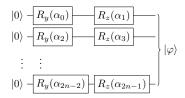


FIG. 11: The local random circuit used in this article is composed of a collection of single-qubit rotation gates (note: this is not a unique construction). By tuning the parameters α_i , this circuit can generate various random states.

There are several approaches that can be used to generate random quantum states. Such as the circuit whose gates are sampled and deployed randomly [33], and the amplitude encoding circuit [34] whose parameters are randomly assigned. Nevertheless, their circuits are quite deep, especially the latter, which gives rise of exponential experimental cost. Here we devise a local random circuit, which is composed of a series of singlequbit rotation gates as illustrated in Fig. 11 and generates quantum states that are the tensor product of n singlequbit random states from the initial state $|0\rangle^n$. worth stating that although this circuit cannot generate isolatable entangled states, they will naturally exist as components in a certain amount in the resultant states. For example, $(|00\rangle + |01\rangle + |10\rangle + |11\rangle)/2$ can be viewed arithmetically as a superposition of entangled states $(|00\rangle+|11\rangle)/\sqrt{2}$ and $(|01\rangle+|10\rangle)/\sqrt{2}$. Another important reason for employing random quantum states is that they keep the training process in an open-loop style, reducing the susceptibility of the optimization to local optima akin to the usage of random samples in the training landscape of classical neural networks [35].

Conclusion

In this work, we proposed a novel RH architecture for redesigning large-size quantum circuits, which are notoriously difficult to implement with existing methods related to classical simulation. The RH architecture is built upon the EQ-GAN that is proposed to replicate a given reference quantum state. By introducing an additional random circuit module, this architecture can be immediately used to checking equivalence between two circuits in quantum hardware, which is immune to the system's size and therefore can be scaled up to serve large-scale circuits. This architecture's completeness was explained, and an efficient random quantum circuit structure was provided.

We demonstrated the feasibility of the RH architecture by three specific applications, namely, the equivalence verification between (non-) parameterized circuits, and the functionality reproduction of a reference circuit with another parameterized circuit in a variational manner. Evaluation results from both classical simulation and quantum hardware confirm that the RH architecture achieves the expected performance. The RH architecture is also compatible with other established methods in circuit optimization, such as the ZX calculus and decision graph. We believe that our RH architecture would help boost innovation in designing advanced quantum circuits.

Data availability

The data that support the findings of this study are openly available at the following URL/DOI: https://gitee.com/mindspore/mindquantum/tree/research/paper with code.

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Author contributions

R.H. He and S.G. Ying established the key idea in this paper. R.H. He did the experiments and wrote the first

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Competing interests

The authors declare no competing interests.

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