An Electrical Signal Disturbance Detector and Compressor Based on FPGA Platform

Eder Barboza Kapisch
Leandro Rodrigues Manso Silva
Carlos Henrique Nascimento Martins
Alexander Silva Barbosa
Carlos Augusto Duque, *IEEE Senior Member*
Luciano Manhães de Andrade Filho
Augusto Santiago Cerqueira
Federal University of Juiz de Fora
Juiz de Fora, Brazil
leandro.manso@engenharia.ufjf.br

***Abstract*— This paper presents a prototype system used to detect and compress disturbances commonly found in electrical signal, on both voltage and current. The algorithm for detecting and compressing the disturbances are synthesized in FPGA platform. The compression algorithm operates in three different stages: the innovation stage, the wavelet stage and the bit compression stage. These three stages provide efficient compression rate. Beside the algorithm description, the paper presents details of the hardware implementation and results obtained from synthetized and real signals.**

***Index Terms*— Detector, Compressor, Power Quality, Data Logger, Wavelet, FPGA.**

I. INTRODUCTION

Continuous data acquisition of electrical signal is required in many power system applications such as protection, control and power quality analysis. The reason for acquiring and storing a large amount of data is supported by the fact that the post-processing of the data can uncover information not previously observed, allowing system enhancement, troubleshoot, algorithm optimization, among others.

However, continuous raw data recordings of electrical signal (voltage and current) is not a simple task due the large amount of data to be recorded and later transferred from the local site to expert room where the data will be post-processed. Besides, few commercial types of equipment are currently available to record continuous raw data at high sampling rate [1]. In general the available equipments are application oriented and are used only for acquiring a short-term of failure signal or disturbance signal. Two examples of commercial equipment that acquire raw data are Waveform Power Quality Data Analyzer (PQDA) and Digital Fault Recorders (DFR). The first one is specialized for detecting a specific disturbance, while the last one is designed to capture faulted current.

However, in the new context of smart-grid, where the behavior of the grid is not clearly understood by the scientists and engineers, the continuous raw data acquisition and the post-processing of the saved data can be extremely important to identify deviation in the system operation, protection and control and can be used to find further information [1]-[3].

It is clear that the raw data recorder will always be of great importance in power systems, and especially so now, with the growth of smart grids. Of course, it is expected that the data recorder becomes smarter in order to reduce the amount of data without losing information. In this direction, the concept of innovation [4] is very attractive. This concept, in the context of event detecting, says that only a frame of data containing new information, or innovation, must be saved for future analysis. This requires adaptive trigger systems and efficient detectors. Furthermore, smarter recorder requires an efficient compress mechanism that can be applied in real time, for example, the ability of the discrete wavelet transform (DWT) [5]-[7] to sparse the signal is widely used in real time compression.

In addition, another tendency of digital system design is adopting reconfigurable hardware, such as FPGA (Field Programmable Gate Array) [8]–[9]. With reconfigurable hardware, it is possible to synthesize dedicated signal processing algorithm or develop a specialized microprocessor.

This paper is divided as follows: section II describes the proposed methodology, section III shows the real time implementation, section IV shows the results obtained and in section V the conclusions are presented.

978-1-4673-6487-4/14/$31.00 ©2014 IEEE

II. PROPOSED METHODOLOGY

The proposed methodology divides the signal in frames containing four cycles of the fundamental frequency and it is able to detect the frame that is different of the reference one. The methodology is composed of four principal blocks as shown in Fig. 1: (a) the Innovation Detector; (b) the Frequency Estimation; (c) the Wavelet Compression; and (d) the Coding. The last one is implemented in an ARM platform and the others in a FPGA platform.

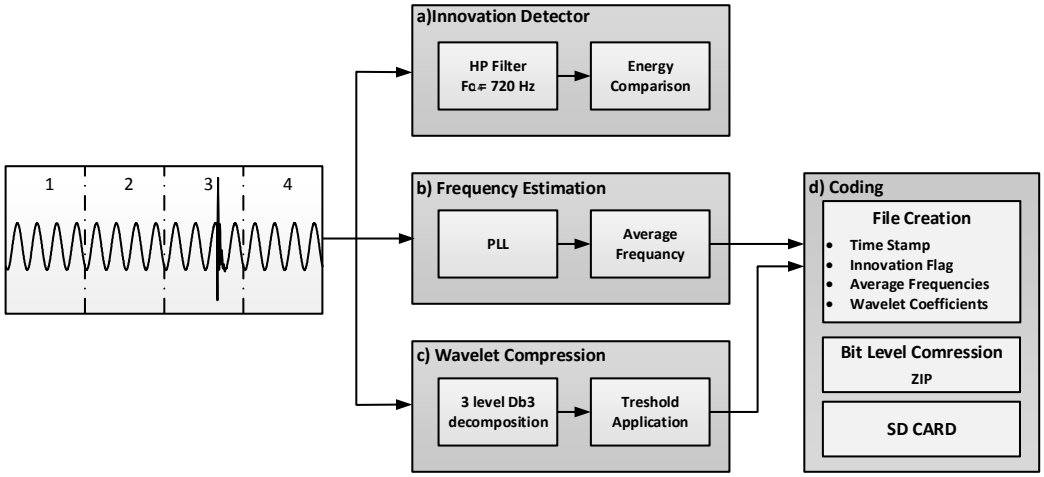

Figure 1. General block diagram.

A. Inovation Detecion

The innovation detector consists in a block that compares one frame with the reference one in order to detect if this frame presents an innovation or not. The detector should be immune to frequency variations; for this it includes a high pass filter with cutoff frequency of 720 Hz to eliminate all the components of low frequency, (where in power system signals is the part of the spectrum with larger energy). After filtering the energy of the processed frames are compared and if it is higher than a threshold, the actual frame is said to an innovation frame. The energy comparison was chosen since it presented better results in noisy scenarios.

This block is the first compression level of the methodology since only the innovation frames are effectively saved.

B. Wavelet Compression

In this block, the signal is decomposed using a three level wavelet tree that uses the mother wavelet Daubechies 3. The decomposition tree is show in Fig. 2 where H_d is highpass filter, L_d the lowpass filter and the black part in the rectangles represents the down sampling by two operation. The output coefficients CD_1, CD_2, CD_3 are the detail coefficients and CA_3 is the approximation coefficient.

The detail output coefficients are compared with a threshold and if they are higher than the threshold they are kept otherwise they are made equal zero, performing the second level of compression of this methodology. The compression in this stage is measured by the number of zeroes in the result coefficients after the threshold application.

C. Frequency Estimation

The PLL implemented was present in [10]-[11] is shown in Fig. 3. It estimates the instantaneous frequency of the signal. This frequency is used to calculate the average frequency of each cycle of the input signal and these frequencies are used in the reconstruction stage that is done offline.

The frequencies are useful because only the innovation frames are saved and we need to reconstruct all the signal. So, the non-innovation frames are reconstructed based on the frame of reference (the last frame of innovation) and on the average frequencies.

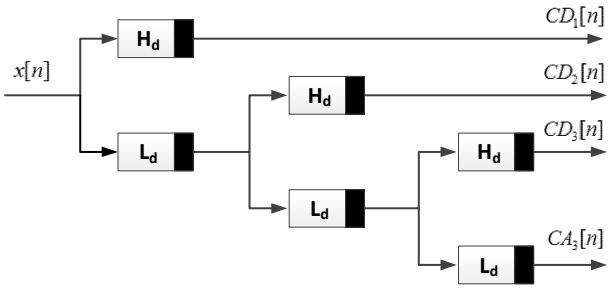

Figure 2. Wavelet decomposition.

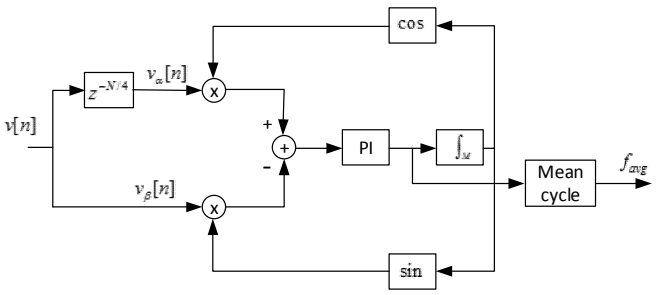

Figure 3. Block diagram of the PLL algorithm.

D. Coding

The coding stage is responsible for compress data in bit level. The data are collected in a predefined structure composed of the header information, the average frequencies and the wavelet coefficients, then a ZIP algorithm to compress is applied and the lossless data compressed is save in a SD Card. All the bit compressing operation and recording are processed in in real time.

The ZIP algorithm used is the Lempel-Ziv-Welch (LZW), described in [12] and consists in the third level of compression of the proposed methodology.

III. REAL TIME IMPLEMENTATION

The methodology described above was implemented in real time using two platforms a FPGA responsible for the Innovation Detector, the Frequency Estimation and the Wavelet Compression, and an ARM Cortex M4 responsible for the Coding Block and the SD Card Control.

A. FPGA

The FPGA used for the signal processing algorithms implementations is from the company ALTERA®, it belongs to the Cyclone IV family (model EP4CE22F17C6). This FPGA has 22,320 logic elements, 154 pins, 608,256 memory bits and 4 PLLs [13].

The clock reference used is 50 MHz, a PLL was used to generate a 12.5 MHz clock for the systems and a 2.5 MHz clock for SPI communication between the FPGA and the ARM processor. The data acquisition block, not shown in Fig. 1 is controlled by the e FPGA. The sample rate used was 7.68 kHz, resulting in 128 points per cycle of 60 Hz. The A/D converter (AD7606 from Analog Device) used has a 16 bits resolution and is capable of converting 8 channels simultaneously. It has three modes of interface, serial, parallel with byte mode and word mode. The interface used is the word mode, where the 16 bits of the data are read at same time.

The hardware that does the entire signal processing, as well as the proposed methodology is divided in three main blocks, they are the Innovation Detector, the Frequency Estimator and the Wavelet Decomposition.

The innovation detector consists of three main blocks: a high-pass filter, a block for adjustment of the threshold level and a block that divides the signal into frames, calculates the energy of each frame and makes the comparison with the reference one.

As stated previously, the innovation detection must be immune to frequency deviations on the fundamental component. To make this possible, a digital high-pass FIR filter of 10th order with cutoff frequency of 720 Hz was implemented. For this filter, a specific hardware was implemented in order to save the FPGA resources. This implementation uses only one multiplier to do the filtering process. A simple diagram of the filter is shown in Fig. 4.

The block that makes the threshold level adjustment provides an adaptive threshold level according with parameters prescribed by the user. These parameters are related to the desired level of compression, the amount of noise permitted, and the similarity between the reconstructed signal and the original one.

The third block is of fundamental importance; it performs the calculation of the energy of each frame and compares it with the energy of the reference frame besides the control of the operation of the other blocks.

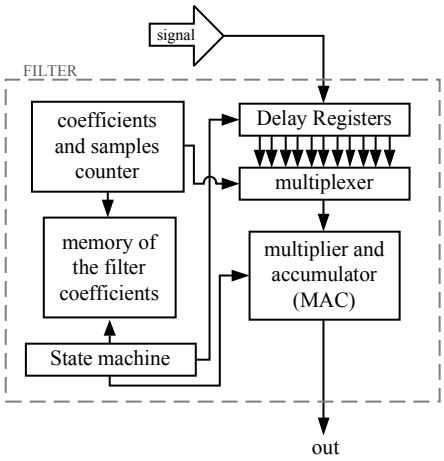

Figure 4. Block diagram of the high-pass filter.

A dedicated processor implemented in the FPGA does the wavelet decomposition. The blocks that constitutes this processor are show in the diagram of Fig. 5. This processor has a Harvard architecture and works with a small set of instructions (RISC). In this diagram the signal is first converted from the fixed point to floating point representation; the calculations are performed in floating point and later converted from floating point to fixed point.

The processor consists of several processing blocks, among which we can highlight the 32 bits floating point Arithmetic and Logic Unit (ALU) that works with a 25-bit mantissa and an 8-bits exponent. The program counter (PC) that holds the address of the actual instruction. The instruction decoder block that is responsible for translating the information from the instruction memory, identifying the part of the instruction word that is referent to the operation code (opcode) for the ALU and the memory address of the operand. This processor also has a data stack, that is implemented as a part of the data memory and with an address stack (stack in the diagram) used to implement the call of subroutines. The processor is able to complete each operation in a single clock cycle. A custom C and an Assembly compilers were developed for this specific processor using the GNU tools FLEX [14] and BISON [15], so that the code of the wavelet algorithm could be implemented in C language and the compilers were responsible to generate the machine code.

The frequency estimation is done by other instance of the same processor that, this time, implements the PLL algorithm cited above.

B. ARM

The ARM processor that was used is of the Stellaris/Tiva family, from Texas Instruments. It is a 32-bit ARM Cortex™-M4F 80-MHz processor with single-precision Floating-Point Unit (FPU), and multi-channel serial/SPI interfaces [16]. The functions of the ARM processor are: data compress, SD card management and system management and communication.

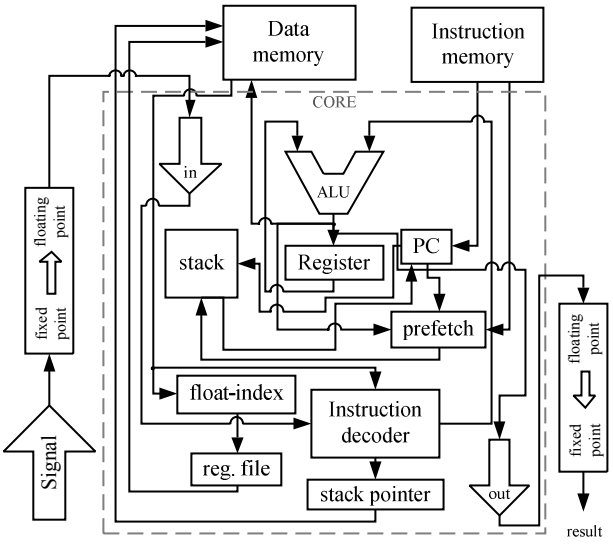

Figure 5. Block diagram of the dedicated processor, implemented in FPGA.

For data compression the algorithm that was used is a modification of the LZW (Lempel-Ziv-Welch) in order that it is capable to run in real time embedded in the ARM processor. The main modification of LZW was restriction of dictionary size which allows a fast search of data sequences.

The SD card management is done by the interface with a dedicated IC (CH376 [17]) that has the entire file system responsible for arranging the files and directories inside the SD card. The ARM has to control the operation of that chip as well as sends the data that will be stored. This data is composed by the data processed by the FPGA, by a time stamp acquired from a RTC (Real Time Clock) and some control bytes need to the decompress algorithm.

The ARM has also the function of saving some parameters of calibration and settings done by the user such as desired compression level, number of channels that will be used and others need to reconstruct the waveform of the signal.

The system has two channels of communication with user, a USB-Serial link and Bluetooth. Both of them are managed by the ARM processor and are used to parameterize the equipment and to provide debug information. Fig. 6 shows a picture of the implemented system.

IV. Results and Discussions

The prototype shown in Figure 6 was tested with a large variety of signals. Some of them synthetic signals generated by a signal generator and real signals from power system. The generated signals were power systems characteristic signals such as transients, harmonics, sags, swells and interruptions. It is important to notice that the signals were conditioned either by the function generator (in the case of the synthetic signals) or by a signal conditioner board (in the case of real signals).

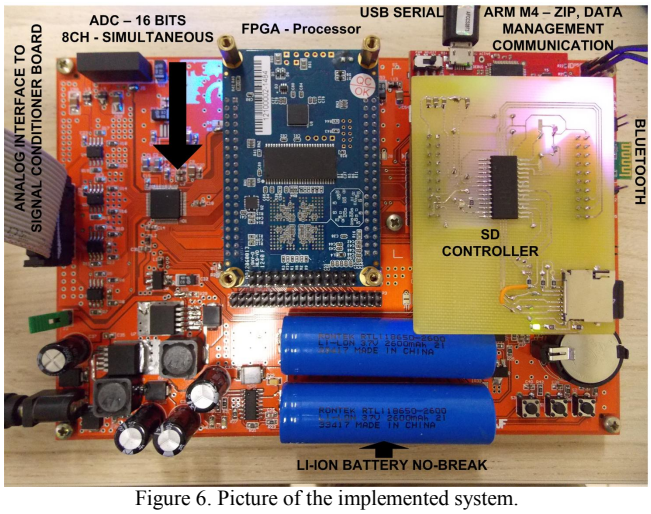

Figure 6. Picture of the implemented system.

The results can be evaluated in three steps of compression: first the compression done by the innovation detection, second the compression done by the wavelet coefficients threshold and finally the bit level compression done by the LZW algorithm.

The results of the first step can be seen through a signal from the FPGA. This signal is named Innovation FLAG and can be seen together with the test signal in the oscilloscope screen of Fig. 7. This flag means that only the signal frames when the Innovation FLAG is in logic level '1' will be stored. In this case it can be noted that only the frame that contains the transient and the next frame will be stored.

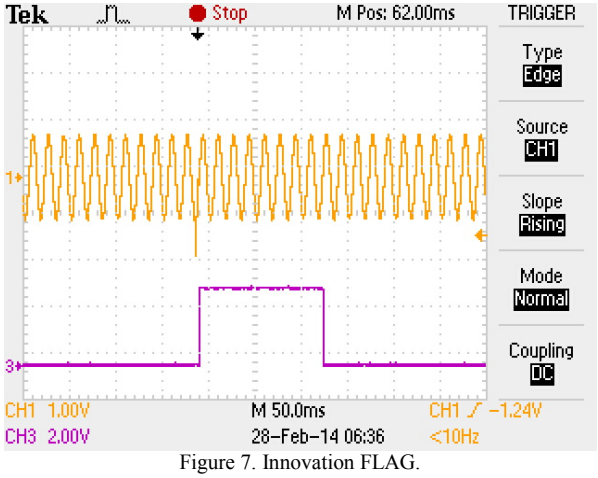

Figure 7. Innovation FLAG.

In the next level, the wavelet coefficients of the innovation frames are submitted to a threshold in order to discard the low energy coefficients that are not necessary to a good reconstruction of the signal. This stage performs a lossy compression since some information will not be stored and the reconstruction of the signal will not be a perfect reconstruction. Fig. 8 shows an example of a wavelet coefficient before and after the threshold application.

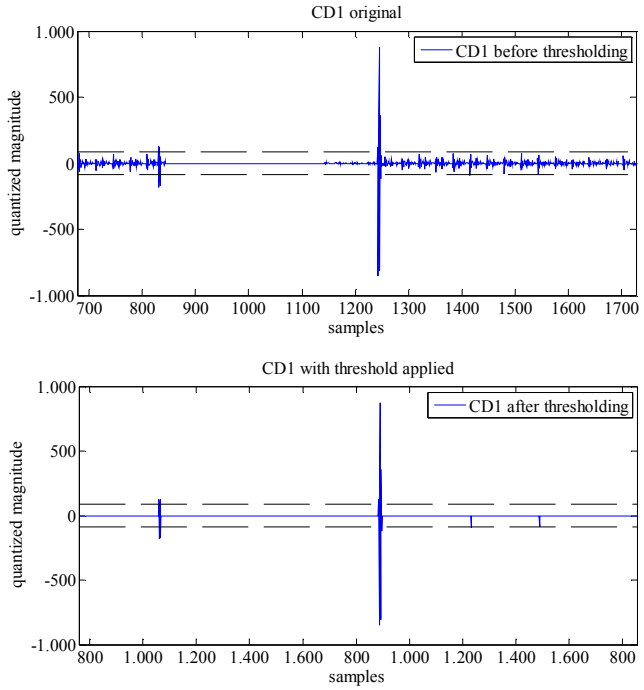

Figure 8. CD1 before (top) and after thresholding (down).

In the present example, 80% of the samples were eliminated (made equal zero) resulting in a reconstruction keeping 99.98% of the energy of the original signal and with a mean squared error in the order of 10^{-4} that is satisfactory in most of the cases. It can be noticed that if a perfect reconstruction is desired the threshold level must be done equal to zero by the user.

The third step consists in a lossless compression done by the LZW algorithm and is capable to reduce the size of the file that will be stored to 60% of its size before the LZW application.

V. CONCLUSION

The proposed method was efficient in compression of the power systems signal, being capable of dealing with all electrical disturbances and also in frequency deviation scenario. Great part of the obtained performance is due the innovation detection that identifies the frames of the signal that have new information and truly need to be stored.

The real time implementation in FPGA and ARM proves the efficiency of the methodology compressing synthetic and real signals. The compression rate is tightly dependent of the innovation rate of the signal and the parameter set by the user such the desired perfectness of the reconstruction.

ACKNOWLEDMENTS

This work was supported in part by CNPq, CAPES and FAPEMIG (Brazilian research agencies). We would like to thanks the KRON MEDIDORES ELETRONICOS for its partnership.

REFERENCES

[1] H. Maass, H. K. Çakmak, W. Suess, A. Quinte, W. Jakob, Karl-Uwe Stucky, and U. G. Kuehnapfel, "First Evaluation Results Using the New Electrical Data Recorder for Power Grid Analysis," IEEE Trans. On Instrumentation and Measurement, Vol. 62, No.0, pp. 2384-2390, September 2013.

[2] Martins, C.H.; Silva, L.M.; Duque, C.; Cerqueira, A.S.; Teixeira, E. C.; Ribeiro, P.F., "A new time-varying harmonic decomposition structure based on recursive hanning window," *Harmonics and Quality of Power (ICHQP), 2012 IEEE 15th International Conference on* , vol., no., pp.70,75, 17-20 June 2012.

[3] R. Zivanovic, P. Schegner, O. Seifert and G. Pilz, "Identification of the Resonant-Grounded System Parameters by Evaluating Fault Measurement Records," IEEE Transactions on Power Delivery, vol.19, no.3, pp.1085-1090, July.2004.

[4] Duque, C.A.; Ribeiro, M.V.; Ramos, F.R.; Szczupak, J., "Power quality event detection based on the divide and conquer principle and innovation concept," IEEE Trans. On Power Delivery, Vol. 20, No. 4, pp. 2361-2369, 2005.

[5] Livani, H.; Evrenosoglu, C.Y., "A Machine Learning and Wavelet-Based Fault Location Method for Hybrid Transmission Lines,"IEEE Transactions on Smart Grid, vol.5, no.1, pp.51, 59, Jan. 2014.

[6] Ming Zhang; Kaicheng Li; Yisheng Hu, "A High Efficient Compression Method for Power Quality Applications," IEEE Transactions on Instrumentation and Measurement, vol.60, no.6, pp.1976, 1985, June 2011.

[7] Bezerra Costa, F., "Fault-Induced Transient Detection Based on Real-Time Analysis of the Wavelet Coefficient Energy," IEEE Transactions on Power Delivery, vol.29, no.1, pp.140, 153, Feb. 2014.

[8] Cheng Qiong and Wang Zhao-Hui, "Research and Design of Portable Fault Recorder Based on FPGA", Elsevier Energy Procedia, Vol 12, pp. 686-692, 2011.

[9] A. D. Femine, D. Gallo, C. Landi, and M. Luiso, "Quality Monitoring Instrument With FPGA Transducer Compensation", IEEE TRAN. On INSTRUMENTATION AND MEASUREMENT, VOL. 58, N° 9, SEPTEMBER 2009, pp. 3149-3158.

[10] da Silva, SA Oliveira, Rhodolfo Novochadlo, and Rodrigo Augusto Modesto. "Single-phase PLL structure using modified pq theory for utility connected systems." Power Electronics Specialists Conference, 2008. PESC 2008. IEEE. IEEE, 2008.

[11] Ciobotaru, Mihai, Remus Teodorescu, and Frede Blaabjerg. "A new single-phase PLL structure based on second order generalized integrator." Power Electronics Specialists Conference, 2006. PESC'06. 37th IEEE. IEEE, 2006.

[12] Nandi, Utpal, and Jyotsna Kumar Mandal. "A Compression Technique Based on Optimality of LZW Code (OLZW)." Computer and Communication Technology (ICCCT), 2012 Third International Conference on. IEEE, 2012.

[13] ALTERA® Corporation, "Cyclone IV Device Datasheet", Cyclone IV Device Handbook, vol. 3, July 2010.

[14] V. Paxson: (1995), "Flex, Version 2.5: A Fast Scanner Generator," http://www.gnu.org

[15] C. Donnelly, R. Stallman: (2002), "Bison: The YACC-Compatible Parser Generator," http://www.gnu.org

[16] DATA, TEXAS INSTRUMENTS-PRODUCTION. "Tiva™ TM4C123GXL Microcontroller." (2013).

[17] DATA, Nanjing QinHeng Electronics Co., Ltd. "File manage and control chip CH376", http://wch-ic.com/download/down.asp?id=121