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Online Pulse Compensation for Energy Spectrum Determination: A Pole-Zero Cancellation and Unfolding Approach

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Abstract: Signal conditioning circuits, in particle energy spectrum determination systems, introduce shaping characteristics that affect pulse integrity. This study explores algorithms to compensate for these effects, focusing on digital signal processing for pole-zero cancellation (PZC) and unfolding techniques. The PZC algorithm successfully corrects baseline shift and pulse amplitude loss, providing significant improvements in signal fidelity. Although a digital PZC applied in streaming for high event rates was previously not feasible, this work proposes its implementation on FPGA, combining it with the unfolding method to enable online compensation and enhanced performance under various experimental conditions.

Keywords: signal conditioning; digital signal processing; inverse problems; FPGA implementation; high-energy calorimetry

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1. Introduction

Pulse detectors are essential measuring instruments in high-energy physics, astronomy, and nuclear physics, among others. They can interact with short-duration phenomena, such as particle interactions, and provide corresponding electrical pulses, albeit with a low electrical charge. These pulses, while small in magnitude, carry crucial information about the energy of interacting particles, contributing to the energy spectrum determination, which is key for precise analysis and understanding of the underlying physical processes.

The instrumentation of these detectors involves pulse conditioning circuits and an analog-to-digital converter (ADC), as illustrated in Figure 1. The conditioning circuits shape the signal to mitigate noise and optimize it for digitization [1], while the ADC converts the conditioned signal into a digital format suitable for storage and detailed computational analysis.

These devices often employ scintillators optically coupled to photomultipliers sensors, with silicon photomultipliers (SiPMs) being a widely adopted choices [2,3]. The emergence of SiPMs in many recent detection systems is driven by their advantages, such as compactness, low operating voltage, and high sensitivity to light. Nevertheless, this widespread adoption comes with the need for careful signal processing, as their inherent

noise [4]. Connected to the SiPMs, charge-sensitive preamplifiers (CSPs) play a crucial role in front-end readout system to collect the charge generated by the photodetector and convert it into a voltage signal with amplitudes suitable for the acquisition system [5]. Nonetheless, these components introduce additional noise [6].

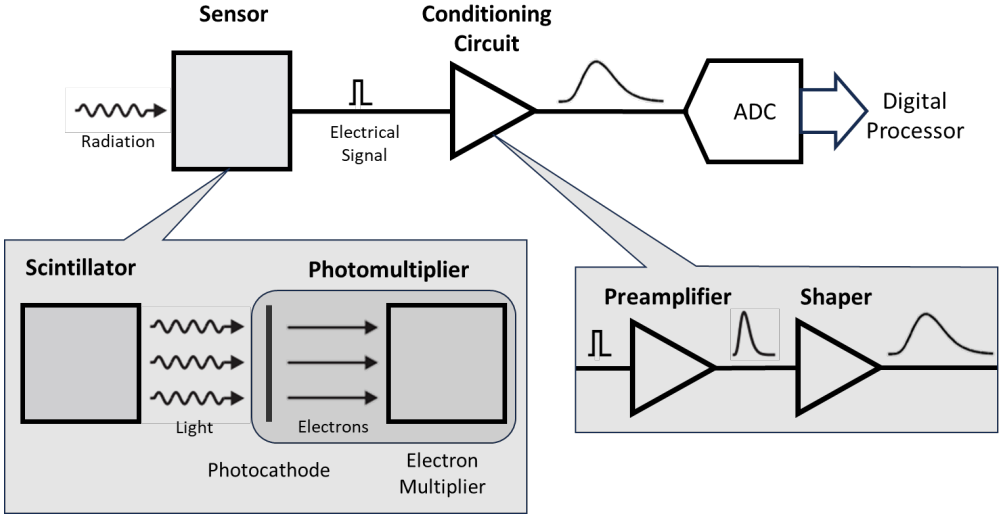

Figure 1. Block diagram of detector's readout chain, and details in the most important blocks.

The combined noise from these sources, along with other potential contributors, poses a significant challenge in energy spectrum measurements, where precise determination of the time of flight and the pulse amplitude are essential for accurately estimating the particle interaction energy. To address noise challenges, filtering techniques by the pulse shaper circuit (PSC) are employed [3].

The typical and simplest configuration of a PSC is the CR-nRC, consisting of a high-pass filter stage followed by n low-pass filter stages [1,7]. This configuration also handles the intrinsic waveform characteristics of SiPM-based detectors, characterized by extremely short rise and fall times (on the order of a few nanoseconds). The increased dynamic range requirements of these waveforms pose significant challenges for digitization in digital processing approaches without prior analog conditioning, as they demand high sampling rates that are often technologically challenging or economically impractical, especially in multi-channel systems. However, the signal conditioning process not only enhances the signal-to-noise ratio but also stretches the pulse duration. This pulse stretching effectively reduces the required sampling rate, alleviating the technological constraints on the acquisition system.

An undesired effect that can arise from pulse stretching is signal pile-up, which is also influenced by the event rate. High event rates combined with wide pulse shapes significantly increase the probability of pile-up. Such pile-up distorts the measured amplitude, deviating it from the true signal amplitude, as presented in Figure 2. When the event rate is known, the PSC can be designed to balance the need for pulse extension to reduce noise with the requirement to minimize pile-up.

Another strategy to mitigate pile-up involves the use of a high-pass filter, which narrows the output pulse widths, thereby decreasing the pile-up probability. However, high-pass filters force the pulse average to zero, introducing negative components into the signal. The accumulation of these negative components leads to an undershooting effect with potentially long time constants, resulting in tail pile-up and causing a baseline shift, as presented in Figure 3 [8]. Inevitably, a coupling capacitor is required in the signal conditioning circuit to block the high supply voltage of the photomultiplier from reaching the readout chain, effectively functioning as a high-pass filter.

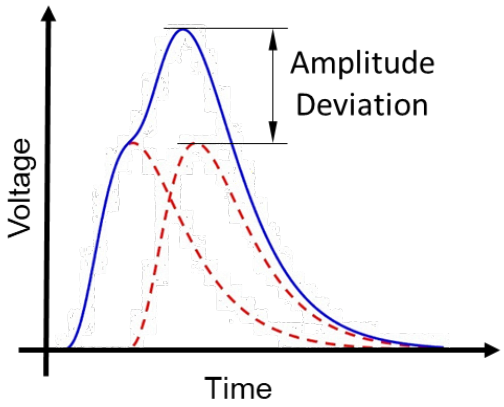

Figure 2. Pile-up effect: two pulses, represented by the red dashed lines, are readout simultaneasly, resulting in a distorted pulse, represented by the blue continous line.

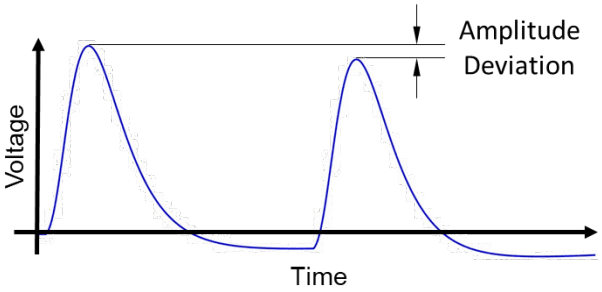

Figure 3. Baseline shift effect.

Baseline shift can be mitigated by incorporating a parallel resistor with the coupling capacitor to achieve pole-zero cancellation (PZC) [8]. Regarding pulse width, reducing it before digitization impacts the design of the digitization system. A potential approach is to maintain a wide pulse with a optimal time constant to reduce noise, while avoiding additional high-pass filtering stages. This highlights the trade-off in analog processing: it can effectively reduce noise and correct baseline shift but does not address pile-up, leaving it as an untreated effect.

PSCs are traditionally implemented through analog approaches, and they have increasingly been adapted to digital implementations using high-speed digitizers in specific applications [9–11]. Digital signal processing offers several advantages, including the ability to implement advanced filtering functions that are impractical in analog circuits, ease of parameter adjustments, adaptive filtering, and efficient correction of baseline shift and pile-up effects [1,12]. Consequently, a hybrid approach that leverages both analog and digital processing provides a compelling solution for balancing performance, complexity, and cost in modern detection systems.

In digital processing, deconvolution, or unfolding, algorithms described by Jordanov [13,14], Difulvio [12], Zeng [15], Födisch [16] and Stezelberger [17] are highly efficient at canceling modal components, enabling both pulse narrowing and undershooting reduction. Consequently, the larger pulse width required for digitization is no longer a limitation, as it can be narrowed post-digitization, effectively mitigating pile-up and restoring the original signal characteristics. Furthermore, the traditional analog approach, using a resistor is unnecessary, since a digitally implemented unfolding PZC algorithm performs this task efficiently while offering the advantage of online adjustment.

According to Jordanov [18], implementing a stable digital PZC algorithm requires resetting the internal states of its feedback circuitry upon the arrival of new pulses. This limitation makes PZC unsuitable for high pile-up environments and, notably, it had not

been applied in streaming mode. In this work, we present the application of the PZC method in streaming mode, alongside an adaptive control mechanism for the internal state variables, preventing baseline divergence and enabling its use in high pile-up scenarios.

This work addresses undesirable drawbacks in a high-event-rate high-energy calorimeter system, namely baseline shift and signal pile-up conditions. To this end, it proposes a hybrid approach that combines analog processing for the initial adjustment of pulse amplitude and duration, as well as noise treatment, with digital processing implemented on an FPGA to enable streaming operation. The implementation of the digital PZC method in streaming mode is innovative, as PZC is typically unsuitable for such applications. However, with the proposed control system, it becomes applicable. Additionally, the combination of unfolding and PZC in streaming mode represents a novel contribution of this work.

As a proof of concept, the Monte Carlo simulation by Lorenzetti [19] is employed to model a scintillator detector with approximately 10,000 channels. The system operates under varying event rates to evaluate the performance of the readout channels in simulated experimental conditions. This evaluation primarily focuses on the acquisition system's ability to handle pile-up and undershooting at high event rates. These conditions are particularly relevant for experiments such as the IceCube Neutrino Observatory [20], ATLAS [21], and CMS [22] at the HL-LHC and FCC [23]. Other notable examples include the Compressed Baryonic Matter (CBM) experiment at the Facility for Antiproton and Ion Research (FAIR) [24], Hyper-Kamiokande [25], and similar studies.

The simulated readout setup consists of a scintillator optically coupled to a SiPM, with the resulting pulses processed by a CSP and a CR-4RC shaper circuit. While effective, this configuration introduces additional challenges in pulse analysis due to the modifications imposed by the signal processing stage. These challenges have motivated the development and application of the unfolding method, which will be detailed in the subsequent sections.

This paper is structured as follows. The next section describes the proposed signal processing strategies to mitigate the signal baseline shift as well as pile-up. The data set and performance evaluation metrics are also presented in the next section. Section 3 shows the evaluation of the proposed algorithms, while Section 4 discusses the performance achieved compared to other approaches. Finally, Section 5 concludes this paper, highlighting the final remarks.

2. Materials and Methods

This section describes the environment and methodology employed to generate the data sets and depicts the proposed signal processing strategies used for performance evaluation.

2.1. Detector Simulation

A stand-alone tool, part of the Lorenzetti Simulator [19], was utilized to generate the energy deposits within a generic calorimeter [26] readout system. The Lorenzetti Simulator is a versatile framework designed to support novel signal reconstruction and triggering strategies, and it was specifically employed to produce the simulated samples used in this study. The Lorenzetti engine facilitates developments at the signal processing chain level, enabling the assessment of advanced signal processing approaches for modern calorimetry and triggering systems. For event generation, Lorenzetti integrates Pythia 8 [27], while event propagation is handled by Geant4 [28–30], a widely adopted framework in fields such as high-energy physics, nuclear physics, accelerator physics, medical science, and space science. Geant4 serves as a primary tool for simulating particle interactions with matter using Monte Carlo methods [30].

2.1.1. Data Events Generation

In this work, 2,000,000 sequential particle collisions were simulated for different event-rate conditions. The event rate, measured in events per unit time, is a critical parameter in detector systems as it reflects the frequency at which interactions or signals are generated.

The considered events rates conditions ranges from 1% to 70%, representing a wide spectrum from very low to relatively high interaction frequencies. The specific intervals were chosen to provide a comprehensive analysis of system performance across different regimes. Lower rates (1% to 10%) allow the system to be tested in conditions where pulses are well separated, ensuring minimal pile-up and baseline interference. High rates (20% to 70%) simulate high-frequency conditions where pile-up and baseline shift become significant challenges, stressing the limits of the readout and signal processing system.

The event rates were selected to align with a natural logarithmic scale (1%, 2%, 3%, 5%, 7%, 10%, 20%, 30%, 50%, 70%), which is particularly useful for systems where performance spans several orders of magnitude and ensures uniform representation across the range, avoiding excessive clustering of values in one region. This approach also provides sensitivity to changes in lower rates, where small variations can have a significant impact on performance, while efficiently analyzing higher rates with fewer points. The analysis captures system behavior across the desired range without requiring an excessively dense sampling while focusing on regions of interest, particularly those where event rates introduce significant challenges in terms of pile-up and baseline stability.

2.1.2. Convolutional Model

In this work, we present the modeling of a detection system based on a scintillator detector with SiPMs, where the system input is modeled as a radiation pulse, and the equivalent electronic circuit consists of a CSP followed by a PSC based on a CR-4RC filter. The goal is to analyze the system's response to these signals and study the characteristics of the pulse after particle interaction with the SiPM, as well as its electronic conversion and processing.

a. Input Electrical Pulse

The pulse modeling first considers the system input as an impulse generated by the particle interaction with the scintillator material, which is converted into an electrical signal by the SiPM. Scintillator detectors produce a temporal light response when particles interact with the material. This response is characterized by a rapid rise in light intensity, followed by an exponential decay due to the scintillation process [31–33]. The capacitive properties of SiPMs further shape the signal through charge accumulation and discharge, which can also be described by exponential functions [34,35]. As a result, the sensor output can be accurately modeled using a multi-exponential function that captures the light pulse's rise and decay phases along with the associated electrical processes [36]. For practical purposes, however, the electrical pulse is approximated by a bi-exponential function, presented in the following equation:

$$i_s(t) = I_0\left(e^{-t/\tau_D} - e^{-t/\tau_R}\right) \tag{1}$$

where I_0 is the incident intensity, τ_D is the decay time of the pulse, and τ_R is the rise time of the pulse.

It is represented in the Laplace domain by

$$I_s(s) = \frac{I_0\tau_D}{\tau_D s + 1} + \frac{I_0\tau_R}{\tau_R s + 1} \tag{2}$$

where, s is the complex frequency in Laplace domain.

b. Charge-Sensitive Preamplifier

The signal generated by the SiPM is then amplified by a CSP, presented in Figure 4, whose role is to convert the accumulated charge into a voltage $v_c(t)$. Its peak amplitude is proportional to the number of detected photons and preserves the energy information deposited in the detector [37,38]. Calculating the CSP transfer function $H_{CSP}(s)$, presented in Equation (3), is essential to model the circuit's response to an input current $I_s(s)$, enabling precise reconstruction of the output signal and ensuring accurate energy measurements.

$$H_{CSP}(s) = -\frac{R_f C_d s}{R_f C_f s + 1} \tag{3}$$

where C_d is the SiPM terminal capacitance, C_f is the integral capacitance, and R_f is the discharge resistance, which defines the accumulation time constant as $\tau_f = R_f C_f$.

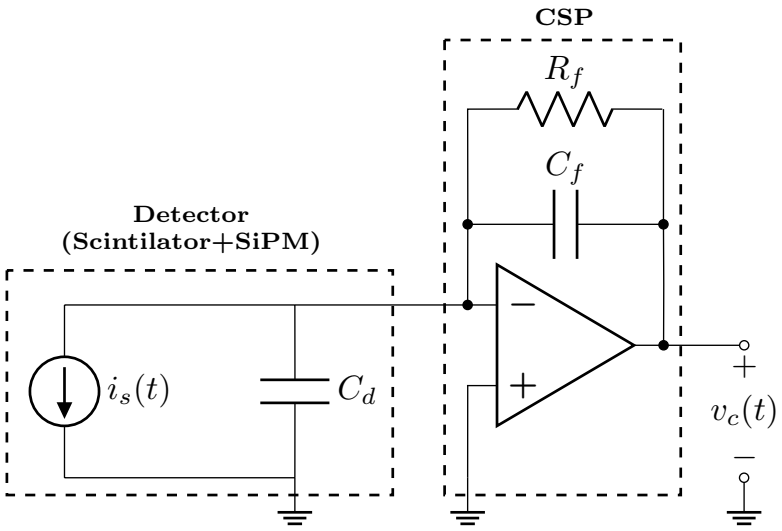

Figure 4. Charge-sensitive preamplifier circuit coupled to SiPM.

c. Pulse Shaper Circuit

Next, the amplified signal passes through a PSC. Regardless of the implementation, noise treatment through PSCs is a well-established topic that is extensively addressed in the literature [1,6,10,39,40]. For instance, optimal pulse shaping in semiconductor detectors under various noise conditions has been widely explored, demonstrating robust methodologies in this field.

A reference study highlights the importance of understanding the purpose of pulse shaping in relation to specific measurement objectives [1]. In this context, the pulse shape refers to the mathematical function describing the waveform of the pulse, while the term "pulse" denotes the individual instance generated by the shaping system.

The semi–Gaussian shaper is a widely used design with many advantages, including simplicity in construction. It is typically implemented using CR-nRC circuits, where n commonly ranges from 1 to 4 [5,10,41,42]. Yet, some studies have extended this configuration to higher orders [7,11]. Active PSCs are also frequently employed, with configurations such as Sallen–Key filters providing enhanced flexibility and performance. Beyond analog implementations, digital pulse shaping circuits have garnered significant attention for their adaptability and precision, making them an attractive alternative in modern detection systems [5–7,10,42–45].

In this work, the PSC is modeled as a CR-4RC filter. The initial CR stage acts as a high-pass filter, removing low-frequency components and improving the temporal response by enabling faster signal transitions. The subsequent RC stages form a low-pass filter, atten-

uating high-frequency noise and smoothing rapid transients. The CR-4RC configuration was chosen to ensure that the pulse width is adequate for the sampling rate, as illustrated in Figure 5.

In addition to the number of integrator stages, selecting an appropriate time constant ($\tau = RC$) is crucial for the proper operation of the PSC. The transfer function of the proposed circuit is presented in the following equation:

$$H_{PSC}(s) = \frac{CRs}{(CR)^5 s^5 + 9(CR)^4 s^4 + 28(CR)^3 s^3 + 35(CR)^2 s^2 + 15CRs + 1} \quad (4)$$

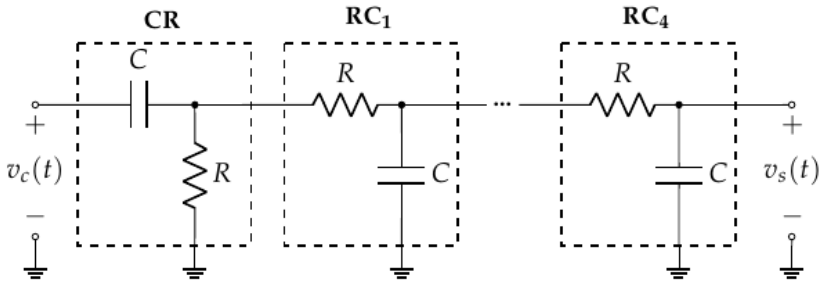

Figure 5. Pulse shaper circuit.

d. Noise Modeling

Noise analysis is crucial for understanding the performance of electronic circuits and sensors. In this analysis, we focus on the circuit assembled in the previous session, which includes the electronic equivalent of the detector, the CSP, and the PSC. While the physical response of the detector and SiPM is primarily measured in terms of the deposited charge, electronic circuits typically use voltage and current as key quantities. Therefore, we will examine the noise contributions from the perspective of these electrical quantities and assess their impact on the impulse response of the system.

The primary type of noise to consider in this case is the thermal noise, which arises due to the random thermal agitation of charge carriers in conductors, resistors, and semiconductor materials. This kind of noise is characterized by a broadband spectrum (Δf) with zero mean and a flat power spectrum density given by the following expression [37]:

$$E_{thermal}(\omega) = \sqrt{4k_B TR\Delta f} = N_{wn} \quad (5)$$

where k_B is the Boltzmann constant, T is the absolute temperature, and R is the resistance of the material or component. For this expression, we can consider this noise as ideal white noise, assuming that the bandwidth Δf is sufficiently wide to encompass the noise contribution across all the relevant frequencies of our circuit. The noise power then is expressed as N_{wn}^2.

In this case, the noise originates from the internal resistances of the circuit, including those arising from the coupling between the detector and the CSP, as well as between the CSP and the PSC. These resistances encompass the sensor electrode resistance, the wiring or PCB traces, and the parasitic resistances in the amplifier transistors.

The noise power associated with these factors is represented by N_{CSP}^2 and N_{PSC}^2, which correspond to the noise at the input of the preamplifier and shaper, respectively.

To evaluate the impact of the preamplifier noise on pulse compensation algorithms, we must pass it through the system and analyze the resulting frequency response. This requires considering the filtering effects of both the CSP and PSC stages. The CSP exhibits a broad frequency spectrum with a low-pass characteristic, while the CR-4RC PSC acts as a band-pass filter.

At lower frequencies, the CSP shows a flat response up to its cutoff frequency, beyond which the response rolls off, attenuating higher-frequency noise components. The shaper, due to its band-pass characteristics, further shapes the system's frequency response, suppressing both low and high frequencies while allowing a specific range of intermediate frequencies to pass.

As shown in the normalized magnitude plot (with a gain of 1 in the passband) in Figure 6, the shaper's passband is largely contained within the preamplifier's frequency response. Therefore, we can approximate the noise at the output of the preamplifier as white noise, with a standard deviation determined by the combined effect of the preamplifier input noise contributions.

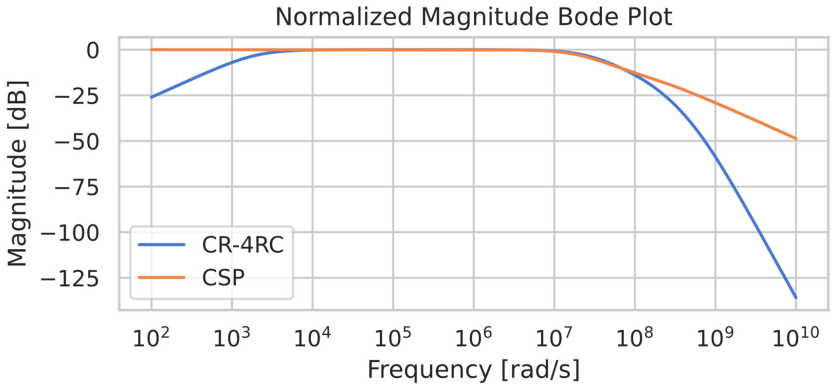

Figure 6. Normalized frequency response of the CSP and shaper circuits.

The output noise power spectrum density $N_s(\omega)$ at the output of the shaper can then be modeled as

$$N_s(\omega) = H_{PSC}(\omega)[N_{PSC} + H_{CSP}(\omega)N_{CSP}]. \quad (6)$$

In addition to the previously discussed noise sources, $\frac{1}{f}$ flicker noise (low-frequency noise) can play a significant role, especially in high-precision amplifiers commonly used in nuclear instrumentation circuits. This type of noise becomes more prominent at lower frequencies and can degrade system performance, particularly in applications requiring the detection of weak signals.

Current noise, which arises from fluctuations in current across various components and parasitic resistances, is another important factor. For example, variability in the avalanche currents of the SiPM's photodetector pixels can introduce additional disturbances, further affecting the signal quality and measurement accuracy.

Although $\frac{1}{f}$ flicker noise and current noise are important, particularly in nuclear instrumentation circuits, they were not included in the current analysis. This choice was made to prioritize the primary noise sources that most significantly affect the system's performance within the scope of this study.

2.2. Digital Processing

The events measured by the detector, after analog processing in the readout chain, are digitized with a sampling period T_s, enabling the implementation of digital signal processing techniques. One such technique is the proposed deconvolution of the waveform using the unfolding method for modal components [13,46]. This approach optimizes the pulse shape and mitigates pile-up effects, particularly in high-rate detection systems. The method focuses on converting the dominant exponential components of the waveform into impulses or, when this is not feasible, into step functions. This transformation preserves the amplitude of the original waveform while reducing the pulse width, thereby enhancing temporal resolution.

2.2.1. Unfolding Algorithm

The first step is to apply the unfolding algorithm to exponential components of the waveform. By deconvolving the exponential decay, the resulting signal is converted into a digital impulse, as proposed by Jordanov [14] and applied by Zeng [15], if all dominant component was removed, maintaining the original amplitude but with a reduced temporal width. This process significantly mitigates the pile-up effects in high-rate environments.

Mathematically, this is achieved by considering that a discrete exponential signal $u[n]$, with a sampling period T_s and a decay rate τ_1, can be represented in the recursive form:

$$u[n] = \begin{cases} bu[n-1], & n \geq 0 \\ 0, & n < 0 \end{cases} \tag{7}$$

where n is the sample number that is renationalized with the time $t = nT_s$ and the parameter $b = e^{-T_s/\tau_1}$.

By subtracting the estimated sample from the actual sample, as shown in Equation (7), all terms for $n \neq 0$ are canceled, while for the sample at $n = 0$, the resulting value is $v[0] = u[0] - bu[-1] = e^0 - 0 = 1$. This effectively recovers the unit impulse function $\delta[n]$ [47].

$$v[n] = u[n] - bu[n-1] \tag{8}$$

where $u[n]$ represents the input signal and $v[n]$ the output signal with component remotion.

The procedure is illustrated in Figure 7, and its unitary impulse response is presented in Figure 8.

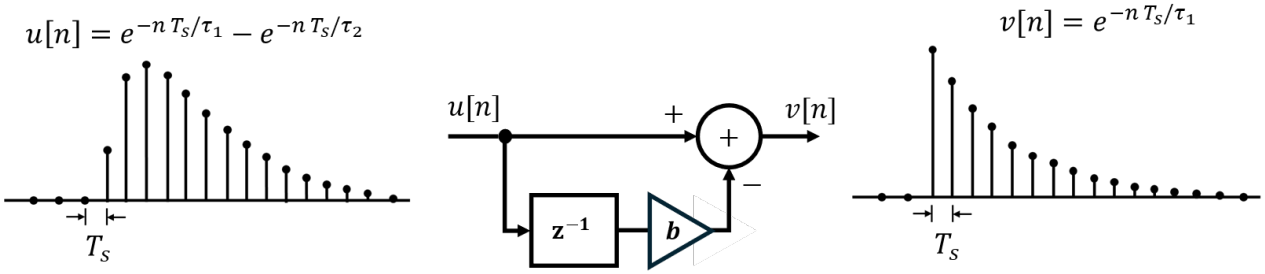

Figure 7. Unfolding algorithm.

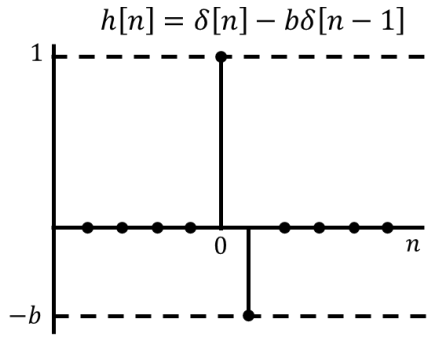

Figure 8. Unfolding impulse response.

2.2.2. Pole-Zero Cancellation

In the presence of a zero in the circuit's dynamic response, the unfolding method becomes ineffective at removing one of the PSC poles due to the system being non-minimum phase. Consequently, an undershoot appears in the poles influenced by the zero, indicating the effect of a zero near the pole.

The distortion is introduced by the CR high-pass filter stage [46] when the parallel resistor is omitted. During a detector event, this causes a shift in the signal's average level. Due to the capacitive coupling in the CR stage, which discharges slowly, this shift results in a displacement of the signal baseline, manifested as a negative component in the output. This negative component compensates for the increase in the signal's average level caused by the event. When the detector's signal undergoes a sudden change, such as during an event, the capacitors in the coupling network attempt to preserve the original voltage difference by generating a reverse polarity signal.

As the event rate increases, the cumulative effect of these shifts becomes more pronounced, resulting in a growing (falling) average signal level. This leads to an increase (decrease) in the baseline shift, which can have a significant impact on both the detection accuracy and the estimation of subsequent signal amplitudes. If left uncorrected, this distortion can lead to erroneous signal measurements, especially when the event rate is high.

Applying the unfolding method to these poles results in a train of unit impulses with oscillatory responses, specifically two impulses of opposite polarities. This behavior arises from the incomplete causality of the filter and follows the unitary impulse response, as presented in Figure 8.

To mitigate this issue, the proposed solution integrates the response pulse of the unfolding algorithm using an accumulator. This results in a step-like function in the system's output [16], with an amplitude gain of $1 - a$, which is lower than the original baseline shift, as presented in Figure 9.

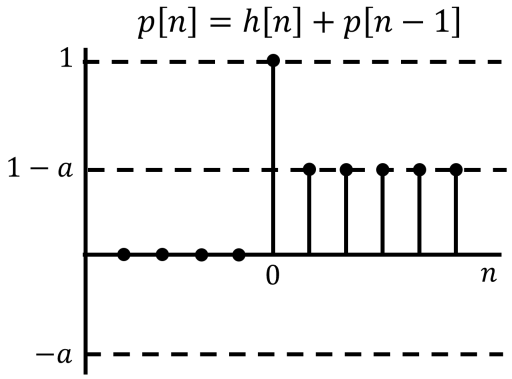

Figure 9. Accumulated unfolding impulse response.

The compensation is achieved by applying the recursive formula:

$$r[n] = v[n] - av[n-1] + r[n-1] \tag{9}$$

where $v[n]$ represents the input signal (with distortion), $r[n]$ is the output signal after compensation, and $a = e^{-T_S/\tau_u}$ is a constant that depends on the exponential decay τ_u.

It is important to note that the baseline shift component is typically negative, which represents the ideal case to minimize confusion between the signal and the baseline. When this is not the case, modifications should be made to achieve this ideal condition.

Another procedure is necessary to compensate for the accumulation of step effects. A constant removal of the step influence is proposed in the implementation, as will be discussed in Section 2.3.2.

2.3. Hardware Implementation

The digital filter requires a hardware fast enough to process the data at the determined frequency rate. The field-programmable gate array (FPGA) was chosen because it has the

possibility to run the filtering process in real time, with high frequencies, and it is largely used at online signal processing environments.

Most of FPGA chips work with a fixed point, which means that the hardware does not do floating points operations natively. Two strategies can be traced to avoid this issue: the first one corresponds to adopting floating point operations via emulation; the second one makes use of the numeric Q notation, which represents the integer and fraction part of the numbers. Both strategies present advantages and disadvantages. For example, the former tends to use the more logic elements but achieves more accurate operations, while the latter normally uses less resources but may introduce approximation errors.

The FPGA chosen for the development is the DE2-115 Kit, manufactured by Terasic (Hsinchu County, Taiwan), which uses an Intel FPGA chip. The board features a Cyclone IV EP4CE115 device with 114,480 logic elements and includes peripherals such as GPIO, keys, switches, and others. As a low-end FPGA, it ensures that if the application runs correctly on this architecture, it will also perform well on high-end boards.

The development of the filtering and amplitude estimation for a real-time processing is described below, using the Q notation numbers.

2.3.1. PZC Implementation

The PZC for the hardware processing is performed using Equations (10) and (11). The two following equations are equivalent to Equation (9). However, here, for hardware implementation, the output signal is not normalized [46].

$$p[n] = v[n] + p[n-1], \tag{10}$$

$$r[n] = M.v[n] + p[n] \tag{11}$$

where v is the input signal of the PZC, and M is the factor defined by $(e^{T_{CLK}/\tau} - 1)^{-1}$. T_{CLK} is the clock period of the system, and τ is the time constant of the exponential decay. The factor M is usually a fixed number much greater than 10, which avoids the scaling of this number. The a factor and the M factor relation is $M = \frac{1}{a-1}$, and the output signal $r[n]$ has the original input amplitude multiplied by $(M + 1)$.

Equation (10) describes an accumulator that is incrementing its value with the actual input reading. At FPGA, this is a register receiving, at each clock border, the adding result of its own value with the actual input signal. This work proposes to include a subtracting signal to the accumulator, known here as accumulator correction (AC), to prevent some diverging results after a long processing time. This step is detailed in the next subsection.

The PZC signal is the product between the M factor and the previous accumulator. This operation can be completed with a continuous assignment approach, since the input data and the register are synchronized with the clock system. This M factor can be expressed as a parameter inside the block and is different for every pulse shape application that needs to be filtered.

For this project, the input data use the Q12.0 representation with 12 bits. The M factor was set to 2000, according the sample period (T_{CLK}) of 25 ns, resulting in output data with 28 bits in the Q28.0 format to accommodate the multiplication and sum operations involved in the implementation.

Figure 10 is a block diagram that describes the PZC operations at the FPGA.

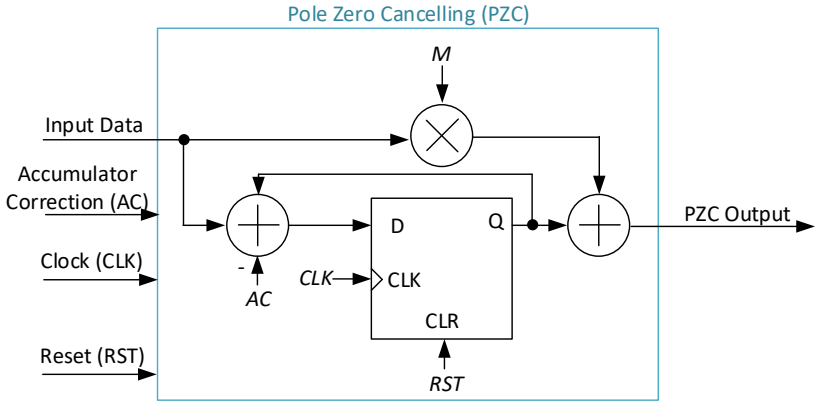

Figure 10. Block diagram of the PZC at FPGA.

2.3.2. Accumulator Correction (AC)

The unfolding filter, when applied to an exponential undershooting component, produces a bipolar response that compromises the filtering process. This issue is addressed by combining the unfolding filter with an accumulator, which defines the PZC algorithm. Figure 11 shows a sequence of three exponential signals as occurs in a streaming process and the respective PZC response. The unfolding filter carries the previous processed amplitudes' information and it can diverge the baseline with a high rate of events.

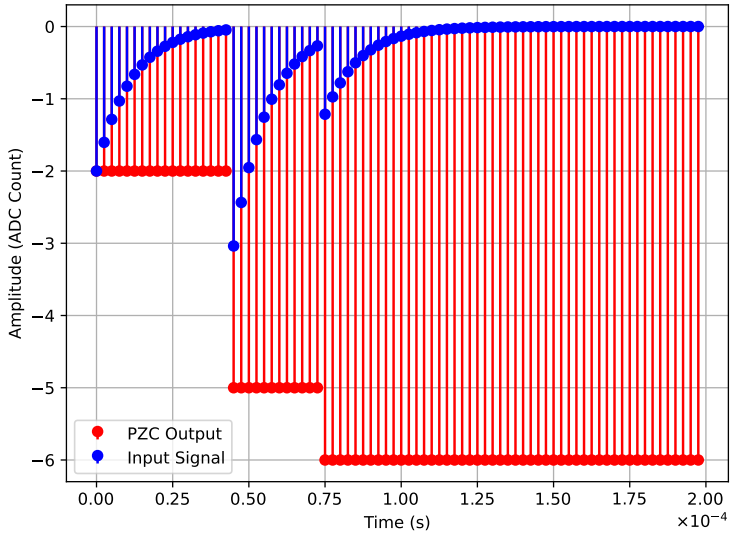

Figure 11. PZC output for a sequence of exponentials.

The negative exponential component of the signal may have a low amplitude when compared to the other components, and the described issue can be significant after several processing signals. The accumulator of the unfolding filter has to be cleaned with the remnant response of processed exponential components, leading to a feedback approach. The problem is that the negative exponential can take significant time to be ceased. This is not good for a high frequency rate of events because the amount of previously processed samples that must be saved will spend unnecessary resources.

The chosen strategy involves analyzing a defined number of PZC output negative samples, calculating the mean of the negative values within this window and subtracting it from the PZC accumulator. The system verifies the PZC output. If the baseline decreases, this is due to the residual accumulator values affecting it. Therefore, the mean of the negative values correct the baseline divergence with a simple and light method of accumulator adjustment. As explained before, the accumulator problem will be relevant after some

processing signals. If this adjustment is performed at certain samples, it will be enough prevent issues.

This compensation is applied only when the number of negative values reaches the defined window size. Once the subtraction process is completed, the next correction is only performed after processing the next set of new samples. In other words, the compensation is not applied at every clock cycle. The process is detailed in Equation (12).

$$p[n] = p[n] - \frac{1}{W} \sum_{0}^{W-1} q[i], \text{ with } \mathbf{q} = (\mathbf{r} < 0) \tag{12}$$

where r is the output signal of the PZC, p is the PZC accumulator, W is the window size for analysis, and q is the vector that stores the last W negative values of r.

For the FPGA implementation, two additional registers are utilized. The first register counts the total number of negative processed samples, and the second stores the sum of these negative values. The logic checks whether the PZC output is negative. If this condition is met, the first counter is incremented, and the sample value is added to the second register.

When the first counter reaches the defined window size, the PZC accumulator is adjusted by subtracting the ratio of the sum of negative values (stored in the second register) to the window size. After this operation, the counter and the register holding the sum of negative values are reset, allowing the process to restart for the next set of samples. It is wise to choose the window size as a power of two because division can be performed by bit shifting, which saves hardware resources and increases the maximum clock frequency. In the implementation, the window size value was 2^4.

Figure 12 presents a block diagram illustrating the accumulator correction process in the FPGA. To clarify the interaction between the PZC and AC blocks, a block diagram is shown in Figure 13.

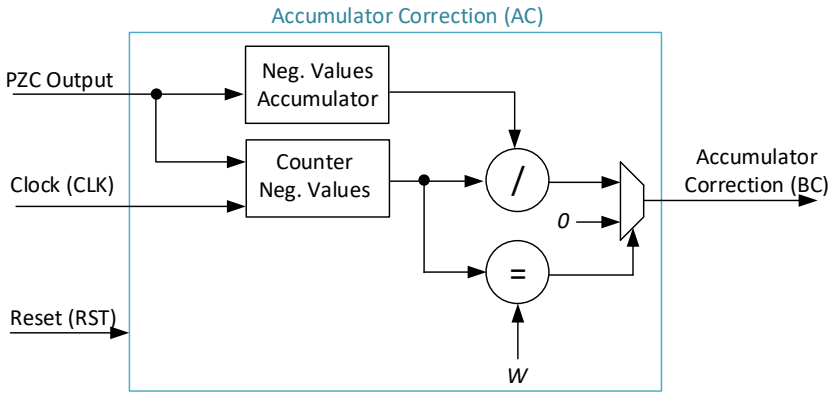

Figure 12. Block diagram of the AC at FPGA .

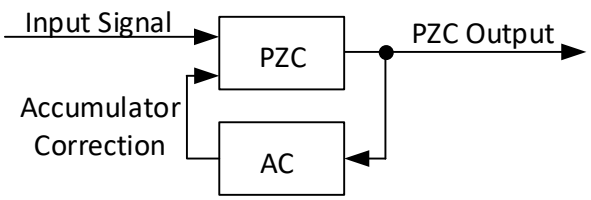

Figure 13. Relation between AC and PZC at FPGA .

Both the input and output data use the Q28.0 format. This format is defined to align with the PZC output and the accumulator. To evaluate the maximum operating frequency of the techniques, PZC implementation and accumulator correction were tested together. The system operates at up to 83 MHz of the clock frequency and utilizes 222 logic elements.

2.3.3. Unfolding Filter

The unfolding filter represents the next step in the implementation. It uses the PZC output to identify the impulse response that reflects the particle's energy, focusing solely on canceling stable poles. This approach effectively isolates zeros in the transfer function, allowing the filter to operate as a finite impulse response (FIR) difference filter [48].

The FIR filter performs the deconvolution process. It is a simple method to be implemented in an online environment, specially at FPGA. First, the weights are defined according the filter order, and the values are predefined to match with the application. Again, as the filter weights might be a float point number, its common to scale theses values. This paper uses the scaling that affects the final results less, obtaining similar results when compared to the same exact weight float point values.

After defining the weights, the input samples are delayed, following the filter order to match the related weight of that sample. The final result of the FIR filter is given by the sum of multiplication products between the delayed samples and the corresponding weight.

In the proposed application, there are two consecutive FIR filters, one for each signal component filtering. The structures of both of them are the same, with an order of two. With the FIR filter processes being completed, the expected output is impulsive energy. Figure 14 represents the block diagram of the FIR filter implementation.

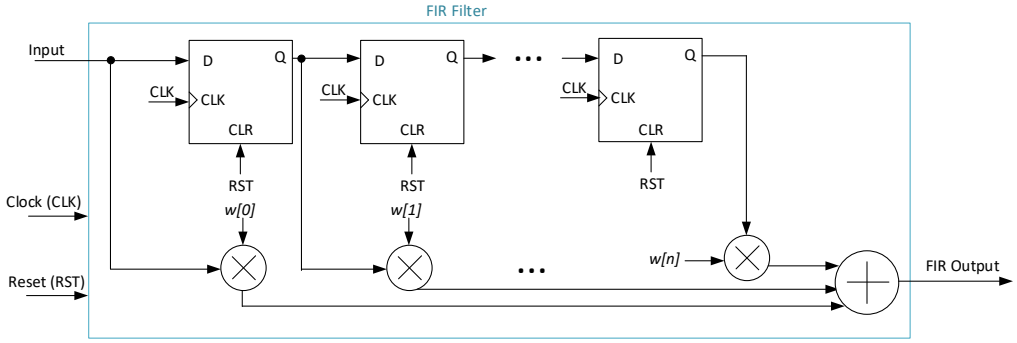

Figure 14. Block diagram of the FIR filter at FPGA .

The filter weights have values between 0 and 1. These values were scaled by a factor of 2^{10} before rounding, using the Q1.9 representation. The first unfolding filter processes input data with 28 bits in the Q28.0 format, matching the PZC output. The second unfolding filter uses input data with 39 bits (Q30.9) and produces output data with 50 bits (Q32.18). These filters require 101 and 157 logic elements, respectively, to perform their tasks.

When evaluating the complete unfolding process, including the PZC operation, the system achieves a maximum operating frequency of 58 MHz. It utilizes 480 logic elements, which represents 0.42% of the total logic elements available on the chosen board.

3. Results

To evaluate the performance of the proposed signal processing approach, system parameters were carefully defined, and simulations were conducted under realistic operating conditions. The system's time constants were used to calculate filter coefficients, aligning the processing stages with the pulse dynamics of the readout chain. The dominant poles of the system, responsible for shaping the waveform, were addressed using the unfolding algorithm. Meanwhile, poles near marginal stability were handled with the PZC approach to ensure proper baseline correction.

The results include the waveforms generated by MATLAB version R2022b simulations at different stages of the readout chain, along with metrics such as baseline shift (BL) and pile-up level (PL), both before and after applying the proposed algorithms. The

performance of the algorithms is verified through FPGA implementations to validate the effectiveness of the proposed methods.

3.1. Readout Waveform

The design performance of the CSP and the PSC is directly influenced by their design parameters, particularly the time constants chosen for each stage. These time constants are critical for balancing pulse width, noise reduction, and temporal resolution, ensuring that the output signal meets the requirements of high-rate detection systems.

The response obtained from the CSP combines the contributions from the scintillator, SiPM, and preamplifier. The time constants chosen for the scintillator and SiPM were based on values from previous studies [3,33], where the rise time is $\tau_r = 1$ ns, and the decay time is $\tau_d = 5$ ns, and the SiPM capacitance is defined as 1 pF. The time constant for the CSP was set to $\tau_f = 510$ ns [5,43].

Similarly, the time constant for the PSC was also defined, being the same for the differentiator stage and the integrator stages ($\tau = \tau_{CR} = \tau_{RC}$), with a value of $\tau = 5$ µs.

It is worth noting that the chosen digitization period was $T_s = 25$ ns, which was one of the primary factors influencing the definition of the time constants in the shaper circuit, ensuring proper digitization.

Figure 15 illustrates the impulse response of the CSP and PSC stages separately, highlighting the contribution of each component according to the selected time constants. In the bottom plot, the broadening effect induced by the semi–Gaussian shaper is evident. This broadens the results from the low-pass filtering characteristics of the shaper, which attenuates high-frequency noise while widening the pulse. This pulse widening enhances the signal-to-noise ratio (SNR) and ensures that the full charge is collected and accurately measured.

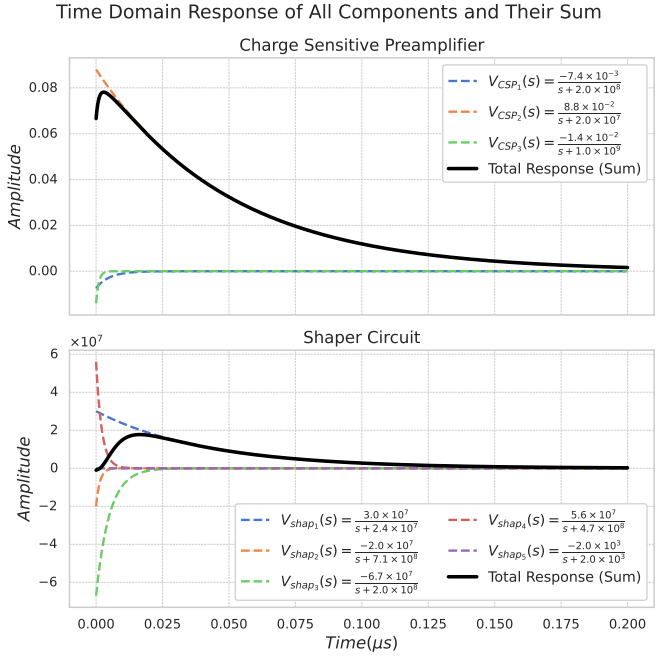

Figure 15. Impulse responses for each component of the CSP and PSC stages. Individual curves show the responses of each individual component, and the bold black line represents the summed total response over time.

Finally, Figure 16 presents the effect of the combined CSP and PSC systems on the overall pulse. The plot clearly reveals a significant long-tail component in the pulse's

response, with a decay time that is approximately three orders of magnitude longer than both the rise and decay times of the initial signal.

The poles and zeros of the acquisition system, along with their associated time constants, are shown in Figure 17. The inset highlights the dominant poles and a pole nearing instability.

The proposed approach involves canceling the two dominant poles using the unfolding method and addressing the marginally stable pole with the PZC algorithm.

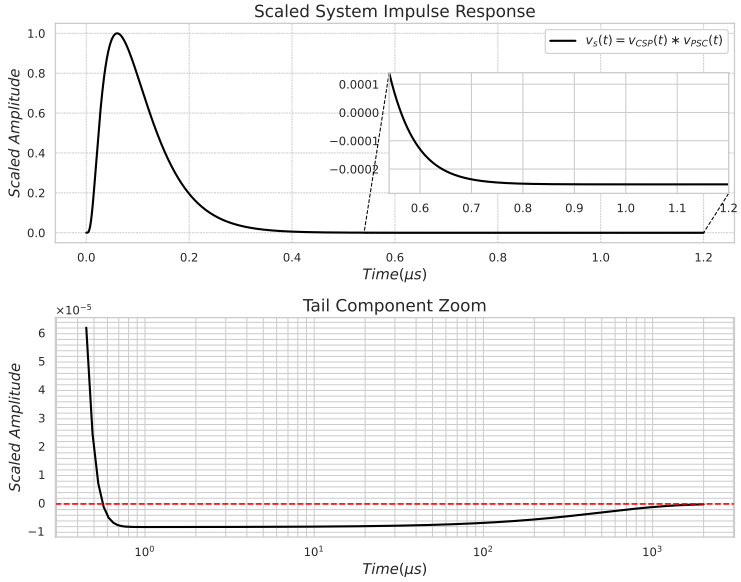

Figure 16. Impulse response of CSP and PSC stages combined. The top graph shows the response over the μs range, with a detailed zoom on the descending part following the peak value. The bottom graph provides a focused view of the tail component, emphasizing its prolonged behavior to highlight the long-term decay characteristics.

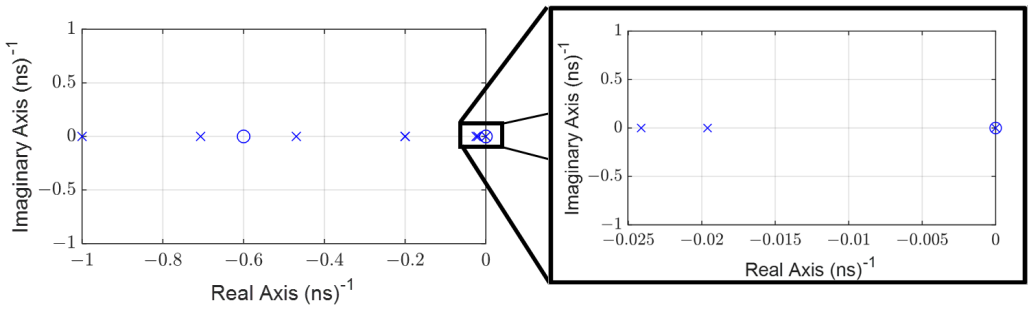

Figure 17. Pole-zero map displaying the distribution of poles (marked with '×') and zeros (marked with '○'). An inset zooms into a region near the origin for a detailed view of closely placed zeros and poles.

3.2. Evaluation Metrics

The pile-up level quantification is an important metric used to evaluate the performance of detectors. pile-up is a random effect where events follow a Poisson time distribution, influenced by the event rate (λ) and the pulse width (Δt). According to Campbell's theorem [49], the probability of N pulses occurring within a time interval equal to the pulse width is given by the following equation:

$$P(N, \lambda, \Delta t) = \frac{(\lambda \Delta t)^N}{N!} e^{-\lambda \Delta t} \tag{13}$$

Here, in order to define a pile-up level (PL) metric that is independent of the number of overlapping events, the complement of the probabilities of exactly one event and zero events

occurring within the interval is calculated. This approach quantifies the probability of pile-up, involving two or more events within the same interval. Consequently, the PL is given by

$$PL(\lambda, \Delta t) = 1 - (1 + \lambda \Delta t)e^{-\lambda \Delta t} \tag{14}$$

Similarly, it is necessary to quantify the baseline shift level (BL) of the pulse. In this case, the proposed approach is to calculate the average of the negative signal, as given by the equation, since in the context of energy detection from particle interactions, only non-negative values are expected. Therefore, any baseline shift or other alterations to the signal result in negative values [50].

$$BL(\lambda, \tau_{neg}) = mean(q[n] < 0) \tag{15}$$

where $q[n]$ is a representation of τ_{neg}, which is the time constant from the negative component that generates the undershooting.

3.3. Algorithm Verification in Hardware Implementation

The verification of the algorithms was carried out on their hardware implementation on an FPGA. The primary focus of this step is to validate the effectiveness of the unfolding and PZC algorithms under streaming processing conditions.

The baseline shift, measured by the BL, introduced by the capacitive coupling in the readout chain was initially quantified for the simulated signal. After applying the PZC algorithm, the baseline was effectively restored, as indicated by a significant reduction in the BL metric. It approached the ideal baseline level, when compared to the BL befor the PZC, as presented in Figure 18.

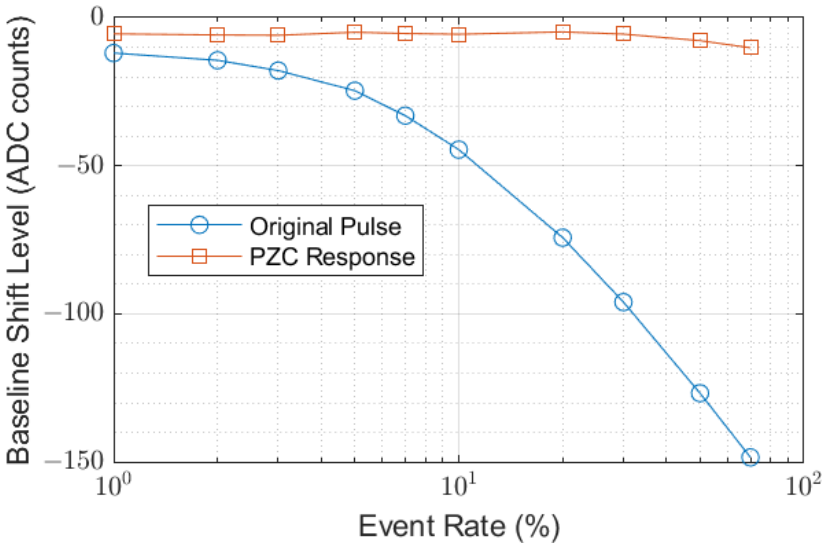

Figure 18. Baseline shift level as a function of the event rate.

The unfolding algorithm's performance is assessed by comparing the PL before and after processing, demonstrating its ability to mitigate pulse overlap, as presented in Figure 19.

pile-up and baseline shift become more pronounced at higher event rates. Nevertheless, the unfolding algorithm effectively mitigated pile-up, while the PZC algorithm efficiently compensated for the baseline shift.

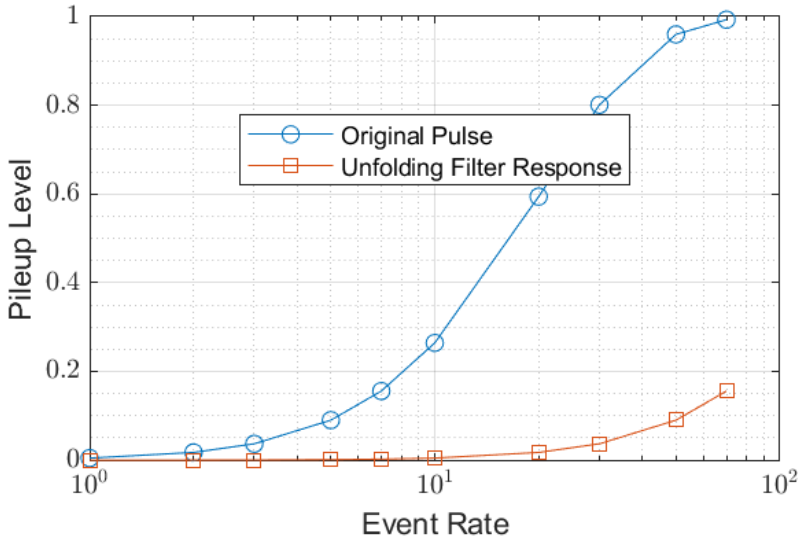

Figure 19. Pile-up level as a function of the event rate.

4. Discussion

The implementation of the PZC algorithm significantly reduced the baseline shift, lowering it from −40 ADC units at high event rate levels to approximately −10 ADC units. This residual shift closely approaches the baseline observed lower than 10% of the event rate and remains only slightly above the noise standard deviation of 5 ADC units. This demonstrates the algorithm's effectiveness in mitigating the baseline shift across the full range of event rates (1% to 70% of the event rate). Moreover, the PZC algorithm enhanced the system's performance by improving the signal-to-noise ratio, thereby increasing the detection accuracy and refining the charge collection resolution.

Furthermore, the application of the unfolding filter effectively addressed pile-up artifacts. For event rates up to 10–20%, the filter reduced the pile-up probability to nearly 0%, compared to an unprocessed pulse that exhibited a pile-up probability of approximately 30%. Even at higher event rates, up to 30% of the event rate, while the pile-up probability for unfiltered pulses approached 100%, the unfolding filter maintained the pile-up probability below 20%. This performance underscores the robustness of the unfolding filter in preserving signal integrity across a broad spectrum of operational conditions.

The PL metric is suitable for measurement systems where the event rate is comparable to the duration of the measured pulses, serving as a valuable tool for system analysis and design. In contrast, the BL metric introduced in this work is intended for measurement or communication applications that incorporate a high-pass filter in signal conditioning, enabling both effective analysis and efficient design of signal processing systems.

The implementation of the digital PZC method in streaming mode is a significant innovation, as PZC is generally unsuitable for such applications. The proposed control system overcomes this limitation, making it applicable to high-pile-up environments. Furthermore, the combination of unfolding and PZC in streaming mode introduced in this work represents a novel contribution to the field.

Regarding the FPGA implementation, the unfolding process uses only 0.42% of the board's logic elements and can operate at up to 58 MHz clock frequency, greater than the 40 MHz sample frequency of the data test. The application is lightweight and fast, making it suitable for streaming data with a high rate of events and multiple cells.

The number of bits for each step and the filter weights must be carefully chosen. A low number of bits may lead to imprecise results, as less data are processed. Increasing the number of bits consumes more hardware resources, which should be avoided when

possible. Therefore, for each solution, the optimal bit size should be found to balance precision and resource usage.

The filtering clock frequency is sufficient to handle high event rates, such as those in particle colliders. For example, in the case of the LHC, the collision frequency is the same used 40 MHz, which is below the 58 MHz achievable by the implementation. The solution can also handle low event rates, as the limitation frequency refers to the maximum frequency, not the minimum. The attention need for others sampling periods is to adjust the M factor and unfolding weights to match with the new value. If not, the unfolding process will not work properly and will not fulfill the objective.

Additionally, the FPGA board tested is a low-end hardware. Since the final implementation works well in the described scenarios, high-end hardware was not tested, but it is expected to perform better due to having more resources.

A significant limitation associated with unfolding filters is the need to know the decay time of the exponential components of the signal. The filter weights are tuned based on these parameters, and if they are not accurately defined, the unfolding process may fail, leading to undesirable results.

The baseline shift correction method using the digital PZC with accumulator adjustment is particularly well suited for scenarios with high event rates and a significant baseline shift. This suitability arises from its tendency to overcompensate in cases where the event rate is below 10%. Another important limitation is the window size of accumulator correction. If the window is too long, the correction process may be delayed, causing the PZC to diverge.

5. Conclusions

Digital signal processing using online data streaming presents many challenges to digital circuit design. In particular, modern high-energy calorimeter systems operate at extremely high-event-rate conditions and must handle severe undesired effects, such as the signal pile-up and signal baseline shifts due to circuit shaper designs. These effects are not fully addressed in current strategies, leading to degraded performance from online optimal filtering techniques that recover signal parameters, such as amplitude, baseline and time [51,52]. This paper proposed a solution to be implemented in FPGA devices in order to mitigate both the signal pile-up and baseline shifts, considering the harsh conditions such as the ones imposed by the high-luminosity LHC program. The proposed algorithm presented promising results with respect to typical solutions, becoming a potential alternative to modern calorimeter systems.

The unfolding algorithm is a linear method that functions as a second-order FIR filter to recover impulse signals. The weight parameter is adjusted based on the decay time of the exponential component provided by the circuit shaper. Pole-zero cancellation (PZC) is a modification of the unfolding algorithm, incorporating an accumulator to filter out undesired long exponential components. This paper proposed a modification of PZC for use in streaming data, utilizing accumulator correction (AC) to average the negative values of the PZC output.

The unfolding algorithm and the modified PZC were implemented on an FPGA using the DE2-115 Terasic Board, which can operate at up to 58 MHz while using only 0.42% of the board's logic elements. The PZC algorithm significantly reduced baseline shifts, decreasing approximately 75% of ADC units at high-event-rate levels. The unfolding filter effectively reduced the pile-up probability to nearly 0% for low event rates, maintaining around 20% for higher event rates.

The digital PZC method applied to stream signal processing, combined with the unfolding filter, is a notable innovation. This technique is feasible on low-end FPGA

hardware and can be applied in scenarios with high event rates. However, some of its disadvantages include the dependency on exponential decay time, overcorrection by the accumulator in scenarios where the event rate is below 10%, and the impact of the accumulator correction window size.

Regarding potential future works, considering the previously discussed limitation, improvements to the accumulator correction process can be explored using alternative approaches. Additionally, we also expect to assess the energy estimation efficiency using the proposed signal processing strategies, evaluating the improvements achieved in the final digital energy reconstruction step.

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Data Availability Statement: The original data presented in this study are openly available at https://cernbox.cern.ch/s/pcP0kY5VxB4gsZ5 (accessed on 15 December 2024).

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Conflicts of Interest: The authors declare no conflicts of interest.

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