A High-Speed Image Acquisition System Based on State Machine and Fast ADCs

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Abstract— **The present work reports on the development of a digital system for image acquisition which is able to process two electric signals of amplitude varying between 0 and 10 V. The system correlates both signals in a two-dimensional histogram. X and Y coordinates for every event are derived from the amplitudes of the two coincident signals. The hardware basically consists of two analog-to-digital converters (ADCs), control electronics, and one 1M Static Random Access Memory (SRAM), implemented in a card that is plugged into any personal computer with an ISA bus. The data acquisition rate may be as high as 1.0×10^6 events per second, and does not depend on the PC processor. The software code has been written in the Delphi environment using Assembly routines. Image sizes may be chosen from 128 x 128 to 1024×1024 pixels and may be viewed in three-dimensional graphics. Images are shown to illustrate the applicability to two-dimensional position sensitive X-ray detectors.**

Keywords— **X-ray detectors, image acquisition, analog-to-digital converter, programmable device, state machine.**

I. Introduction

PARTICLE detectors which use gas as the absorbing medium and wires as charge collection electrodes [1] are widely used in several applications, covering the range from simple counters up to large area two-dimensional position sensitive detectors. These kinds of applications require the use of electronics modules (pre-amplifiers, amplifiers & discriminators, external delay and TACs - time-to-amplitude converters) and a data acquisition system to acquire and visualize the data collected. For instance, in the case of one-dimensional position sensitive particle detectors, the coordinate of a photon's position is represented by a proportional voltage amplitude in the TAC output. Analog-to-digital conversion of the TAC output therefore provides the photon position information. The Two-Dimensional Data Acquisition System (TDAS) here presented performs the analog-to-digital conversion of two TAC outputs, corresponding to the X and Y coordinates of the event. The digital X and Y words are grouped to define one address on the memory address bus. The histogramming circuit accumulates events in specific memory positions over a period of time, thus constructing the resulting image. The present work proposes a new scheme for the TDAS which is based on the use of logic state machine, instead of a microprocessor, to control and process the digitized data. This design speeds up the acquisition rate of the TDAS, reducing circuit dead time. High-speed sampling ADCs, without pipeline delay, are used to digitize the input signals. Combining low conversion time with high-speed data processing, we achieve minimum dead time for this particular position readout technique.

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II. The position sensitive detector

The proposed image acquisition system was intended to be used with an X-ray gas position sensitive detector (PSD) to acquire two coordinates of the position of detected photons. The detector [2] uses a single electrode, the X&Y cathode, to sense the electric electric charge induced by ionization avalanches generated by the absorption of X-ray photons in a multiwire proportional counter (MWPC). Fig. 1 shows the scheme of a MWPC where one of the conducting planes is the detector window, while the other one is subdivided in discrete sampling elements, composing the X&Y cathode. The X&Y cathode is compacted to one multilayer printed circuit board and does not involve wires. Two-dimensional localization of photons is achieved by associating one delay line to each coordinate. The discrete cells of each delay line are properly connected by conducting strips to the corresponding sampling pads, so that the propagation time of electric pulses can be related to the avalanche position [3].

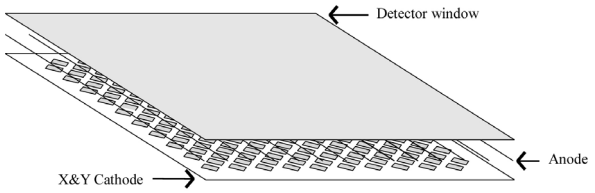

Fig. 1. Scheme for the MWPC with discrete cathode sampling elements.

III. Read-out electronics

Signals coming from the delay lines feature very small amplitude (typically $< 1mV$). A pre-amplifier is therefore required as the first stage in the read-out chain. In order to define a precise timing criterium, after pre-amplification signals are sent to the amplifier and discriminator modules. The simplest timing technique is based on the use of leading edge discriminators. It consists in providing a circuit which compares the signal amplitude to a pre-set value above the electronic noise. Whenever a photon is detected, the amplitude at the circuit input is higher than the pre-set value and a fast logic pulse is generated, indicating that a valid event has occurred. However, this timing technique

0-7803-7324-3/02/$17.00 © 2002 IEEE

incorporates some error depending on the input signal amplitude, since the preset comparation voltage is fixed while the signal amplitude varies. This error is compensated for by use of the so called constant fraction discriminators, in which the timing signal is emitted when the input signal reaches a given fraction of its maximum amplitude.

The information concerning the X&Y coordinates of an event is represented by the interval between the electric signals coming from both ends of each delay line. This interval is measured by the TACs. Each TAC converts the time delay between two logic pulses to a proportional amplitude pulse. Therefore, at the last analog stage of the read-out chain, two analog pulses corresponding to the X&Y coordinates of each photon absorbed at the detector are available for digitization.

IV. Two-dimensional data acquisition circuit

The complete detection system includes the detector itself, the read-out electronics, the digital circuitry for two-dimensional data acquisition and a software interface. A block diagram of the TDAS is shown in Fig. 2 and briefly described below.

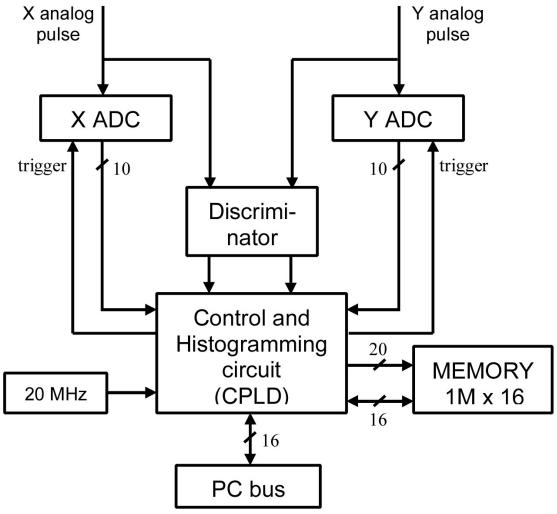

Fig. 2. Simplified block diagram of the digital circuit for image acquisition.

A. Analog-to-digital conversion

We have selected the AD1671KP converter, manufactured by Analog Devices, to digitize the analog input pulses. It is a monolithic 12-bit, 1.25 $MSPS$ analog-to-digital converter with an on-board, high performance sample-and-hold amplifier and voltage reference. The AD1671 uses a subranging flash conversion technique [4], implemented in a combination of high speed bipolar/CMOS process. A single pulse is used to initiate the conversion process, which is finished about 800 ns later, being indicated by an output single pulse. Besides of the high-speed conversion, the AD1671 presents another important feature for our design, it is a sampling converter (no pipeline delay is imposed), which is required for applications with random input signals. In order to improve the image quality we used only the ten most significant bits of the ADC, resulting in a reduced differential non-linearity of $\pm 0.5 LSB$, instead of $\pm 2.0 LSB$, specified for the converter. This approach was tested in an early design of a multichannel-analyzer and has proved its efficiency [5]. We have also designed a digital right shifter, which acts ont he memory bytes and allows one to decrease the image resolution down to 128×128 pixels, speeding up the counting rate per pixel and the image updating on the PC screen.

B. TDAS Discriminator

The two analog pulses coming from the TACs are sent to the ADCs and to a leading edge 2-channel discriminator. Its circuit includes fast comparators that perform noise rejection and pre-trigger action. When the analog input pulses exceed an adjusted threshold, digital pulses are generated at the output of the comparators, starting the ADCs trigger process. We have used the dual ultra-fast TTL comparator MAX912. It presents fast propagation delay of 10 ns, low supply current, and a wide common-mode input range, which, with a bit of signal conditioning, supply design demands.

C. Control and Histogramming circuit

All the control signals and the histogramming process are generated by digital logic implemented in two complex programmable logic devices (CPLDs) [6], which use a 20 MHz clock for timing. Each CPLD presents 7.5 ns pin-to-pin logic delays on all pins, containing 108 macrocells with 2400 usable gates. The following sections describe the main digital modules and their functions in the control and histogramming circuit.

C.1 Coincidence logic

Once there is a time coincidence between the two analog pulses coming from the TACs, a single trigger pulse is generated by a digital scheme and sent to the ADCs, indicating that a valid event occurred in the active window of the detector. The digital scheme for coincidence verification receives the outputs of the TDAS discriminator and provides a single trigger pulse to ADCs, if both edges of the inputs occur inside a 300 ns window. Besides the coincidence function, this circuit introduces a delay of 550 ± 50 ns between the inputs activation and the generation of the trigger pulse. This is so done to avoid sampling of the TAC signal in its rising edge region, where the amplitude is not yet stable.

C.2 Histogramming circuit (state machine)

After the analog signals have been digitized, the histogramming process is initiated. In order to deal with this process, a state machine was designed, clocked by a 20 MHz signal. The machine generates 100 ns width pulses to perform the reading, incrementing, and writing of data

to the corresponding address in memory. By using this circuit instead of microprocessors or microcontrollers in the histogramming process, we achieved a minimum processing dead time of 200 ns, increasing the overall acquisition rate. The state machine operates in continuous mode during data taking, just pausing during a host PC access. At this period, the host takes the address and data buses of the on-board memory, reading its contents and reseting it after that. Finally, an updated image is displayed in the PC screen. The updating process is fast enough to provide almost real-time image acquisition in generally used PCs.

C.3 Control circuit

The control circuit functions are: global enable, memory access control (including data/address buses and read/write/enable pins) and ADC data shift. These operations are carried out by use of I/O instructions and D flip-flops to latch control signals. The global enable signal is used to take the memory control pins to tri-state, disabling any data access, and to latch the comparators outputs, also disabling any start of conversion. The memory access control is done by multiplexing all memory pins and buses, allowing access by the host PC and by the histogramming circuit. ADC data shift allows for varying the image resolution from 128x128 up to 1024x1024 pixels.

V. Results

In order to evaluate the system performance, concerning the image quality, we have done two tests. First, we have illuminated the detector window with an ^{55}Fe X-ray source, through a mask containing round holes with the same diameter (0.762 mm) and equally spaced (2.54 mm between centres). From the resulting image, as shown in Fig. 3, we have evaluated the linearity of the image acquisition system. In the second test, we have obtained an image of a real object by illuminating the detector with the same source used before. The next sections illustrate the results.

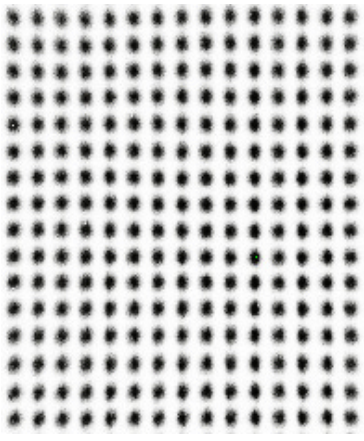

Fig. 3. X-ray image obtained by illuminating the detector window with an ^{55}Fe source through a mask containing round holes.

A. Linearity

In the linearity measurement, we have used transversal cuts, illustrated in Fig. **??**, from the most central row and column in the image of Fig. 3. Those cuts provide the peaks corresponding to each hole in the mask. By fitting each peak with a gaussian function, we have obtained the central position, in channels, for each peak. As the distance between the holes centres is a constant (2.54 mm), the relation between the peak centres and the hole positions should be linear. We have assumed the maximum deviation to a linear fit as the linearity error of our system. The measured linearity error was 0.6 % for the X direction and 1.6 % for the Y direction. Notice the the Y direction is the one orthogonal do the anode wires in the detector. For this direction, a bigger linearity error is expected for peaks lying inbetween two wires.

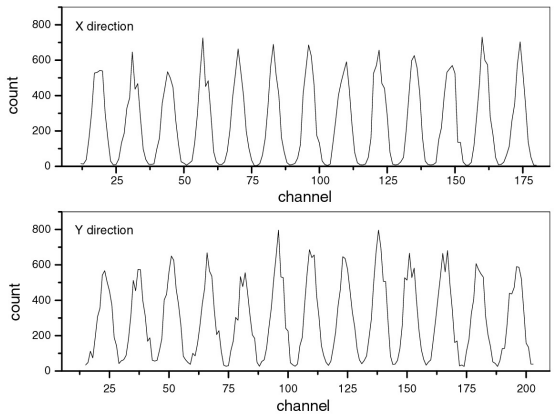

Fig. 4. Transversal cuts from the most central row and column in the image of Fig. 3.

B. Images

Fig. 5 is the image obtained by illuminating the detector with an ^{55}Fe X-ray source placed about 50 cm away from its window for a few hours. For this image, we used 1024×1024 pixels of resolution and we obtained around 1000 counts per pixel. This tests illustrates fairly good image homogeneity. In Fig. 6, a 512×512 pixels image of an empty mineral water bottle is shown. It can be seen that the remaining water bubbles are thick enough to completely absorb the radiation, while the plastic bottle material is almost transparent.

VI. Conclusions

A high-speed image acquisition system, with a two-dimensional position sensitive detector, standard read-out electronics and a new digital circuit for data acquisition, is presented. By using fast analog-to-digital converters and complex programmable logic devices, we achieved sampling rate slightly above 1.0×10^6 events per second. The counting rate is presently limited by the ADCs sampling rate. Images may be visualized with up to 1024×1024 pixels resolution. Linearity tests were evaluated resulting in errors

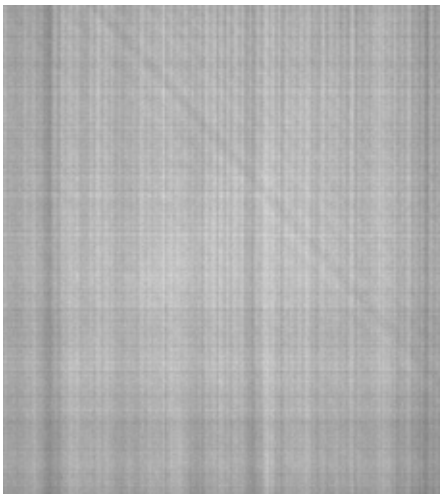

Fig. 5. Response of the detector to illumination by an ^{55}Fe source, with 1024 x 1024 pixels resolution.

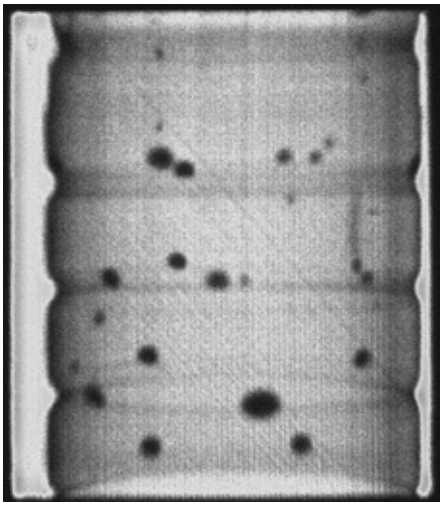

Fig. 6. X-ray image, with 512 x 512 pixels, of an empty mineral water bottle of with some remaining bubbles.

lower than 0.6 % for X direction and 1.6 % for Y direction. The obtained spatial resolution is better than 1mm in both X and Y directions, limited by the detector anode wire pitch.

Acknowledgments

The present work has been developed in the Brazilian Center for Physics Research (CBPF-Brazil). Finantial support has been granted by CNPq (brazilian national research funding agency) and FAPERJ (Rio de Janeiro research funding agency).

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