A TDC-Based System for X-Ray Imaging Detectors

L. M. de Andrade Filho, A. F. Barbosa, H. P. Lima, Jr., and P. R. B. Marinho

***Abstract*—An image acquisition system is presented for use with position sensitive detectors (PSD). The system is based on a high-resolution time-to-digital converter (TDC) and a field programmable gate array (FPGA). The detectors use gas as absorbing medium and two delay lines to identify the coordinates of each detected particle. The TDC translates the time information coming from the delay lines into digital words, from which the particle position coordinates are encoded. The FPGA is responsible for processing each event, controlling the data acquisition and communicating with a personal computer. 256 pixels × 256 pixels images are stored into an on-board memory. This resolution is increased to 512 pixels × 512 pixels by using a time multiplexing technique. The maximum data acquisition rate is 1.2 million events per second. X-ray images obtained with the system are shown, which illustrate the overall performance.**

***Index Terms*—Delay line readout, image acquisition system, time-to-digital converter, X-ray detector.**

I. Introduction

POSITION sensitive detectors (PSDs) are at the base of imaging systems for ionizing particles. In particular, multiwire proportional counters (MWPC) [1], [2] have been widely used in applications where two-dimensional localization of particles is required. More recently, multi Gas Electron Multiplier (GEM) structures [3] are also being considered in the conception of imaging PSDs. In this work we report the development of an image acquisition system for PSDs in which the position measurement is based on the measurement of a time interval. This is the case for both the MWPC [4] and the GEM-based detectors [5] when a delay line is incorporated to encode the particle position. The time measurement relies on a time-to-digital converter (TDC), and the data acquisition is implemented with a field programmable gate array (FPGA). The process includes the detection of the ionizing particles, analog and digital signal processing, data acquisition and displaying. The complete imaging system is illustrated in Fig. 1.

The read-out chain starts with fast pre-amplifiers at the detector front-end level. The pre-amplifiers are homemade and were designed to match the used PSDs and the delay lines. For discrimination, we use standard NIM electronic modules. The TDC is an 8-channel commercially available integrated circuit featuring time resolution adjustable down to 120 ps. Each TDC channel converts the time interval between the signal from one end of a delay line and a reference signal (start), provided by the detector anode, which triggers the occurrence of the event. In order to improve the position encoding technique, signals from both ends of the delay lines are used to compose the final position information.

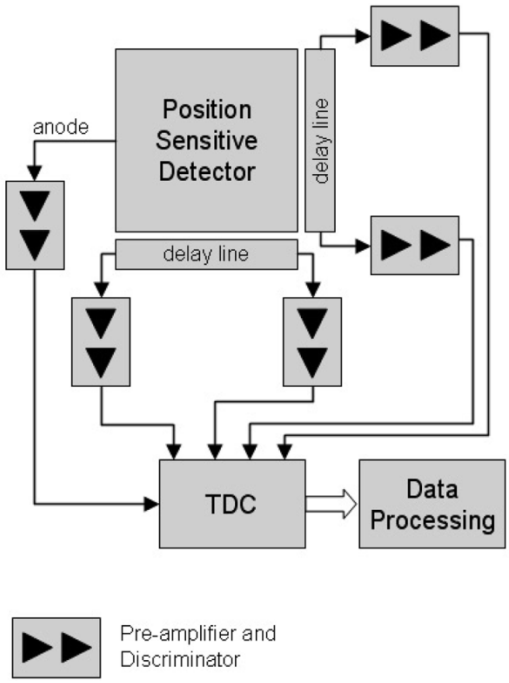

Fig. 1. Block diagram of the complete imaging system.

II. Detectors

Two position sensitive detectors have been used to test the image acquisition system here presented. The first one is a MWPC using an anode wire plane and two delay lines coupled to a cathode plane. The latter is a multilayer printed circuit board called X&Y cathode [6], in which the ionization charge is sampled and shared by two orthogonal sets of strips related to the X and Y position coordinates. The second detector, similar to the MWPC, makes use of the same read-out scheme. However, instead of using a wire plane, a triple-GEM structure is used [7]. The delay line read-out method, used in both detectors, consists in sampling the electric signal in a segmented electrode, with the segments connected to the discrete L-C cells of a delay line circuit. Each cell provides an approximately constant delay ($\tau = \sqrt{LC}$), provided that the signal frequencies are below the cutoff frequency ($w_o = 2/\tau$). The delay line characteristic impedance is given by ($\sqrt{L/C}$) for frequencies below w_o. The time taken by a signal to travel through the delay line is proportional to the position of the particle originating the signal.

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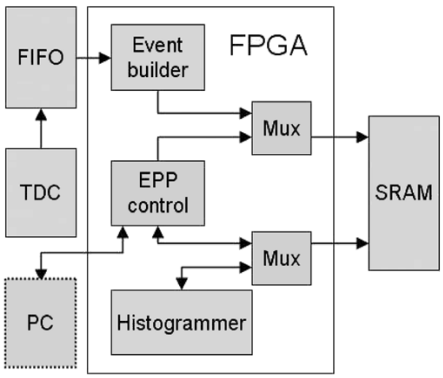

Fig. 2. Schematic diagram of the acquisition system.

The results presented for the MWPC refer to a detector with an 8.0 cm $\times$ 8.0 cm beryllium window, filled with an argon-methane gas mixture at 0.1 Atm above normal pressure. The anode is built with 10 μm gold coated tungsten wires at 1.0 mm pitch. The gap between the anode and the X&Y cathode planes is 4.0 mm. The total delay of each delay line is $\approx$250 ns. The MWPC features a gain of 10^4, when operated at 2.6 kV.

The second detector uses a similar multilayer printed circuit board as an X&Y anode in a triple-GEM structure. The charge sensing elements in the X&Y anode individually collect the electrons derived from the last GEM. The results reported were obtained with a GEM size of 30 mm $\times$ 30 mm, one of the standard types produced at CERN. The hole shape is double-conical, with an inner diameter of about 50 μm and 80 μm at the metal surface. The holes are arranged in a hexagonal pattern at 140 μm pitch. The overall thickness of the GEM foil is about 60 μm: 50 μm thick Kapton with 5 μm copper on each side. For the drift cathode a metal mesh with 81% transparency was used. Below the last GEM was placed the X&Y anode. The drift, transfer and induction gaps were kept at 3.2 mm, 1.9 mm and 4.0 mm, respectively. The detector window is made with 0.4 mm thick carbon fiber, 2.3 cm $\times$ 2.3 cm area. The detector operates in flow mode at atmospheric pressure, with $\mathrm{Ar/Xe/CO_2}$ (64/16/20) gas mixture. The drift, transfer and induction fields were kept constant at 1.5 kV/cm, 2 kV/cm and 3 kV/cm, respectively. The electrodes were polarized so that the detector operates with a gain close to 5×10^5. The total delay of the delay lines in the triple-GEM detector is $\approx$80 ns.

III. Data Acquisition System

The data acquisition system, illustrated in Figs. 1 and 2, basically consists of four time-to-digital conversion channels, one memory [first in, first out (FIFO)] to store the TDC conversions, an FPGA (Xilinx XC4010E) to control the data acquisition process, and a static memory used to store the 256 pixels $\times$ 256 pixels image with counting capacity of 16 bits per pixel. This design is an alternative to previous systems that used standard time-to-analog converter modules plus an analog-to-digital converter at the input stage [8].

Under the operating conditions of the data acquisition system here described (1 common start plus 4 stop channels used), the TDC is able to process up to 1.2 million events per second, which is enough for a wide range of applications. The detectors expected spatial resolution is approximately 1 mm FWHM for the MWPC and 0.3 mm FWHM for the triple-GEM. Assuming that at least 4 pixels in each direction are required to sample the detectors point-spread functions, we conclude that the best quality images would require the TDC time resolution to be set to 0.78 ns and 0.26 ns respectively for the MWPC and for the triple-GEM. The resulting image would not fit into 256 pixels $\times$ 256 pixels. We therefore have to provide 512 pixels $\times$ 512 pixels images. In order to obtain this image size with a lower capacity on-board memory, the detector window is virtually divided in four quadrants. The TDC time resolution is then programmed so that each quadrant fills a 256 pixels $\times$ 256 pixels image. This is carried out by digitally analyzing the data coming from the TDC and histogramming only the events occurring inside the quadrant of interest. The quadrants are multiplexed in time, which means that the circuit acquires the data and fills the memory only with information of one quadrant at a time. This process generates a 512 pixels $\times$ 512 pixels image. It is worth noting that this technique allows one to obtain an enhancement in image resolution while keeping a lower capacity memory circuit, and that it may be extended to higher memory sizes. The data are read and transferred to the PC, and the higher resolution image is built and stored in the PC memory. It should also be noted that, since only events in one quadrant at a time are acquired, the effective data acquisition rate for the whole detector is decreased, while the image resolution is increased. However, it also means that the rate of events hitting the detector window may be up to 4 $\times$ 1.2 MHz with negligible dead-time losses due to the data acquisition, since each quadrant acquires data independently.

A. The Time-to-Digital Converter

The TDC chosen is the F1 model of Acam (available online at http://www.acam.de). It features one common start and 8 individual stop channels, 16-bit range, with time resolution adjustable down to 120 ps. Using a software facility, the time resolution may be adjusted and calibrated by means of a quartz crystal, through a phase locked loop (PLL) circuitry [9]. All the input signals are LVPECL standard, but may also act as single ended inputs if one applies a trigger threshold to the TDC negative input. The F1 model provides an interface to directly control some digital-to-analog converters commercially available. By using this interface, the threshold levels for each stop input may be controlled by software. The TDC F1 is programmed by some configuration registers. Write operations in these registers are carried out in a serial way, using a specific protocol. A control block inside the FPGA is responsible for the implementation of this protocol. In order to keep design modularity, a separate card is used only to host the TDC, as shown in Fig. 3.

The start signal and the eight stop signals are connected to the card through 50 Ω coaxial cables and LEMO standard connectors. For the present application, only four channels are needed, one pair for each delay line. A second card, shown in Fig. 4, was designed to host the remaining devices (FPGA, FIFO, and static memory) of the acquisition system.

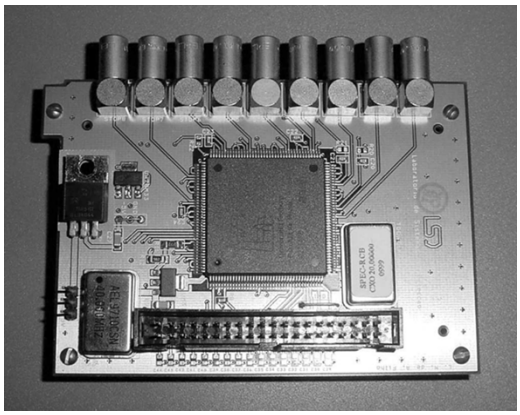

Fig. 3. Card hosting the time-to-digital converter.

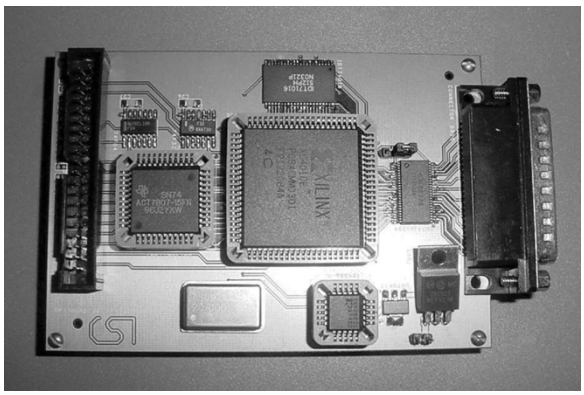

Fig. 4. Card for event building and histogramming.

B. The Event Builder and the Histogrammer Blocks

All the hardware in the image acquisition system is controlled by means of commands received through the EPP[1] Control block, shown in Fig. 2, which interfaces the parallel port of a PC. The parallel port was chosen because it is available in most PCs, old or new, but any other standard bus could have been used. The EPP Control block is responsible, for instance, for the configuration of the TDC and for the readout of its status signals. The EPP control shares the access to the on-board memory with the Event Builder and the Histogrammer blocks. The Event Builder is responsible for interpreting the data coming from the TDC, generating the final address to the memory, where the events are accumulated by the Histogrammer block. A control signal disables the Event Builder block when the PC requests a memory access through the EPP Control. In order to avoid the loss of data coming from the TDC during that period, a FIFO memory featuring 2048 addresses is used as a buffer to store the TDC conversions. When the Event Builder is enabled, it generates a trigger signal to set the Histogrammer to a wait state. As soon as a new memory address is provided, the Histogrammer is triggered and initiates a new processing cycle. Since the Event Builder and the Histogrammer blocks are based on state machines running at 20 MHz in pipeline mode, the system dead time is only due to the TDC acquisition rate.

[1]EPP stands for *Enhanced Parallel Port*, which is a fast mode for transferring data up to 2 MBytes/s.

Among the internal blocks in the FPGA, the Event Builder is the most complex and important one, being described here in more detail. The input stage is responsible for separating the events converted by the TDC according to the input channel from where they have been received. The next stage combines the information coming from the delay lines. The time difference for signals from the delay lines with respect to the common start signal is computed. Alternatively, the time differences for signals coming from both ends of each delay line may also be computed. In either case, the final result is treated as a memory address which should have its content incremented by one (histogramming). The last two stages in the Event Builder are the coincidence trigger and the event filter. In the coincidence trigger, a time window is generated to assure that an event is valid. For each channel, an event is required to occur inside that window before it is passed to the next stage. The time window width corresponds to the total delay of the delay lines, so that the signals involved in the particle position measurement have to be registered during this time, otherwise it is not a valid event. The event filter is applied when the time multiplexing technique is used. It discards events outside the quadrant of interest.

IV. Results

The data acquisition system performance has been evaluated in specific tests where the linearity and the resolution have been measured. The measurements are focused on the TDC, since the detectors spatial resolution does not depend on the data acquisition system. The characterization results presented below were obtained using pulse generators. X-ray images acquired with the two detectors are also presented, so that the overall performance of the complete system is also evaluated.

A. Resolution

In order to check that the TDC performs as expected and as specified by the manufacturer, its time resolution was programmed to match the PSD's spatial resolution. Notice that, when the position readout is done by subtracting time intervals from both ends of each delay line, the range of measured time intervals corresponds to twice the total delay of the delay lines. The TDC resolution may therefore be relaxed by a factor two, and still the best quality images fit in 512 pixels $\times$ 512 pixels. In practice, the time resolutions used are 1.92 ns for the MPWC and 480 ps for the GEM-based detector. The programmed time resolution measurement is done by imposing a fixed delay (16 ns coaxial cable) to the four stop signals sent to the TDC, while the start signal is not delayed. This scenario simulates an event occurring in the central location of the detector, i.e., both ends of each delay line producing the same delay with respect to the start signal. For a periodic signal of frequency varying from a few Hz up to 1.2 MHz, it has been found that, for both the programmed time resolutions, mainly one single pixel is hit, with a small fraction of the counts shared with neighbor pixels. The coordinates of the hit pixels have been varied by changing one of the stop signal delays, and this confirmed that the counts are again concentrated in one pixel. By fitting a Gaussian to the counts dis-

TABLE I
INL MEASURED FOR DIFFERENT TIME RESOLUTIONS

	INL X	INL Y
1.92 ns (MWPC)	0.11%	0.16%
0.48 ns (GEM)	0.77%	0.86%

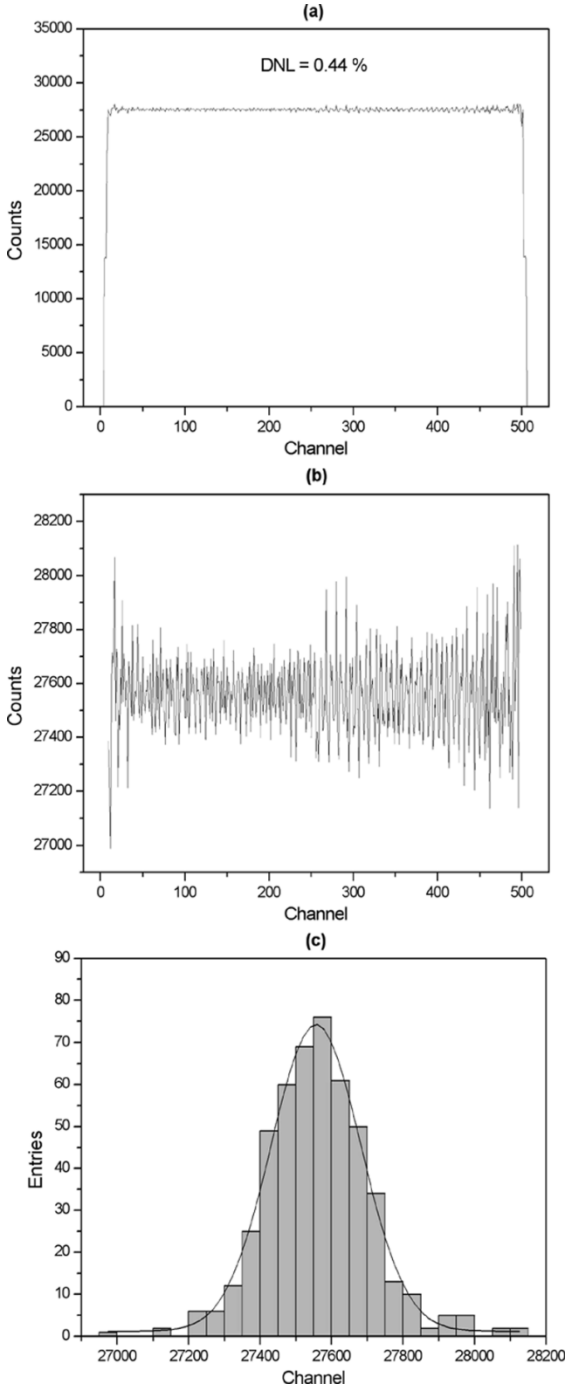

Fig. 5. Homogeneity spectrum (a), close view of the spectrum (b), and respective Gaussian fitting (c) used for the evaluation of differential non-linearity in the X direction.

tribution, the standard deviation is found to be smaller than the pixel width in time.

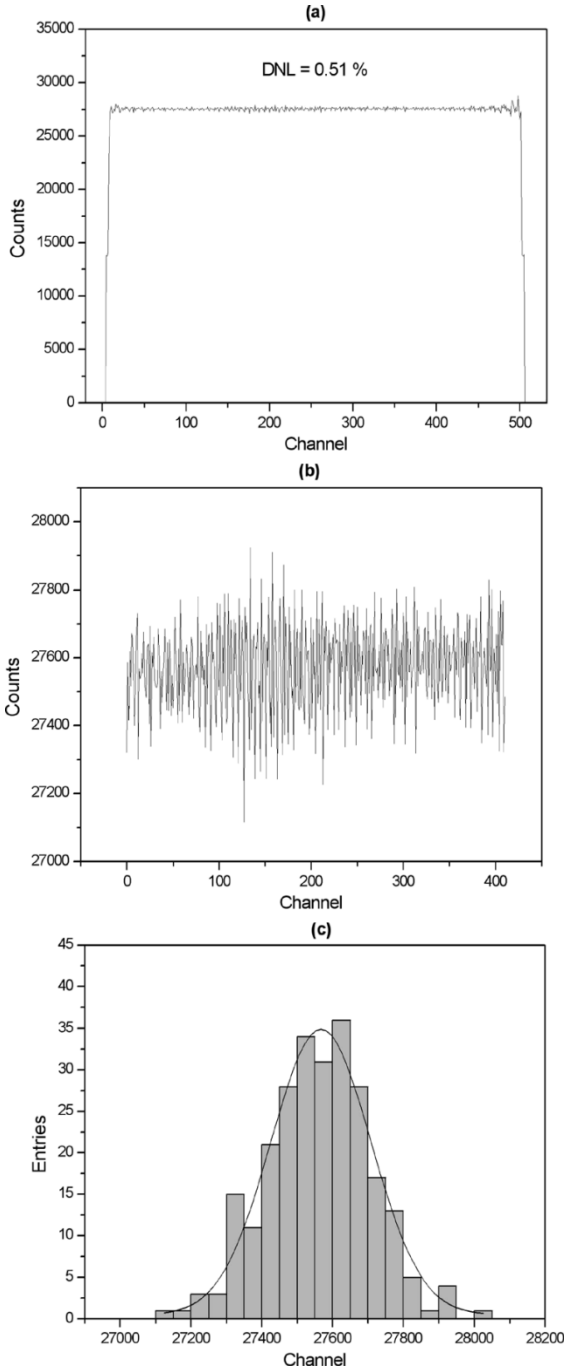

Fig. 6. Homogeneity spectrum (a), close view of the spectrum (b), and respective Gaussian fitting (c) used for the evaluation of differential non-linearity in the Y direction.

B. Linearity and Homogeneity

The linearity test of the TDC was done by varying the time difference between the start and the stop pulses in regular steps, so that the measured time intervals cover the time range of the delay lines. This measurement is done for both the PSD's resolutions, and for both directions. The used steps were 10 ns and 40 ns, respectively for the triple-GEM and MWPC cases. For each case, a plot of *true* versus *measured* time interval is obtained, to which a straight line is fit. The integral non-linearity (INL) is defined as the maximum deviation of the measurement

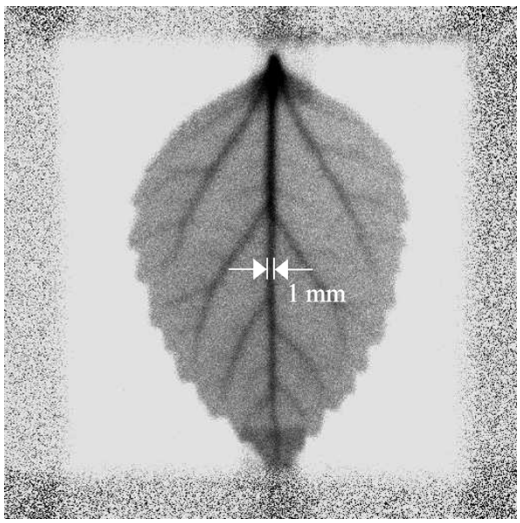

Fig. 7. X-ray image of a leaf, using the MWPC, with 512 × 512 pixel resolution.

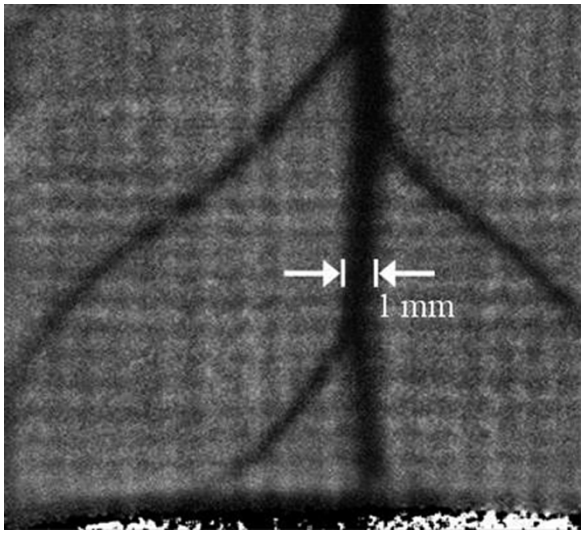

Fig. 8. X-ray image of a leaf, using the GEM-based detector, with 512 × 512 pixel resolution.

with respect to the linear fit, divided by the total range. The INL measurement results are summarized in Table I. In short, the INL is below 1.0% for both PSDs and for both coordinates.

The TDC homogeneity is equivalent to its differential non-linearity (DNL). In order to measure this parameter, events have to be generated at the same rate over the whole active window, i.e., corresponding to all time intervals in the measurement range. It is possible to do this by using two pulse generators at frequencies slightly different to provide the start and the stop signals. With this technique, time intervals are generated in the range covered by the lower period signal. Typical DNL results obtained with this procedure are shown in Figs. 5 and 6, which refer respectively to the X and to the Y coordinates. A close view of the spectra is also shown in the figures, with a Gaussian fit to the counts distribution. The DNL is taken as the standard deviation (σ) of this Gaussian fit. Again, the measurements were done for the two used time resolutions, and the maximum observed DNL was 0.51%. The important information to retain from the spectra is that, although the measurements include noise from the input pulses, the fluctuations observed in the count distribution measured by the TDC are below the Poisson noise present in radiation emission phenomena.

C. Images

Radiographic images of a leaf were obtained for both detectors using the data acquisition system, so that its performance may be visually inspected. The leaf was fixed upon the detector window and illuminated by an ^{55}Fe source. The resulting images are shown in Figs. 7 and 8.

In order to correct for detector inhomogeneities, not related to the data acquisition system, the raw image is divided by the image obtained for a long time exposure of the detector to an isotropic radiation source (the ^{55}Fe source, placed more than 30 cm away from the detector window center). This process is equivalent to normalize the detector efficiency over the window surface.

The detectors performance has been studied separately [4], [7]. The MWPC features DNL 3.6% for the X direction and 3.7% for the Y direction. The GEM-based detector DNL values are 8.4% and 6.3%, respectively for the X and Y directions. Both detectors exhibit INL below 1.0%.

Notice that the expected spatial resolution for the PSDs is correctly revealed by the developed imaging system.

V. Conclusion

A complete image acquisition system for PSDs has been developed. The system is presently designed to be used with PCs via connection to the parallel port, and it has been made so that it may be adapted to any other standard bus. A user interface software was also developed, which provides visualization and pre-analysis of the obtained images. The characterization results reported show that the data acquisition hardware and software are fairly adequate for use with PSDs where the position information is expressed as a time interval between two signals. A time multiplexing technique is included, which allows a high resolution image to be obtained from lower capacity memory integrated circuits. The system is particularly attractive for featuring low cost and compactness.

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