A TDC-Based System for X-Ray Imaging Detectors

L.M. de Andrade Filho, A.F. Barbosa, H.P. Lima Jr and P.R.B. Marinho

***Abstract*— This work presents an image acquisition system to be used with Position Sensitive Detectors (PSD). The system is based on a high-resolution Time-to-Digital Converter (TDC) and a Field Programmable Gate Array (FPGA). The detectors use gas as absorbing medium and make use of two delay lines to identify the coordinates of each detected particle. Reading the position information provided by the delay lines, the system is able to encode the position of incidence for an event in the detector window. The TDC translates the time information coming from the delay lines, while the FPGA is responsible for processing each event, controlling the whole system and communicating with a personal computer. 256×256 pixels images are stored into an on-board memory. This resolution is increased to 512×512 pixels by using a time multiplexing technique. The maximum data acquisition rate is 1.2 million events per second.**

***Index Terms*— X-Ray Detector; Delay line readout; Time-to-Digital Converter; Image Acquisition System.**

I. Introduction

Multiwire proportional counters (MWPC) [1] [2] have been widely used in systems dedicated to two-dimensional localization of particles. In this work we have developed a complete image acquisition system for these detectors, based on a Time-to-Digital Converter and a Field Programmable Gate Array. The whole process includes the detection of the ionizing particles, analog and digital signal processing, data acquisition and displaying. Home-made pre-amplifiers and NIM standard discriminators are used as the front-end electronics. The PSD may as well be a GEM based detector [3], or any other in which the particle position information is contained in a time measurement. The complete imaging system is illustrated in Fig. 1.

The readout chain starts with fast pre-amplifiers at the detector front-end level. The pre-amplifiers were specially designed to match the PSD and the delay lines in use. For discrimination, we use standard NIM electronic modules. The TDC is an 8-channel commercially available integrated circuit featuring $120\ ps$ time resolution. Each TDC channel converts the interval between the signal from one end of a delay line and a reference signal (start), provided by the detector anode, which triggers the occurrence of the event. In order to improve the image resolution, signals from both ends of the delay lines may be used to encode the final position information.

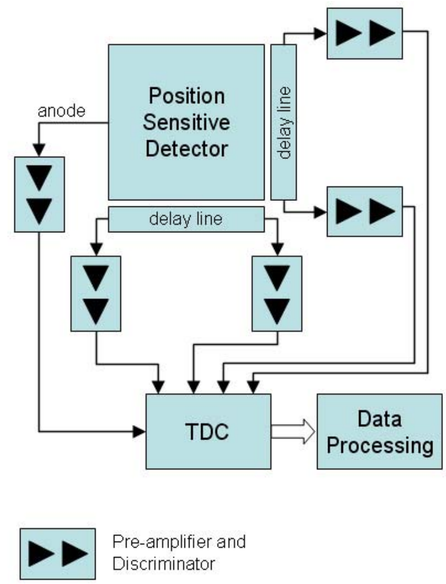

Fig. 1. Block diagram of the complete imaging system.

II. Detectors

Two position sensitive detectors (PSDs) have been used to test the image acquisition system here presented. The first one is an MWPC, using an anode wire plane and two delay lines coupled to a cathode plane, which is a multilayer printed circuit board called X&Y cathode [4]. The second detector, similar to the MWPC, makes use of the same readout scheme. However, instead of using a wire plane, a triple GEM structure is used [5].

The first PSD uses a single electrode, the X&Y cathode, to sense the electric charge induced by ionization avalanches generated by the absorption of particles. Two dimensional localization is achieved by associating one delay line to each coordinate. The presented results refer to a detector with an $8.0 \times 8.0\ cm^2$ beryllium window, filled with an Argon-Methane gas mixture at $0.1\ Atm$ above normal pressure. The anode is built with $10\ \mu m$ gold coated tungsten wires at $1.0\ mm$ pitch. The gap between anode and X&Y cathode planes is $4.0\ mm$. The total delay of each delay line is about $300\ ns$.

The second detector uses a similar multilayer printed circuit board as an X&Y anode in a triple GEM structure. The charge sensing elements, in the X&Y anode, individually collect the electrons derived from the last GEM. The results reported were

L.M. de Andrade Filho is with the Laboratório de Sistemas de Detecção, Centro Brasileiro de Pesquisas Físicas, Rio de Janeiro, RJ 22290-180 Brazil (telephone: 55-21-2141-7371, email: lucianof@cbpf.br).

A.F. Barbosa is with the Laboratório de Sistemas de Detecção, Centro Brasileiro de Pesquisas Físicas, Rio de Janeiro, RJ 22290-180 Brazil (telephone: 55-21-2141-7263, email: laudo@cbpf.br).

H.P. Lima Jr is with the Laboratório de Processamento de Sinais, Universidade Federal do Rio de Janeiro, Rio de Janeiro, RJ Brazil (telephone: 55-75-224-8289, email: herman@lps.ufrj.br).

P.R.B. Marinho is with the Laboratório de Sistemas de Detecção, Centro Brasileiro de Pesquisas Físicas, Rio de Janeiro, RJ 22290-180 Brazil (telephone: 55-21-2141-7371, email: renato@cbpf.br).

obtained with a GEM size of $30\times30\ mm^2$, one of the standard types produced at CERN; the hole shape is double-conical with an inner diameter of about 50 μm and 80 μm at the metal surface. The holes are arranged in a hexagonal pattern at 140 μm pitch; the overall thickness of the GEM foil is about 60 μm: 50 μm thick Kapton with 5 μm copper on each side. For the drift cathode we used a metal mesh with 81 % transparency. Below the last GEM was placed the X&Y anode. The drift, transfer and induction gaps were kept at 3.2, 1.9 and 4 mm, respectively. The detector window is $2.3\times2.3\ cm^2$ made with a 0.4 mm thick carbon fiber. The detector operates in flow mode at atmospheric pressure, with $Ar/Xe/CO_2$ (64/16/20) gas mixture. The drift, transfer and induction fields were kept constant at 1.5, 2 and 3 kV/cm, respectively. The electrodes were polarized in such a way that the detector operates with a gain of 5×10^5. The total delay of the delay lines is 100 ns.

III. Data Acquisition System

The data acquisition system, shown in Fig. 1 and Fig. 2, basically consists of four time-to-digital conversion channels, one memory (FIFO) to store the TDC conversions, an FPGA to control the acquisition process, and a static memory used to store the 256×256 pixels image with counting capacity of 16 bits per pixel. This design is an alternative to previous systems that used standard Time-to-Analog Converter modules plus an Analog-to-Digital Converter in the input stage [6].

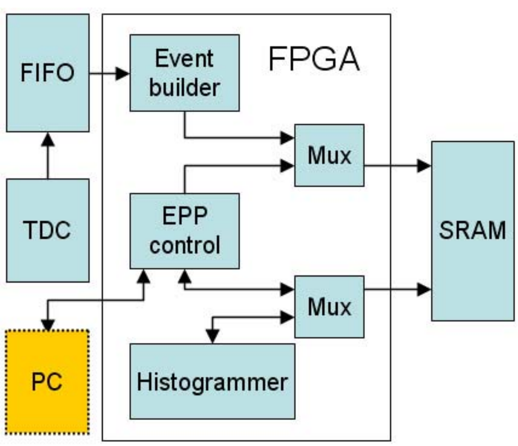

Fig. 2. Schematic diagram of the acquisition system.

The maximum acquisition rate of 1.2 million of events per second is imposed by the TDC. In order to obtain better resolution, generating an image with 512×512 pixels, the active window of the detector is divided in four quadrants. This process is carried out by digitally analyzing the data coming from the TDC and accumulating only the events occurring inside the quadrant of interest. The quadrants are multiplexed in time, which means that the circuit acquires the data and fills the memory only with information of one quadrant at a time. This process may be extended yet to higher resolution (up to 8192×8192 pixels) provided that higher capacity memory chips are available in the PC board. Finally, data are read through the parallel port of the PC and the image is stored in the PC memory. Since the events that occurr inside other quadrants are discarded, the effective data acquisition rate is decreased, while the resolution is increased.

A. The Time-to-Digital Converter

The TDC chosen, the F1 model of Acam [7], has 8 channels, resolution adjustable down to 120 ps per channel and 16 bits of encoding resolution. Using a software facility, the resolution may be adjusted and calibrated by means of a quartz crystal, through a PLL (Phase Locked Loop) circuitry [8]. There is one common start signal for the 8 channels. All the input signals (start and stop) are LVPECL standard, but may act also as single ended inputs if one applies a trigger threshold to the TDC negative input. In order to simplify and make this feature more powerful, the TDC F1 provides an interface to directly control some digital-to-analog converters commercially available. By using this interface, the threshold levels for each stop input may be controlled by software. The TDC F1 is controlled by some configuration registers. Write operations in these registers are carried out in a serial way, using a specific protocol. A control block inside the FPGA is responsible for the implementation of this protocol. In order to keep design modularity, a separate card is used only to host the TDC, as shown in Fig. 3.

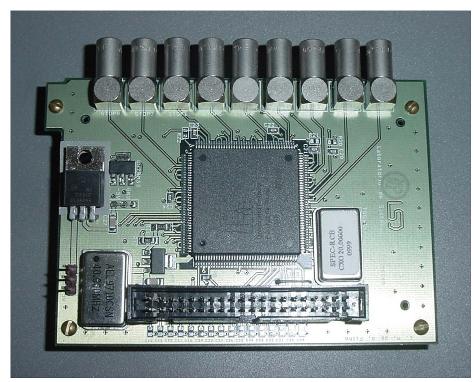

Fig. 3. Card hosting the Time-to-Digital Converter.

The start signal and the eight stop signals are connected to the card through 50 Ω coaxial cables and LEMO standard connectors. For the present application, only four channels are needed, one pair for each delay line. A second card, shown in Fig. 4, was designed to host the remaining devices (FPGA, FIFO and static memory).

B. The Event Builder and the Histogrammer blocks

All the hardware in the image acquisition system is controlled by means of commands received through the EPP Control block, shown in Fig. 2, which interfaces the parallel port of a PC. This block is responsible, for instance, for the configuration of the TDC and for the readout of its status

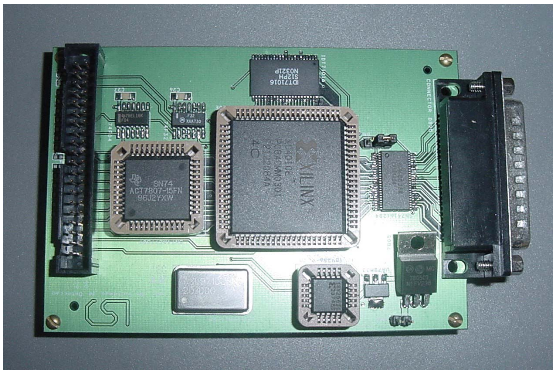

Fig. 4. Card for event building and histogramming.

signals. The EPP Control block shares the access to the on-board memory with the Event Builder and the Histogrammer blocks. The Event Builder is responsible for interpreting the data coming from the TDC, generating the final address to the memory, where the events are accumulated by the Histogrammer block. A control signal disables the Event Builder block when the PC requests a memory access through the EPP Control. In order to avoid that data coming from the TDC are lost during this period, a FIFO is used to store the last conversions from the TDC. When the Event Builder is enabled, it generates a trigger signal to set the Histogrammer to a wait state. As soon as a new memory address is provided, the Histogrammer is triggered and initiates a new processing cycle.

Among the internal blocks in the FPGA, the Event Builder is the most complex and important one, being described here in more detail. The input stage is responsible for separating the events converted by the TDC according to the input channel from where they have been received. The next stage combines the information from both ends of the same delay line, subtracting them to form an address. The last two stages in the Event Builder are the coincidence trigger and the event filter. In the coincidence trigger, a time window is generated to verify that an event is valid. For each channel, an event is required to occur inside that time window before it is passed to the next stage. The second filter is applied only when the time multiplexing technique is used. It discards events outside the quadrant of interest.

IV. RESULTS

Several tests have been carried out to measure the system linearity and resolution. Some results are presented corresponding to the use of a pulse generator instead of the detector and the delay lines. Results obtained using the detectors are also presented.

A. Resolution

In order to measure the time resolution, a fixed delay (a 16 ns coaxial cable) was imposed to the four stop signals sent to the TDC. This scenario simulates an event occurring in the central location of the detector, that is, both ends of each delay line producing the same delay related to the start signal. The TDC resolution was matched to the MWPC. Since the maximum delay of the delay line is 300 ns, and the memory stores 256 pixels per direction, the resolution chosen for the TDC was 1.0 ns. This resolution is selected by discarding some least significant bits of the TDC. As expected, in the resulting image, only one pixel is hit in the center (coordinate [128,128]). The measurements have shown that only this pixel is activated for the whole range of operation frequencies of the TDC (from few Hz up to 1.2 MHz).

B. Linearity and Homogeneity

The linearity test was done by varying the difference in time between the start and stop pulses up to 450 ns, in steps of 50 ns. In the X direction, for each variation in the time difference, the peak moves exactly 13 channels, therefore non-linearities were not observed. In the Y direction, the maximum deviation from the fit divided by the number of channels was measured as 0.20 %. This value is the Integral Non-Linearity (INL) of the system in the Y direction.

In order to measure the homogeneity, a second pulse generator was used. The output of the first generator (at 1.00 MHz) drives three stop inputs of the TDC, while the second generator (at 1.05 MHz) drives the fourth stop. By using this configuration, the position of the events in one of the directions (X for example) is fixed and one can measure the DNL in the other direction (Y). The small difference in the frequencies of the generators provides the possibility to scan all the time intervals up to 1.0 μs. Fig. 5 and Fig. 6 show the resulting homogeneity curves, respectively for X and Y. A close view of the spectrum and the Gaussian fit to the counts distribution are also shown for each direction.

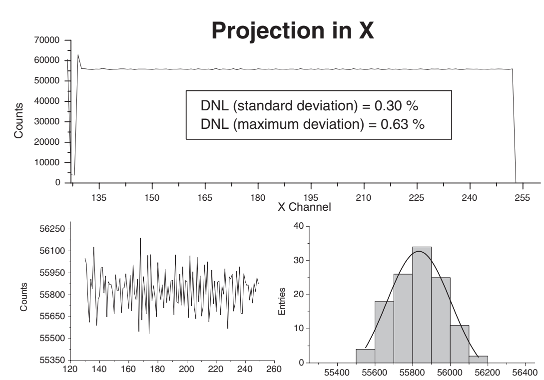

Fig. 5. Differential Non-Linearity (homogeneity) in the X direction.

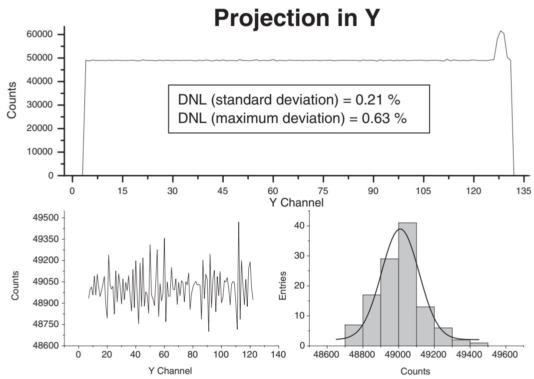

Fig. 6. Differential Non-Linearity (homogeneity) in the Y direction.

C. Images

The radiographic image of a leaf was obtained for both detectors using the data acquisition system, so that its performance could be visually inspected. The leaf was fixed upon the detector window and illuminated by an ^{55}Fe source. The resulting images are shown in Fig. 7 and Fig. 8.

In order to correct for detector inhomogeneities, the raw image has been divided by the image obtained by a long time exposure of the detector to an isotropic radiation source (the ^{55}Fe source, placed more than 30 cm away from the detector window center). This process is equivalent to normalize the detector efficiency over the window surface.

Note that the GEM-based detector provides better spatial resolution, as expected from its micro-fabricated electrodes.

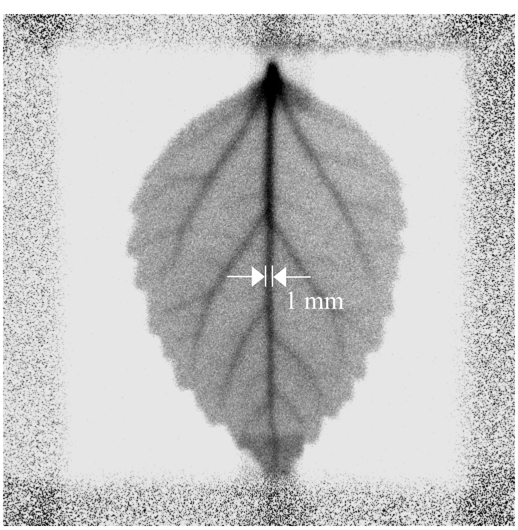

Fig. 7. X-ray of a leaf, using the MWPC, with 512×512 pixel resolution.

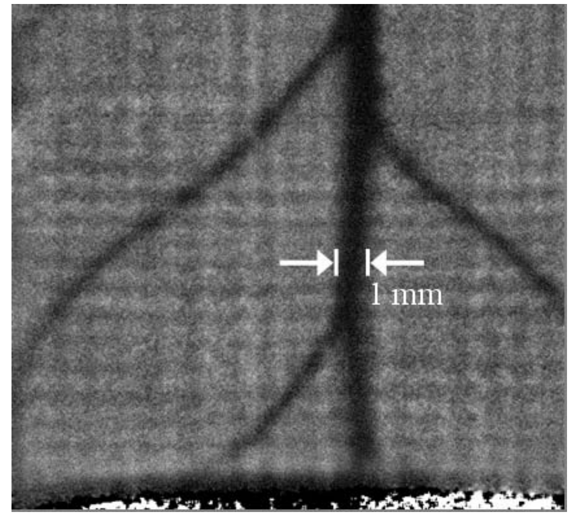

Fig. 8. X-ray of a leaf, using the GEM-based detector, with 512×512 pixel resolution.

V. Conclusion

A complete image acquisition system for PSDs has been developed. The system is designed to be used with a personal computer, connected to the parallel port. An user-friendly software was also developed, which allows easy visualization and analysis of the images obtained. The maximum differential non-linearity, measured as the standard deviation of a homogeneity curve, was 0.30%, which is mainly due to the use of a high-resolution Time-to-Digital Converter. The acquisition electronics may be used in any other two-dimensional detection experiment, where the position information for an event is expressed as a time interval between two signals. Preliminary images, with 512×512 pixels, illustrate the viability of the system. Image processing algorithms are currently under development to improve the quality of the raw images. These algorithms apply techniques such as background suppression, filtering and smoothing, to remove some imperfections present in the detectors.

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