THEORETICAL EXERCISE 5

ANSWER 1

a) 8MB = 64000000 bit
   $64000000*10^{-5}$ = 640 dollars Ram
   1MB = 8000000 bit
   $8000000*10^{-4}$ =800 dollars Cache
   Ram is cheaper than cache.

b) RAM
   1320=H*1200+(1-H)(100+1200)
   1320=1200H+1300-1300H
   1320=1300-100H
   100H=-20
   H=-20/100=-0,2
   CACHE
   110=H*100+(1-H)(100+1200)
   110=100H+1300-1300H
   110=1300-1200H
   1200H=1190
   H=1190/1200=0,99

c) 0,901 =H*100+(1-H)(100+1200)
   0,901=1300-1200H
   1200H=1300-0,901
   H=(1300-0,901)/1200=1,082
   Performance improved.

ANSWER 2

a) Cache = Numbers of blocks*Size of each Word
   Cache = 2K*128=$2^1*2^{10}*2^7 = 2^{18}$ words
   Physical address= $\log_2(2^{18})$=18
   Word offset= $\log_2(128)$=7
   Number of lines(cache)=64
   Line number=$\log_2(64)$=6
   Tag=18-(7+6)=5bits S=6bits W=7bits

b) Cache=Numbers of blocks*Size of each Word
Cache = 2K*128=2^1*2^{10}*2^7 = 2^{18} words
Physical Address= $\log_2(2^{18})$=18
Word offset= $\log_2(128)$=7
Tag=18-7=11bits W=7bits

c) Cache= Numbers of blocks*Size of each Word
Cache= 2K*128=2^1*2^{10}*2^7 = 2^{18} words
Physical Address= $\log_2(2^{18})$=18
Word offset= $\log_2(128)$=7
Number of lines(cache)=64
Number of sets(cache)=64/4=16
Set number= $\log_2(16)$=4
Tag=18-(7+4)=7bits S=4bits W=7bits

ANSWER 3

a) Block size=16 bytes
Lines=8 KB/16B=$2^{13}/2^4=2^9$ r=9
Blocks=64MB/16B=$2^{26}/2^4=2^{22}$ s=22
Words=16B/1B=2^4 w=4
Number of addressable unit(2^{s+w})=2^{26}
Address length(s+w)=26
Block size$2^w=2^4$
Number of blocks in main memory(2^s)=2^{22}

b) Direct mapping
Tag=22-9=13

c) Associative mapping
Tag=22

d) Set Associative
Tag=22-1=21

e) 0011 1111 0100 1010 1101 0110 1001
3 F 4 A D 6 9
Direct Mapping
Tag= 0011 1111 0100 = 7E9
Word=1001=9
Associative Mapping
Tag=0011 1111 0100 1010 110101=FD2B5
Word=1001=9

Set Associative Mapping
Tag=0011 1111 0100 1010 11010=6E95A
Word=1001=9

ANSWER 4

a) Miss ratio = 97/386=0,251
   Hit ratio=1-0,251=0,749
b) Hit time=8ns → Access time of cache
   Miss time=23ns →Access time of cache+Access time of ram
c) Non-overlapped
   Effective Access Time=H*Access(cache)+M*(Access(cache)+Access(ram))
   = 0,749*8+0,251*23
   = 11,76
   Overlapped
   Effective Access Time=H*Access(cache)+M*Access(ram)
   =0,749*8+0,251*15
   =9,75

ANSWER 5

a) 101010101100 →Hit
b) 1100110011001100 →Hit
c) 1010101100 →Miss
d) 0101011000000→Miss
e) 0000110 →Miss
f) 0110000 →Miss

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