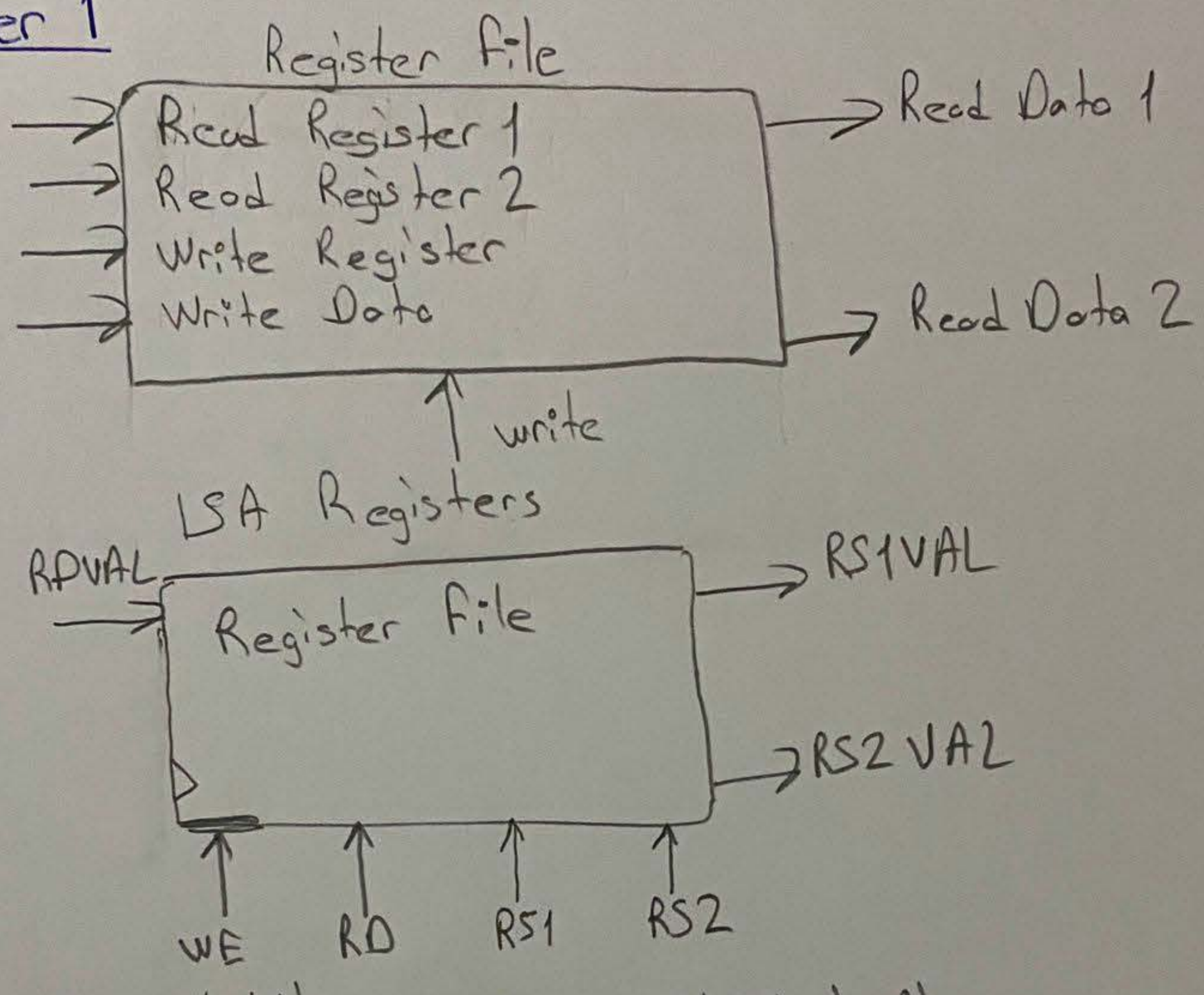
THEORETICAL EXERCISE 4

Answer 1

a)



b)

RDVAL = 16 bits
RS1VAL = 16 bits
RS2VAL = 16 bits

Register 16 bits length

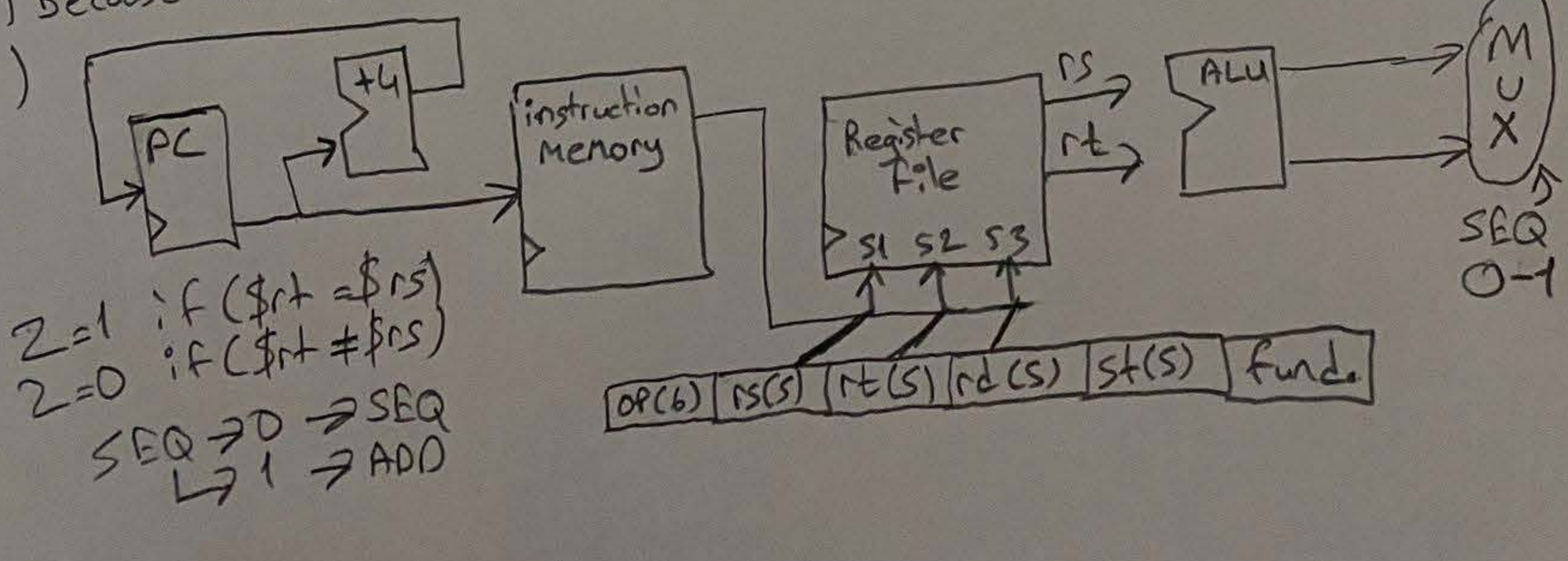
c) $2^n = 2 \quad n = 1 \Rightarrow$ RD = 1 bit RS1 = 1 bit RS2 = 1 bit

Answer 2

a) Add instruction and R-type

b) Because its byte addressable

c)



Z=1 if ($rt = $rs)
Z=0 if ($rt ≠ $rs)

SEQ → 0 → SEQ
↳ 1 → ADD

Answer 3

a) Branch instruction because B-Type is used and BR is 1.

b) Z=0 ⇒ PC+4
Z=1 ⇒ PC+4+shift

c) There is no return to the register file, so control signals are not used.

Answer 4

a) rwe=1, br=0, up=0, Aluop=0 ALU inB=1, rwd=0, rdst=0
dmwe=don't care

b) ALU inB=1, Aluop=0, dmwe=1, rdst=0, sp=0, br=0
rwd=don't care rwe=don't care

c) sp=1 br=0

Answer 5

a) opcode → 000

b) opcode → 010

c) Its depends on the sw instruction being 1.

d) addi=0
sw=0
lw=0

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