

Roteiro 9 - Laboratório de Organização e Arquitetura de Computadores

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PROBLEMA 1

3.a O endereço que memória que aponta para a primeira instrução é 0x00000000

The screenshot shows a MIPS simulator interface. At the top, there are control buttons: Run, Step, Prev, Reset, Dump, Trace, and Re-assemble from Editor. Below these is a table of instructions with columns for PC, Machine Code, Basic Code, and Original Code. The first instruction is at PC 0x0, Machine Code 0x04C0006F, Basic Code jal x0 76, and Original Code j main. To the right, there is a memory dump window showing a table with columns Address, +3, +2, +1, and +0. The first row shows address 0x00000018 with values 00, 02, 8C, and 63. Below the instruction table is a console output area.

PC	Machine Code	Basic Code	Original Code
0x0	0x04C0006F	jal x0 76	j main
0x4	0xFF810113	addi x2 x2 -8	addi sp, sp, -8
0x8	0x00C12023	sw x12 0(x2)	sw a2, 0(sp)
0xc	0x00112223	sw x1 4(x2)	sw ra, 4(sp)
0x10	0x00200293	addi x5 x0 2	addi t0, x0, 2
0x14	0x005622B3	slt x5 x12 x5	slt t0, a2, t0
0x18	0x00028C63	beq x5 x0 24	beq t0, x0, anotherCall
0x1c	0x00412083	lw x1 4(x2)	lw ra, 4(sp)
0x20	0x00012603	lw x12 0(x2)	lw a2, 0(sp)
0x24	0x00810113	addi x2 x2 8	addi sp, sp, 8
0x28	0x00100513	addi x10 x0 1	addi a0, x0, 1
0x2c	0x00000067	jalr x0 x1 0	jr ra

Address	+3	+2	+1	+0
0x00000018	00	02	8C	63
0x00000014	00	56	22	83
0x00000010	00	20	02	93
0x0000000C	00	11	22	23
0x00000008	00	C1	20	23
0x00000004	FF	81	01	13
0x00000000	04	C0	00	6F
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Jump to -- choose -- Up Down

3.b O endereço de memória que aponta para a última instrução é 0x00000050

The screenshot shows a MIPS simulator interface. At the top, there are control buttons: Run, Step, Prev, Reset, Dump, Trace, and Re-assemble from Editor. Below these is a table of instructions with columns for PC, Machine Code, Basic Code, and Original Code. The last instruction is at PC 0x0, Machine Code 0x04C0006F, Basic Code jal x0 76, and Original Code j main. To the right, there is a memory dump window showing a table with columns Address, +3, +2, +1, and +0. The first row shows address 0x00000060 with values 00, 00, 00, and 00. Below the instruction table is a console output area.

PC	Machine Code	Basic Code	Original Code
0x0	0x04C0006F	jal x0 76	j main
0x4	0xFF810113	addi x2 x2 -8	addi sp, sp, -8
0x8	0x00C12023	sw x12 0(x2)	sw a2, 0(sp)
0xc	0x00112223	sw x1 4(x2)	sw ra, 4(sp)
0x10	0x00200293	addi x5 x0 2	addi t0, x0, 2
0x14	0x005622B3	slt x5 x12 x5	slt t0, a2, t0
0x18	0x00028C63	beq x5 x0 24	beq t0, x0, anotherCall
0x1c	0x00412083	lw x1 4(x2)	lw ra, 4(sp)
0x20	0x00012603	lw x12 0(x2)	lw a2, 0(sp)
0x24	0x00810113	addi x2 x2 8	addi sp, sp, 8
0x28	0x00100513	addi x10 x0 1	addi a0, x0, 1
0x2c	0x00000067	jalr x0 x1 0	jr ra

Address	+3	+2	+1	+0
0x00000060	00	00	00	00
0x0000005C	00	00	00	00
0x00000058	00	00	00	00
0x00000054	00	00	00	00
0x00000050	FB	5F	F0	EF
0x0000004C	00	50	06	13
0x00000048	00	00	80	67
0x00000044	02	A6	05	33
0x00000040	00	81	01	13
0x0000003C	00	01	26	03
0x00000038	00	41	20	83
0x00000034	FD	1F	F0	EF
0x00000030	FF	F6	06	13

Jump to -- choose -- Up Down

3.c No total, são ocupados 21 bytes de memória.

4.a O conteúdo do registrador que armazena o valor de n (a2) é 0x00000000

The screenshot shows a MIPS simulator interface. At the top, there are tabs for Registers, Memory, Cache, and VDB. Below these is a table of registers with columns for Register Name, Integer (R), and Floating (F). The registers are listed from zero to a4 (x14). The value of register a2 (x12) is 0x00000000. Below the register table is a console output area.

Register Name	Integer (R)	Floating (F)
zero	0x00000000	
ra (x1)	0x00000000	
sp (x2)	0x7FFFFFFD	
gp (x3)	0x10000000	
tp (x4)	0x00000000	
t0 (x5)	0x00000000	
t1 (x6)	0x00000000	
t2 (x7)	0x00000000	
s0 (x8)	0x00000000	
s1 (x9)	0x00000000	
a0 (x10)	0x00000001	
a1 (x11)	0x7FFFFFFD	
a2 (x12)	0x00000000	
a3 (x13)	0x00000000	
a4 (x14)	0x00000000	

Display Settings Hex

4.b O conteúdo do registrador que armazena o valor do fatorial (a0) é 0x00000001

Registers	
Integer (R) Floating (F)	
zero	0x00000000
ra (x1)	0x00000000
sp (x2)	0x7FFFFFFDC
gp (x3)	0x10000000
tp (x4)	0x00000000
t0 (x5)	0x00000000
t1 (x6)	0x00000000
t2 (x7)	0x00000000
s0 (x8)	0x00000000
s1 (x9)	0x00000000
a0 (x10)	0x00000001
a1 (x11)	0x7FFFFFFDC
a2 (x12)	0x00000000
a3 (x13)	0x00000000
a4 (x14)	0x00000000

Display Settings Hex

5.a O conteúdo do registrador que armazena o valor de n (a2) é 0x00000005

Registers	
Integer (R) Floating (F)	
zero	0x00000000
ra (x1)	0x00000054
sp (x2)	0x7FFFFFFDC
gp (x3)	0x10000000
tp (x4)	0x00000000
t0 (x5)	0x00000001
t1 (x6)	0x00000000
t2 (x7)	0x00000000
s0 (x8)	0x00000000
s1 (x9)	0x00000000
a0 (x10)	0x00000078
a1 (x11)	0x7FFFFFFDC
a2 (x12)	0x00000005
a3 (x13)	0x00000000
a4 (x14)	0x00000000

5.b O conteúdo do registrador que armazena o valor do fatorial (a0) é 0x00000078

Registers	
Integer (R) Floating (F)	
zero	0x00000000
ra (x1)	0x00000054
sp (x2)	0x7FFFFFFDC
gp (x3)	0x10000000
tp (x4)	0x00000000
t0 (x5)	0x00000001
t1 (x6)	0x00000000
t2 (x7)	0x00000000
s0 (x8)	0x00000000
s1 (x9)	0x00000000
a0 (x10)	0x00000078
a1 (x11)	0x7FFFFFFDC
a2 (x12)	0x00000005
a3 (x13)	0x00000000
a4 (x14)	0x00000000

PROBLEMA 2

2. Os valores encontrados foram

Registers Memory Cache VDB	
Cache Levels	1
Block Size (Bytes)	4
Number of Blocks	2
Associativity	1
Cache Size (Bytes)	8
Enable?	Enables current selected level of the cache.
Direct Mapped	
LRU	L1
Hit Count	2
Accesses	20
Hit Rate	0.1
0) MISS 0) MISS	
NOTE: This is a write through, write allocate cache.	
Seed	-2673334269648431485

Display Settings Hex

5. Os valores encontrados foram

Registers Memory Cache VDB	
Cache Levels	1
Block Size (Bytes)	8
Number of Blocks	2
Associativity	1
Cache Size (Bytes)	16
Enable?	Enables current selected level of the cache.
Direct Mapped	
LRU	L1
Hit Count	10
Accesses	20
Hit Rate	0.5
0) HIT 0) MISS	
NOTE: This is a write through, write allocate cache.	
Seed	-2673334269648431485

Display Settings Hex

Com base nos resultados, podemos observar que houve um aumento no “Hit count” e o “Hit rate”. Com o mesmo número de acessos à memória cache, conseguimos aumentar a taxa de acerto para a metade ao aumentar o tamanho dos blocos.

8. Os valores encontrados foram

Registers

Memory

Cache

VDB

Cache Levels	1
Block Size (Bytes)	8
Number of Blocks	8
Associativity	1
Cache Size (Bytes)	64
<div>Enable?</div>	Enables current selected level of the cache.
Direct Mapped	▼
LRU	▼
L1	▼
Hit Count	14
Accesses	20
Hit Rate	0.7
<div>0) HIT</div> <div>1) HIT</div> <div>2) HIT</div> <div>3) HIT</div> <div>4) EMPTY</div> <div>5) EMPTY</div> <div>6) HIT</div> <div>7) HIT</div>	
NOTE: This is a write through, write allocate cache.	
Display Settings	Hex ▼

Quando aumentamos tanto o tamanho dos blocos quanto sua quantidade, temos um aumento expressivo na taxa de acerto na memória cache. A princípio, quando tínhamos somente dois blocos de 2 bytes, a taxa de acerto era de apenas 0.1. Isso significa que 90% dos acessos à memória cache precisavam acessar a memória principal para buscar as informações. Agora, com 8 blocos de 8 bytes cada, a taxa de acerto subiu para 0.7. Com isso, somente foi preciso acessar a memória principal 30% das vezes.