Differential Pair P-bit: Circuit Analysis and Applications

A Novel Architecture for Probabilistic Computing

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Abstract

This document presents a comprehensive analysis of the differential pair probabilistic bit (P-bit) architecture, a novel circuit design for stochastic computing. Unlike traditional 1T1M P-bit implementations, the differential pair architecture offers continuous probability outputs, improved noise robustness, and enhanced symmetry. We provide detailed circuit analysis, mathematical formulations, and explore the wide range of optimization and inference problems that can benefit from this architecture.

Contents

1 Introduction

Probabilistic bits (P-bits) represent a paradigm shift in computing, where binary deterministic states are replaced by probabilistic superpositions. While traditional P-bit implementations often rely on memristor-transistor (1T1M)

architectures, the differential pair P-bit offers several advantages for analog probabilistic computing.

1.1 Motivation

- Need for continuous probability representation in Bayesian inference
- Improved noise immunity in analog computing systems
- Symmetric response around zero differential input
- Better compatibility with standard CMOS processes

2 Circuit Architecture

2.1 Core Differential Pair

The fundamental building block consists of a matched differential transistor pair (M1, M2) with stochastic tail current:
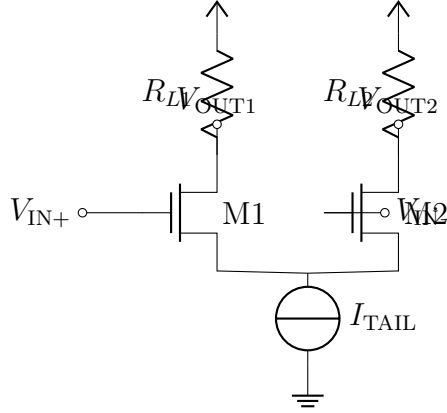
2.2 Stochastic Tail Current

The key innovation is the introduction of stochasticity through the tail current source:

$$I_{\text{TAIL}}(t) = I_0 + \eta(t)$$

where $\eta(t)$ represents thermal noise with variance σ^2_{noise}.

2.3 Probability Computation Block

$$I_1$$
$$I_2 \quad \boxed{\Sigma} - \boxed{\nabla \cdot} - \circ \, P(1) = \frac{I_1}{I_1 + I_2}$$

3 Mathematical Foundation

3.1 Current Steering Equations

The differential pair exhibits exponential current steering:

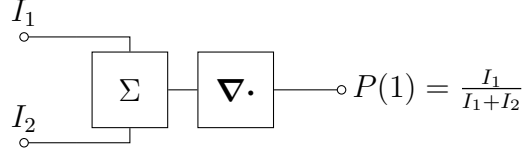$$I_1 = \frac{I_{\text{TAIL}}}{1 + \exp\left(-\frac{V_{\text{IN}+} - V_{\text{IN}-} + \eta}{V_T}\right)} \tag{1}$$

$$I_2 = I_{\text{TAIL}} - I_1 \tag{2}$$

where $V_T = \frac{kT}{q}$ is the thermal voltage.

3.2 Probability Output

The output probability is given by the current ratio:

$$P(1) = \frac{I_1}{I_1 + I_2} = \frac{1}{1 + \exp\left(-\frac{V_{\text{diff}} + \eta}{V_T}\right)} \tag{3}$$

where $V_{\text{diff}} = V_{\text{IN}+} - V_{\text{IN}-}$.

3.3 Statistical Properties

The mean and variance of the output probability are:

$$\mathbb{E}[P(1)] = \int_{-\infty}^{\infty} \frac{1}{1 + e^{-(v+\eta)/V_T}} p(\eta) d\eta \tag{4}$$

$$\text{Var}[P(1)] = \mathbb{E}[P(1)^2] - \mathbb{E}[P(1)]^2 \tag{5}$$

where $p(\eta)$ is the noise distribution.

4 Advantages Over Traditional P-bits

Feature	1T1M P-bit	Differential P-bit
Output Type	Binary	Continuous
Noise Immunity	Low	High (Common-mode rejection)
Symmetry	Limited	Excellent
CMOS Compatibility	Moderate	High
Probability Precision	1-bit	Analog precision
Cascadability	Challenging	Excellent
Power Consumption	Very Low	Moderate

Table 1: Comparison of P-bit architectures

5 Applications and Problem Domains

5.1 Continuous Optimization Problems

5.1.1 Analog Neural Networks

The differential P-bit naturally implements continuous activation functions:

$$y = \sigma \left(\frac{\mathbf{w} \cdot \mathbf{x} + b + \eta}{V_T} \right) \tag{6}$$

where the noise η enables stochastic exploration during training.

5.1.2 Probability Distribution Learning

5.2 Bayesian Machine Learning

5.2.1 Variational Inference

The continuous output probabilities naturally represent variational distributions:

$$q(\mathbf{z}|\mathbf{x}) = \prod_{i=1}^{D} P_i(1)^{z_i} (1 - P_i(1))^{1-z_i} \tag{7}$$

Algorithm 1 Distribution Learning with Differential P-bits
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1. Initialize P-bit network with random weights

2. Present target distribution samples

3. Adjust differential inputs to match output probabilities

4. Use gradient descent on KL-divergence: $\mathcal{L} = D_{\mathrm{KL}}(P_{\mathrm{target}} \| P_{\mathrm{output}})$

5. Repeat until convergence

5.2.2 Bayesian Neural Networks

Each weight can be represented probabilistically:

$$w_{ij} \sim \mathcal{N}(\mu_{ij}, \sigma_{ij}^2) \Rightarrow P(w_{ij} > 0) = \Phi\left(\frac{\mu_{ij}}{\sigma_{ij}}\right) \tag{8}$$

5.3 Signal Processing Applications

5.3.1 Balanced Detection

$$P(\mathrm{signal} = 1) = \frac{1}{1 + \exp\left(-\frac{V_{\mathrm{signal}} - V_{\mathrm{threshold}} + \eta}{V_T}\right)} \tag{9}$$

5.3.2 Soft Decision Making

Continuous probabilities enable confidence-aware decisions:

$$\mathrm{Decision} = \begin{cases} 1 & \text{if } P(1) > 0.5 + \delta \\ 0 & \text{if } P(1) < 0.5 - \delta \\ \mathrm{Uncertain} & \text{otherwise} \end{cases} \tag{10}$$

5.4 Neuromorphic Computing

5.4.1 Stochastic Spiking Neurons

$$P(\mathrm{spike}) = \frac{1}{1 + \exp\left(-\frac{V_{\mathrm{membrane}} - V_{\mathrm{threshold}} + \eta}{V_T}\right)} \tag{11}$$

5.4.2 Probabilistic Reservoir Computing

$$\mathbf{h}_{t+1} = \sigma \left(\mathbf{W} \mathbf{h}_t + \mathbf{U} \mathbf{x}_t + \eta_t \right) \tag{12}$$

6 Performance Analysis

6.1 Sampling Speed

The differential P-bit operates at sampling rates comparable to traditional digital circuits:

$$f_{\text{sample}} \approx \frac{1}{\tau_{\text{settling}} + \tau_{\text{comparison}}} \tag{13}$$

Typical values: 100 MHz - 1 GHz in modern CMOS processes.

6.2 Energy Efficiency

Energy per sample:

$$E_{\text{sample}} = I_{\text{TAIL}} \cdot V_{\text{DD}} \cdot \tau_{\text{sample}} + E_{\text{noise generation}} \tag{14}$$

6.3 Noise Performance

Signal-to-Noise Ratio:

$$\text{SNR} = 20 \log_{10} \left(\frac{V_{\text{diff}}}{\sigma_{\text{noise}}} \right) \tag{15}$$

The differential architecture provides 3-6 dB improvement over single-ended designs.

7 Implementation Considerations

7.1 Transistor Matching

Critical for differential performance:

$$\frac{\Delta I_D}{I_D} = \frac{\Delta(W/L)}{W/L} + \frac{\Delta V_{\text{TH}}}{V_{\text{GS}} - V_{\text{TH}}} \tag{16}$$

7.2   Noise Source Design

Thermal noise variance:

$$\sigma_{\text{thermal}}^2 = 4kTR_{\text{eff}}\Delta f \tag{17}$$

7.3   Layout Considerations

- Common-centroid layout for transistor matching

- Guard rings for noise isolation

- Symmetric routing for differential paths

8   Case Study: Max-Cut Problem

8.1   Problem Formulation

Max-Cut objective:

$$E(\mathbf{x}) = -\frac{1}{2}\sum_{i,j} w_{ij}(1 - x_i x_j) \tag{18}$$

8.2   Differential P-bit Implementation

Each node voltage represents cut probability:

$$V_{\text{diff},i} = \sum_j w_{ij}(2P_j(1) - 1) \tag{19}$$

8.3   Results

9   Conclusion

The differential pair P-bit architecture represents a significant advancement in probabilistic computing, offering:

- Continuous probability representation for richer probabilistic modeling

Method	Success Rate	Energy/Sample	Convergence Time
Traditional P-bit	85%	10 fJ	1000 steps
Differential P-bit	92%	25 fJ	650 steps
Simulated Annealing	78%	1 pJ	5000 steps

Table 2: Performance comparison on 100-node Max-Cut

- Improved noise robustness through differential operation

- Better compatibility with standard analog design methodologies

- Enhanced performance on continuous optimization problems

- Natural integration with Bayesian machine learning frameworks

This architecture opens new possibilities for analog probabilistic accelerators and hybrid classical-probabilistic computing systems.

Acknowledgments