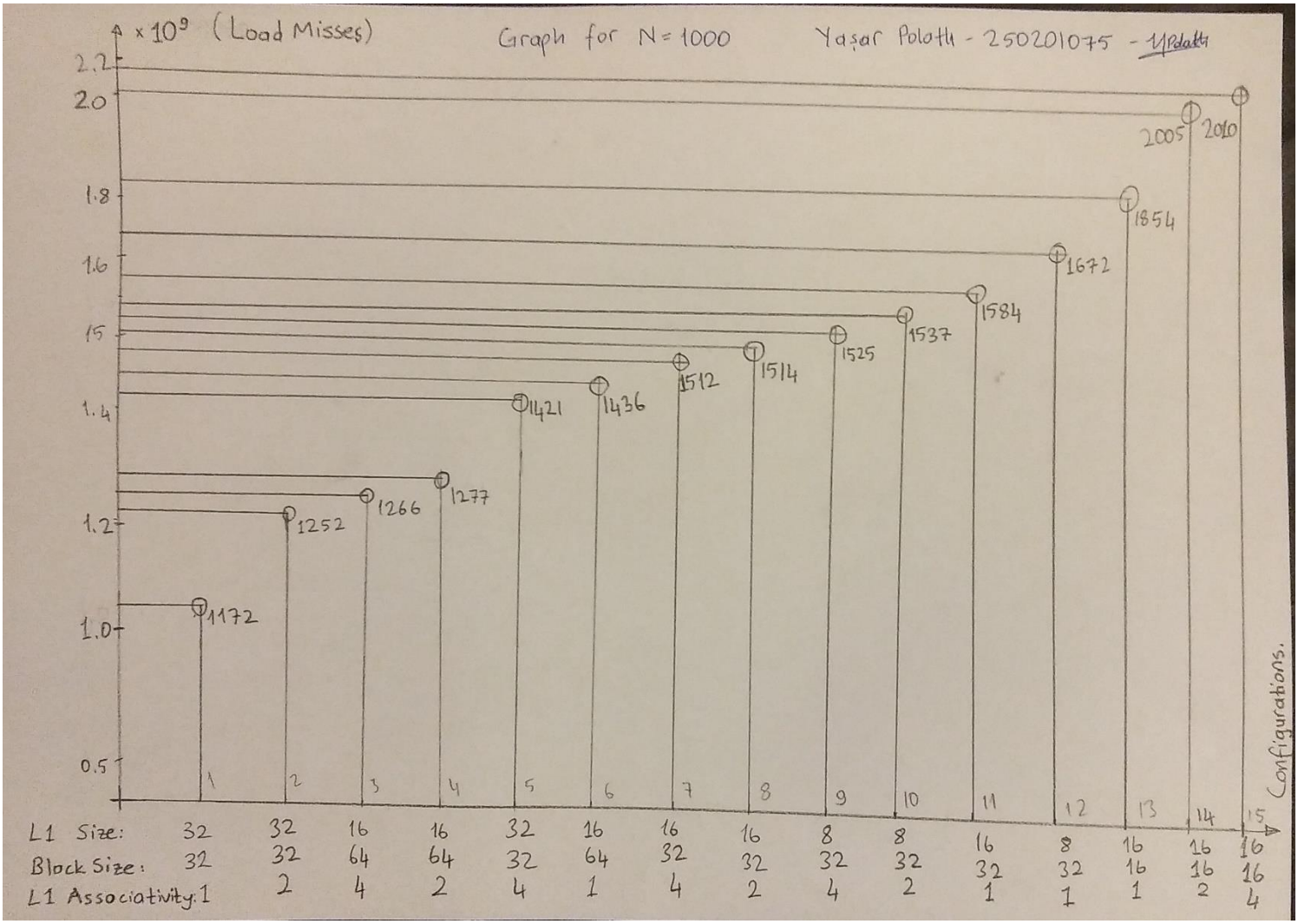
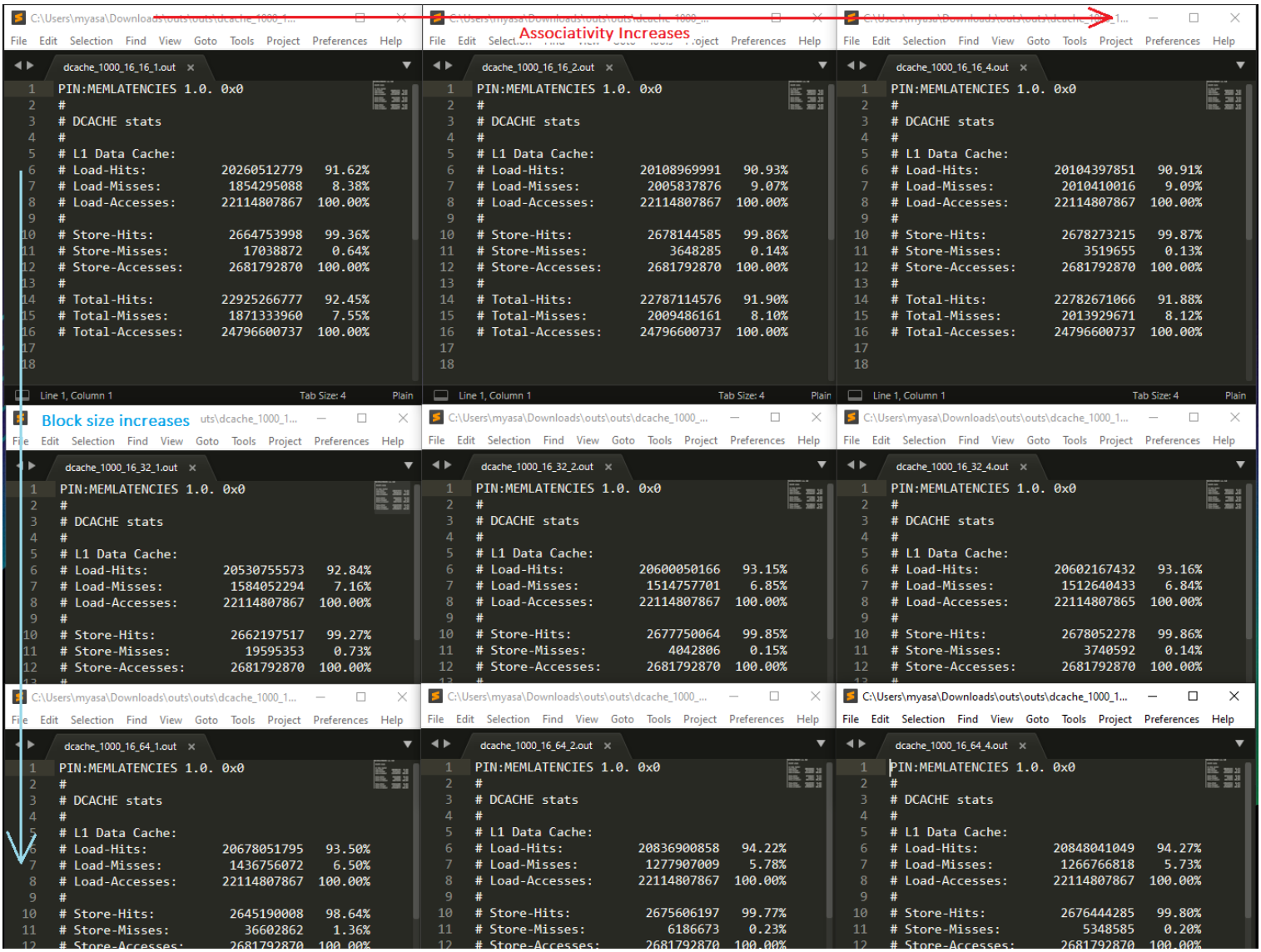
CENG311 Fall 2020

REPORT FOR PROGRAMMING ASSIGNMENT 4

Firstly, let us start the report with default matrix size (N=1000). Here is the graph that shows number of load-misses for L1 data cache:

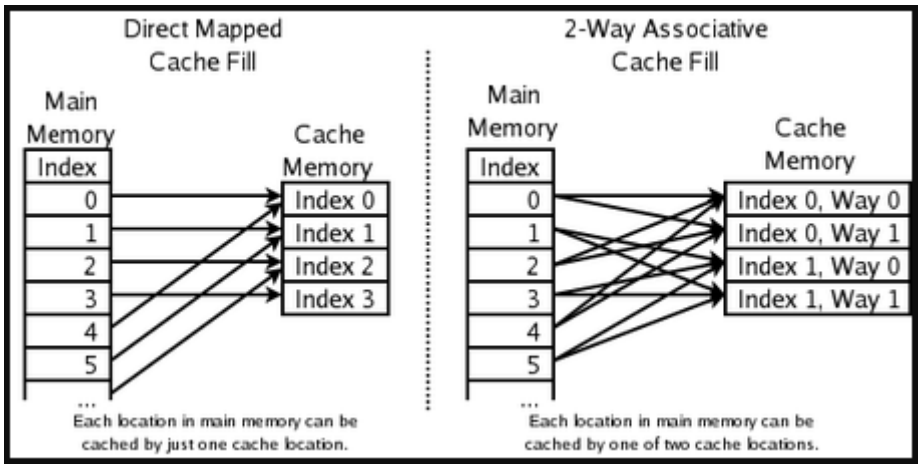


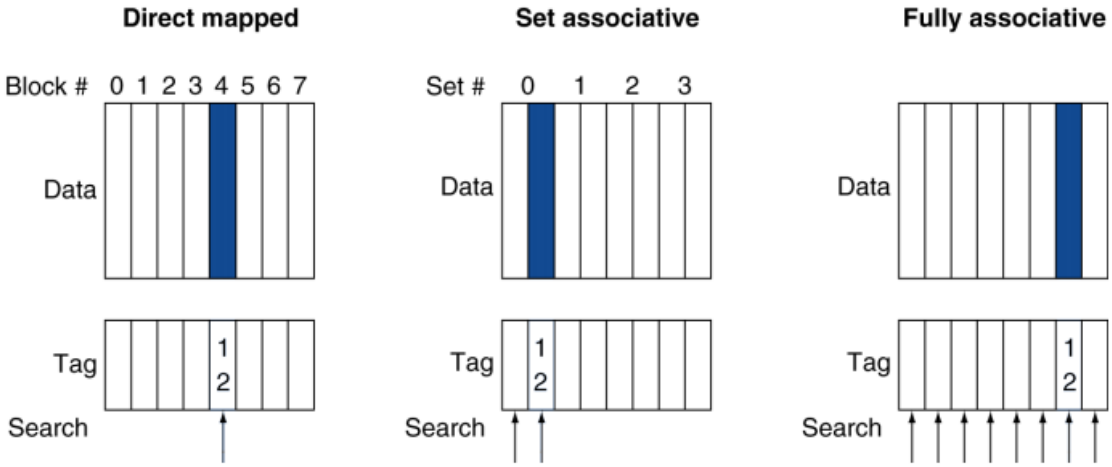
In order to comment the cache parameters differently let’s look at this image:



As you can see when the associativity becomes larger (red line), miss rate getting smaller. Because the associativity means more room for data (2 associativity means, 2 blocks for 1 data) to be placed. And it increases the hit rate, decreases the misses naturally.

Some pictures from lecturer materials that show what I try to explain:





Associativity allows a set of blocks to go in cache entries. When the one of block is full, data can be located another block which is element of the same set.

There is a coincidence to must indicate is that when the cache size and block size is equal (when they both are 16 or 32), miss rate is getting bigger with associativity. I am not sure, but this might happen because block size becomes a significant portion of the cache size (actually their size is equal) and we cached lots of values (N=1000) that we use just once.

When the cache size and block size are both small there is high miss rate is inevitable. To lower these misses associativity can be increased.

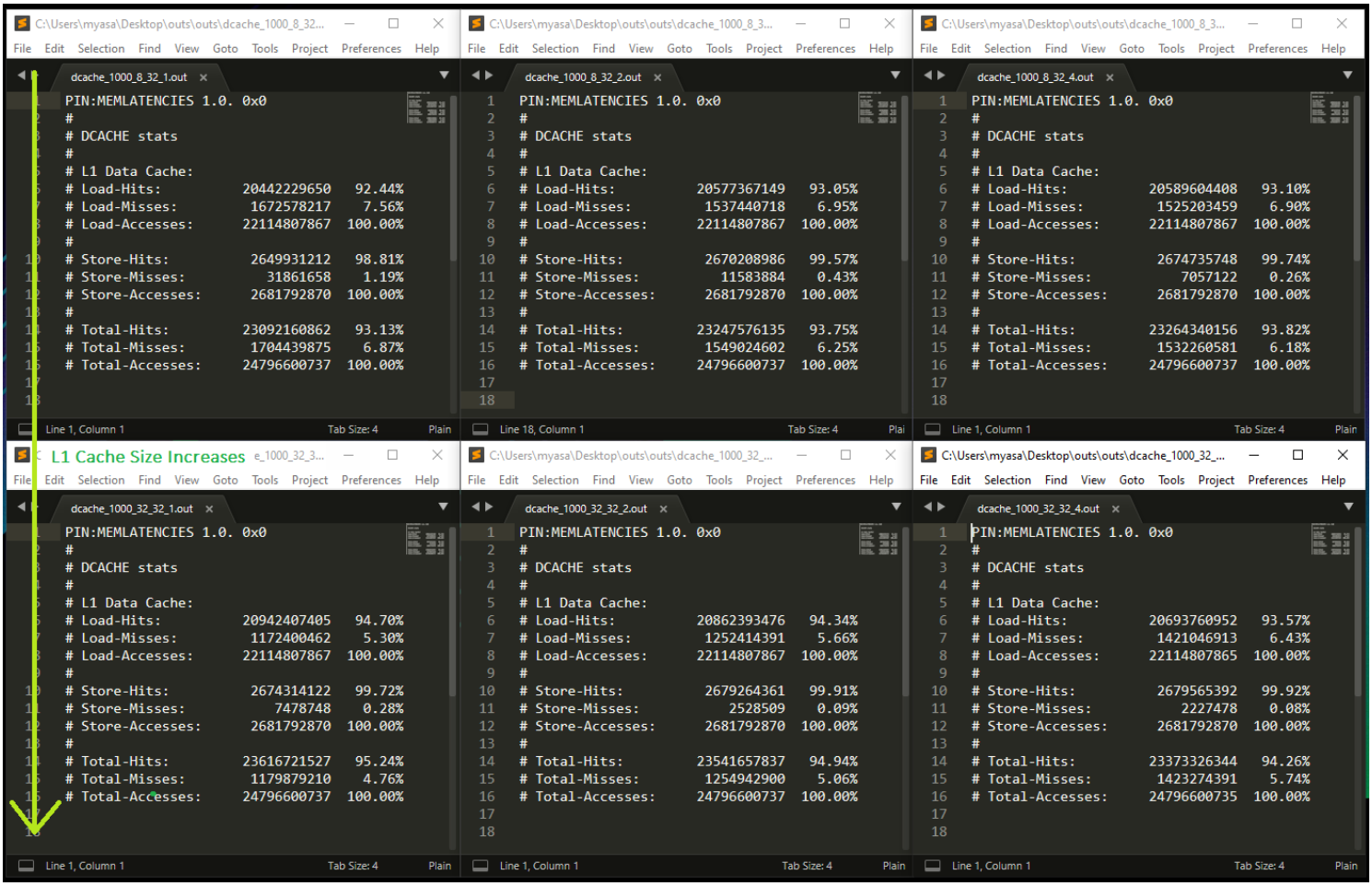
Second part of my commenting, I will explain block size differences.

When the block size is small, we cannot use spatial locality. This situation occurs more misses.

As you can see (blue line) when the block size increases, misses getting smaller.

And moreover, the block size matters a lot because the row-majority of matrix implementation. We can access continuous elements of matrix easily when the block size is bigger, due to spatial locality.

When we consider the different cache sizes about load misses let us look at this image:



As you can see when the cache size increases (green line), number of load-misses getting decrease. Because bigger cache size can exploit temporal locality better. There is a pros about miss rates, cons about latency for larger cache size but we are just focusing number of load-misses.

Secondly, let us check the results for another matrix size (N=10).

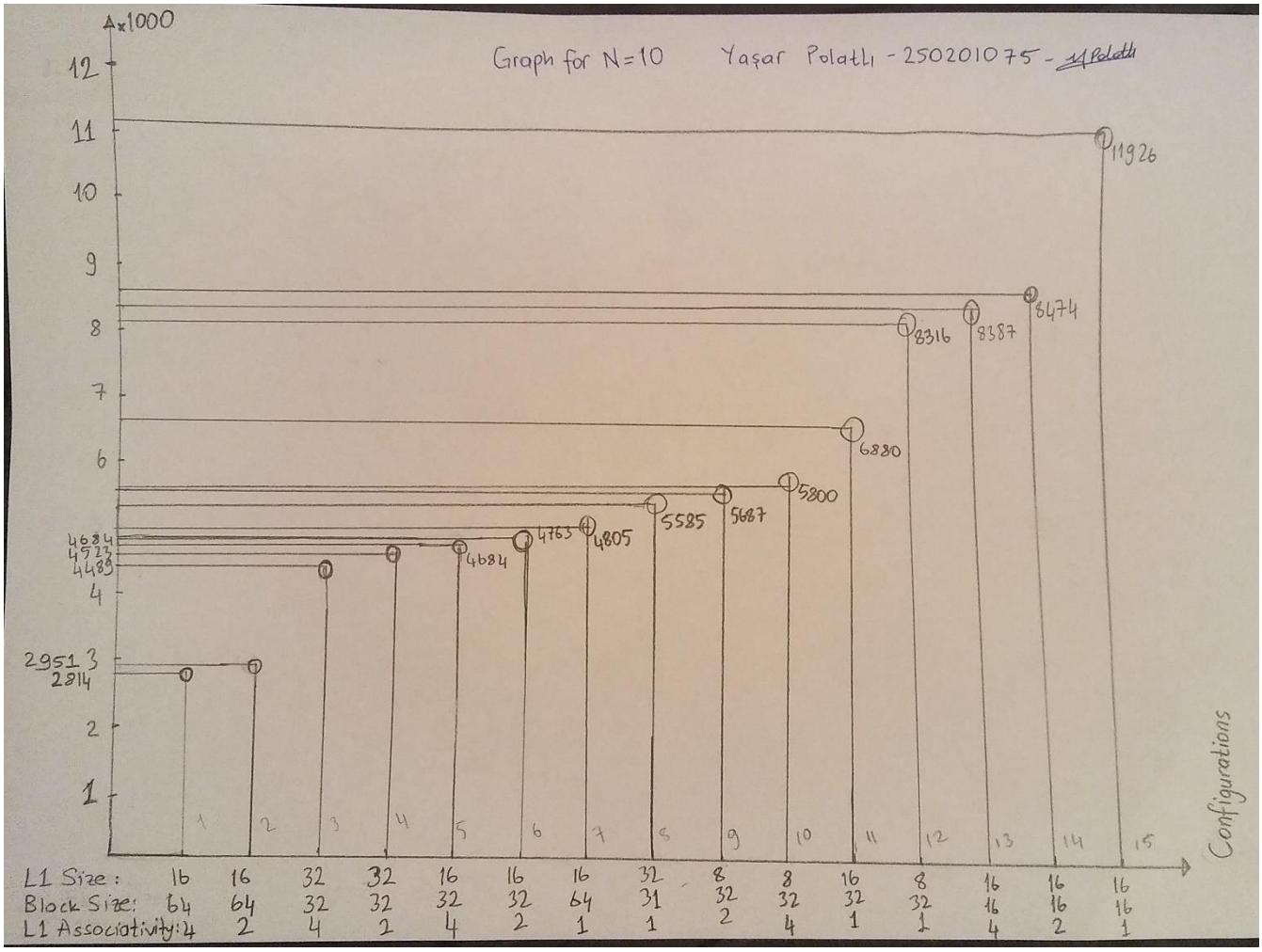
In this scenario there is not much difference that should be indicated.

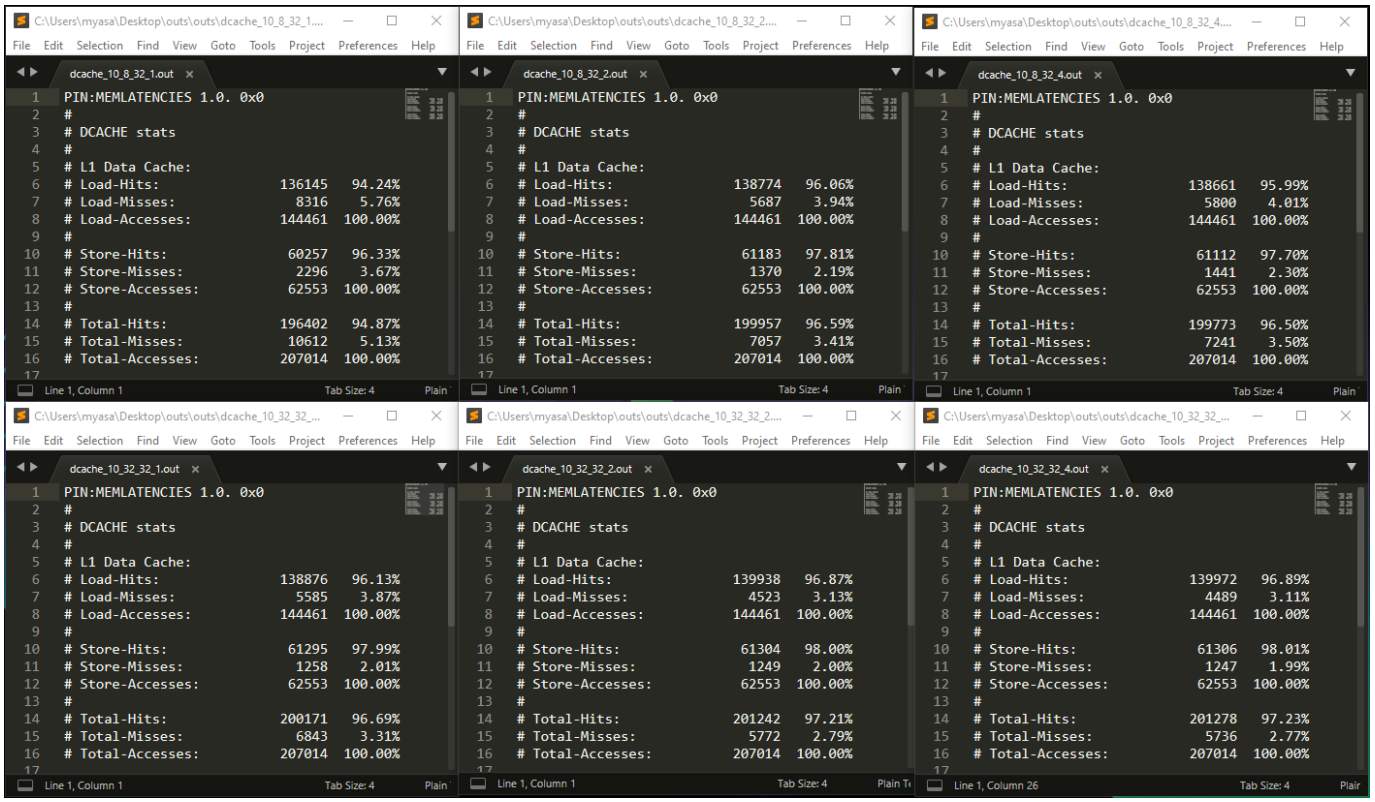
But some observations about like this:

- Since number of operations decreases miss rate is smaller than 1000. When the operation is data intensive (N=1000) there is lots of deletion operation occurs and this affects overall rate. But when the N=10 there is not much deletion needed so miss-rate (%) is smaller than before.
- There is no coincidence happening here since data intense is small.

Other than these, observations and comment would be the same with as N=1000.

Here is the values and the graph for N=10:





dcache_10_8_32_1.out

```
PIN:MEMLATENCIES 1.0. 0x0
#
# DCACHE stats
#
# L1 Data Cache:
# Load-Hits:              136145   94.24%
# Load-Misses:              8316    5.76%
# Load-Accesses:          144461  100.00%
#
# Store-Hits:              60257   96.33%
# Store-Misses:             2296    3.67%
# Store-Accesses:          62553  100.00%
#
# Total-Hits:             196402   94.87%
# Total-Misses:            10612    5.13%
# Total-Accesses:         207014  100.00%
```

dcache_10_8_32_2.out

```
PIN:MEMLATENCIES 1.0. 0x0
#
# DCACHE stats
#
# L1 Data Cache:
# Load-Hits:              138774   96.06%
# Load-Misses:              5687    3.94%
# Load-Accesses:          144461  100.00%
#
# Store-Hits:              61183   97.81%
# Store-Misses:             1370    2.19%
# Store-Accesses:          62553  100.00%
#
# Total-Hits:             199957   96.59%
# Total-Misses:             7057    3.41%
# Total-Accesses:         207014  100.00%
```

dcache_10_8_32_4.out

```
PIN:MEMLATENCIES 1.0. 0x0
#
# DCACHE stats
#
# L1 Data Cache:
# Load-Hits:              138661   95.99%
# Load-Misses:              5800    4.01%
# Load-Accesses:          144461  100.00%
#
# Store-Hits:              61112   97.70%
# Store-Misses:             1441    2.30%
# Store-Accesses:          62553  100.00%
#
# Total-Hits:             199773   96.50%
# Total-Misses:             7241    3.50%
# Total-Accesses:         207014  100.00%
```

dcache_10_32_32_1.out

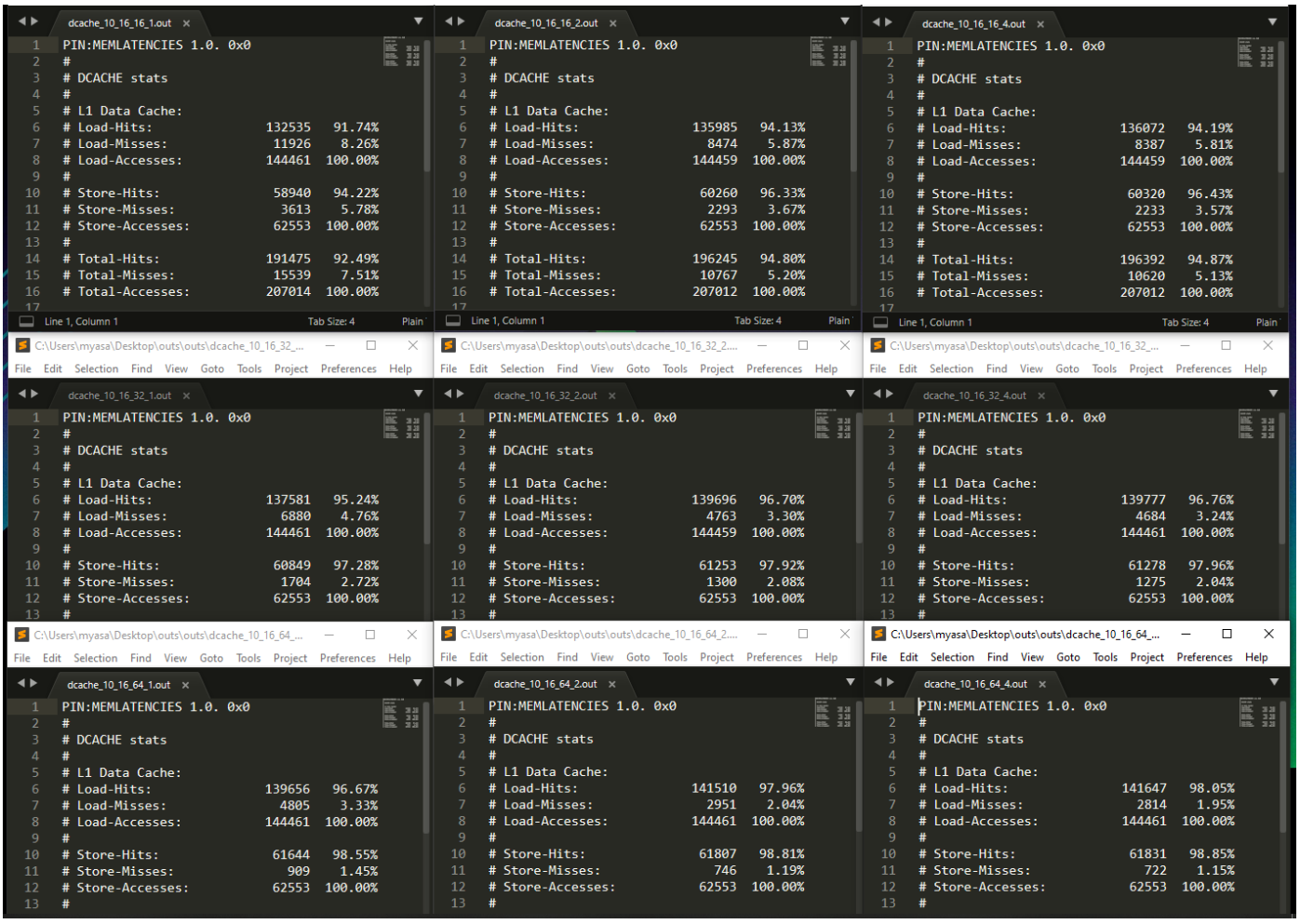
```
PIN:MEMLATENCIES 1.0. 0x0
#
# DCACHE stats
#
# L1 Data Cache:
# Load-Hits:              138876   96.13%
# Load-Misses:              5585    3.87%
# Load-Accesses:          144461  100.00%
#
# Store-Hits:              61295   97.99%
# Store-Misses:             1258    2.01%
# Store-Accesses:          62553  100.00%
#
# Total-Hits:             200171   96.69%
# Total-Misses:             6843    3.31%
# Total-Accesses:         207014  100.00%
```

dcache_10_32_32_2.out

```
PIN:MEMLATENCIES 1.0. 0x0
#
# DCACHE stats
#
# L1 Data Cache:
# Load-Hits:              139938   96.87%
# Load-Misses:              4523    3.13%
# Load-Accesses:          144461  100.00%
#
# Store-Hits:              61304   98.00%
# Store-Misses:             1249    2.00%
# Store-Accesses:          62553  100.00%
#
# Total-Hits:             201242   97.21%
# Total-Misses:             5772    2.79%
# Total-Accesses:         207014  100.00%
```

dcache_10_32_32_4.out

```
PIN:MEMLATENCIES 1.0. 0x0
#
# DCACHE stats
#
# L1 Data Cache:
# Load-Hits:              139972   96.89%
# Load-Misses:              4489    3.11%
# Load-Accesses:          144461  100.00%
#
# Store-Hits:              61306   98.01%
# Store-Misses:             1247    1.99%
# Store-Accesses:          62553  100.00%
#
# Total-Hits:             201278   97.23%
# Total-Misses:             5736    2.77%
# Total-Accesses:         207014  100.00%
```



dcache_10_16_16_1.out

```
PIN:MEMLATENCIES 1.0. 0x0
#
# DCACHE stats
#
# L1 Data Cache:
# Load-Hits:              132535   91.74%
# Load-Misses:             11926    8.26%
# Load-Accesses:          144461  100.00%
#
# Store-Hits:              58940   94.22%
# Store-Misses:             3613    5.78%
# Store-Accesses:          62553  100.00%
#
# Total-Hits:             191475   92.49%
# Total-Misses:            15539    7.51%
# Total-Accesses:         207014  100.00%
```

dcache_10_16_16_2.out

```
PIN:MEMLATENCIES 1.0. 0x0
#
# DCACHE stats
#
# L1 Data Cache:
# Load-Hits:              135985   94.13%
# Load-Misses:              8474    5.87%
# Load-Accesses:          144459  100.00%
#
# Store-Hits:              60260   96.33%
# Store-Misses:             2293    3.67%
# Store-Accesses:          62553  100.00%
#
# Total-Hits:             196245   94.80%
# Total-Misses:            10767    5.20%
# Total-Accesses:         207012  100.00%
```

dcache_10_16_16_4.out

```
PIN:MEMLATENCIES 1.0. 0x0
#
# DCACHE stats
#
# L1 Data Cache:
# Load-Hits:              136072   94.19%
# Load-Misses:              8387    5.81%
# Load-Accesses:          144459  100.00%
#
# Store-Hits:              60320   96.43%
# Store-Misses:             2233    3.57%
# Store-Accesses:          62553  100.00%
#
# Total-Hits:             196392   94.87%
# Total-Misses:            10620    5.13%
# Total-Accesses:         207012  100.00%
```

dcache_10_16_32_1.out

```
PIN:MEMLATENCIES 1.0. 0x0
#
# DCACHE stats
#
# L1 Data Cache:
# Load-Hits:              137581   95.24%
# Load-Misses:              6880    4.76%
# Load-Accesses:          144461  100.00%
#
# Store-Hits:              60849   97.28%
# Store-Misses:             1704    2.72%
# Store-Accesses:          62553  100.00%
#
```

dcache_10_16_32_2.out

```
PIN:MEMLATENCIES 1.0. 0x0
#
# DCACHE stats
#
# L1 Data Cache:
# Load-Hits:              139696   96.70%
# Load-Misses:              4763    3.30%
# Load-Accesses:          144459  100.00%
#
# Store-Hits:              61253   97.92%
# Store-Misses:             1300    2.08%
# Store-Accesses:          62553  100.00%
#
```

dcache_10_16_32_4.out

```
PIN:MEMLATENCIES 1.0. 0x0
#
# DCACHE stats
#
# L1 Data Cache:
# Load-Hits:              139777   96.76%
# Load-Misses:              4684    3.24%
# Load-Accesses:          144461  100.00%
#
# Store-Hits:              61278   97.96%
# Store-Misses:             1275    2.04%
# Store-Accesses:          62553  100.00%
#
```

dcache_10_16_64_1.out

```
PIN:MEMLATENCIES 1.0. 0x0
#
# DCACHE stats
#
# L1 Data Cache:
# Load-Hits:              139656   96.67%
# Load-Misses:              4805    3.33%
# Load-Accesses:          144461  100.00%
#
# Store-Hits:              61644   98.55%
# Store-Misses:              909    1.45%
# Store-Accesses:          62553  100.00%
#
```

dcache_10_16_64_2.out

```
PIN:MEMLATENCIES 1.0. 0x0
#
# DCACHE stats
#
# L1 Data Cache:
# Load-Hits:              141510   97.96%
# Load-Misses:              2951    2.04%
# Load-Accesses:          144461  100.00%
#
# Store-Hits:              61807   98.81%
# Store-Misses:              746    1.19%
# Store-Accesses:          62553  100.00%
#
```

dcache_10_16_64_4.out

```
PIN:MEMLATENCIES 1.0. 0x0
#
# DCACHE stats
#
# L1 Data Cache:
# Load-Hits:              141647   98.05%
# Load-Misses:              2814    1.95%
# Load-Accesses:          144461  100.00%
#
# Store-Hits:              61831   98.85%
# Store-Misses:              722    1.15%
# Store-Accesses:          62553  100.00%
#
```

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