King Abdulaziz University

Faculty of engineering

Digital 2

(EE460)

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Assignment three: 8-bit processor

Introduction:

The objective of this design assignment is to extend the functionality of a simple 8-bit processor by incorporating additional operations and increasing the number of registers. Specifically, the processor will be enhanced to support bitwise AND, OR, and XOR operations, as well as a store operation to output data from a register. Additionally, the number of registers will be expanded from 4 to 8, providing more flexibility and capability for data storage and manipulation, solving the problem of limited operations in the alu.

Top Level Design:

It shows the top-level design that includes a control module and Datapath module .

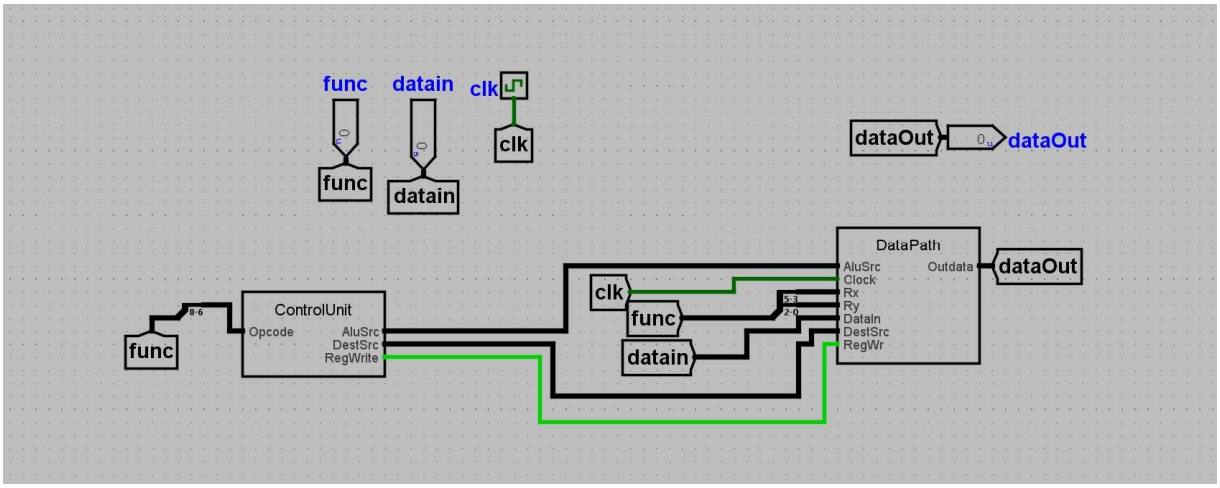

Figure 1 TOP LEVEL

Data path:

The data path includes alu, mux, file register and the operations are done in it.

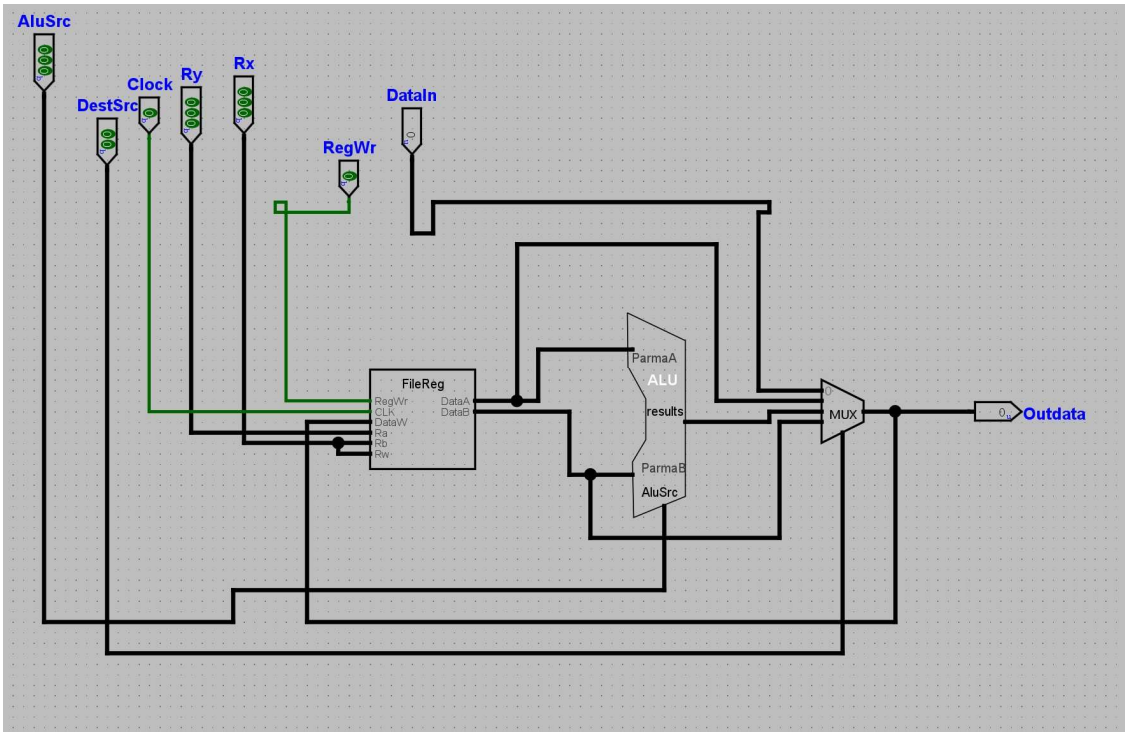

Figure 2 data path

Control:

The control module doses the operation to convert the machine code from the user to the actual operation the processor does it works as a translator.

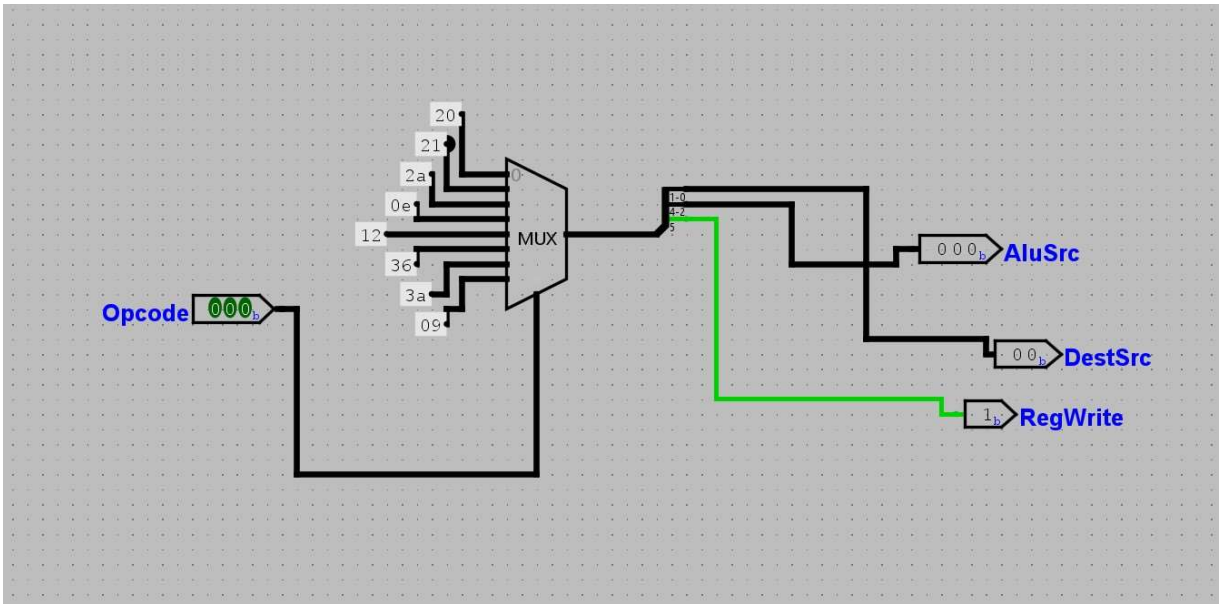

Figure 3 Control

Operation:

The operations instruction sheet shows the operation and what it does and how to use it and its machine code for the user to use it.

operation	opcode	Machine code	Description
load	000	000_000_xxx	Rx ← dataIn
move	001	001_000_000	Rx ← [Ry]
add	010	010_000_000	Rx ← [Rx] + [Ry]
sub	011	011_000_000	Rx ← [Rx] − [Ry]
and	100	100_000_000	Rx ← [Rx] & [Ry]
or	101	101_000_000	Rx ← [Rx] | [Ry]
xor	110	110_000_000	Rx ← [Rx]⊕[Ry]
store	111	111_000_xxx	Rx → dataOut

Figure 4 instruction sheet

Testing:

Accurate operations between registers with all the possible operations.

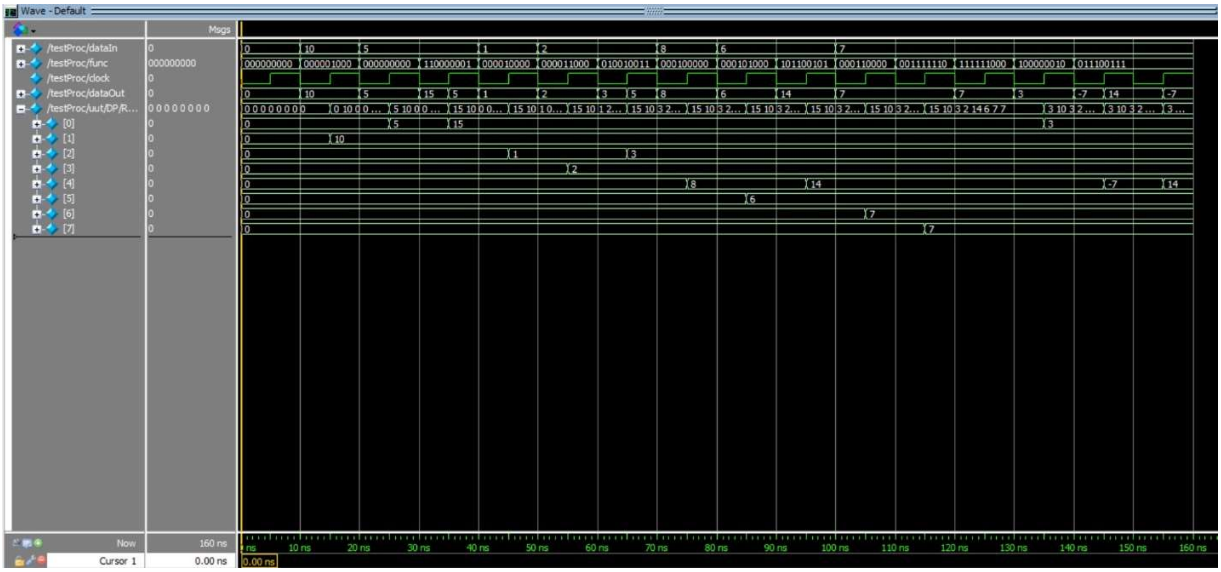

Figure 5 wave