Chanseung Lee

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• Education

Kyung Hee University, Republic of Korea

- B.S. in Applied Physics & Electronic Engineering 2023 – 2027 (expected)

• Research Interests

Developing semiconductor-based photonic integrated circuits for next-generation quantum computers.

- Silicon Photonics: Towards integrated optical computers with strain-engineered on-chip lasers

- Quantum Photonics: Towards integrated quantum processors with strain-engineered 2D quantum devices

• Research Experience

Q-SPIN Laboratory (Quantum semiconductor Photonic Integrated Lab), KAIST
Advisor: Professor **Donguk Nam** Research Intern, Dec 2025 – Feb 2026

- Modeling strain-engineered optical & quantum behavior

- Exploring integration strategies for on-chip optical quantum computing

• Projects

- Characterization and Parameter Extraction of Long- and Short-Channel MOSFETs [pdf]

Measured I–V characteristics using MS TECH probe station and CLARIUS software

Extracted Vt (ext/lin/sat), SS, Ioff, GIDL, DIBL, and gm

Analyzed long-channel vs short-channel behaviors and body-bias effects

Compared device scaling effects based on L = 10 μm and L = 0.35 μm transistors

- TCAD CMOS Process Simulation [pdf]

Built full NMOS process flow (oxidation → implantation → annealing → metallization)

Simulated ID–VG, ID–VD, Vth, gm, ro using Silvaco ATLAS, ATHENA

- Designing multistage Analog Amplifier using LTspice) [pdf]

Designed differential → gain → output stages - AC/DC/transient analysis and pole-zero extraction

• Skills

- TCAD (ATHENA, ATLAS)

- LTspice (analog IC design)

- Semiconductor device physics, photonics, 2D materials

- Semiconductor Fabrication, MEMS