Fall Semester 2025

Electronic Circuits 2 Design Results Report

Title: Multistage Amplifier Design

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1. Design Background

A. Originality/Creativity of the Design Work

The goal of this design is to implement a low-power MOSFET multistage amplifier that satisfies the given conditions. The final stage consists of a differential amplifier using a current-mirror active load, with the entire circuit comprising two high-gain amplification stages followed by the final output buffer. Requirements include a total voltage gain of 50dB or higher, a 3-dB bandwidth of 100Hz to 100kHz, an input resistance of 100kΩ or higher, a load resistance of 100Ω or lower, and total power consumption of 500mW or less.

This circuit first employs a high-gain two-stage configuration. The first stage uses a differential pair + current-mirror active load structure to achieve a large output resistance and high current gain. The second stage employs a common-source amplifier to provide additional voltage gain, raising the total open-loop gain to approximately 130dB. This design ensures the required closed-loop gain is sufficiently met even under relatively low supply voltage and bias current conditions.

Furthermore, a Wilson MOS current mirror structure is employed for the bias current source to significantly increase the output resistance and supply nearly ideal constant current to each amplification stage. This simultaneously ensures the gain and linearity of both amplification stages while maintaining a relatively stable operating point against process and temperature variations.

Finally, a source follower is placed at the final output stage. This ensures that the output voltage swing and drive capability are maintained even when a very small load resistance, on the order of 100Ω , is connected. In summary, this multistage amplifier aims to simultaneously achieve very high voltage gain and output swing relative to its low power input, while maintaining a low bias current level of tens of μA and low power consumption of tens of mW.

B. Expected Effects

This design is expected to deliver the following benefits. First, by achieving sufficiently high voltage gain and the required bandwidth, it can amplify small differential inputs ranging from tens of microvolts to tens of millivolts up to several volts. Consequently, it can serve as a fundamental analog building block for various applications, including sensor signal conditioning for low-level sensor signals, measurement frontends, and audio-band signal processing.

Additionally, thanks to the differential structure, current-mirror active load, and current-source bias, it exhibits low sensitivity to supply/temperature variations and strong common-mode noise immunity. By employing a source follower at the output stage to significantly reduce output resistance, the amplifier maintains its output voltage swing and drive capability even with very low load resistances around 100Ω. Furthermore, even when additional external circuits are connected in parallel, voltage drop and distortion remain relatively small. This is a highly advantageous characteristic in actual system-level design.

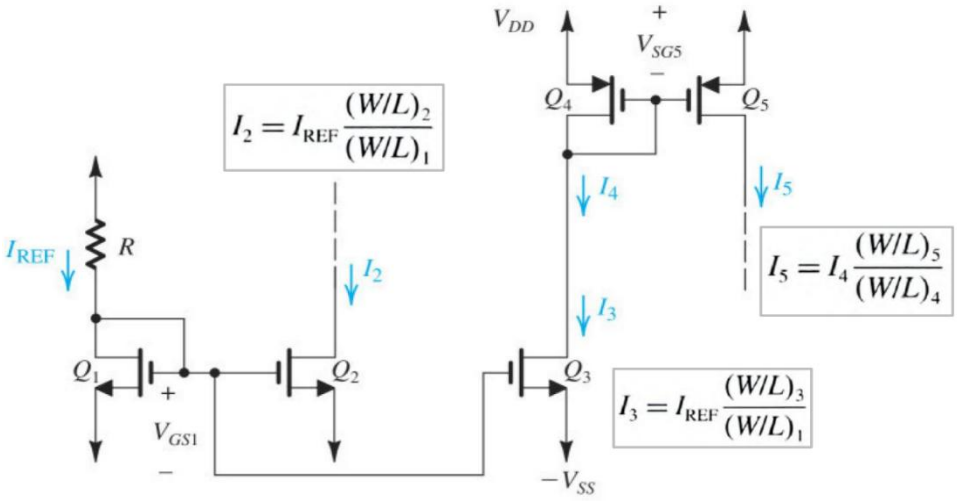
In terms of power consumption, this circuit operates at a supply voltage of 5V and a current consumption of approximately 12mA, resulting in a total power consumption of about 60mW. This comfortably meets the 500mW limit specified in the project requirements. Therefore, it is a suitable structure for application in portable devices or battery-powered low-power/small-form-factor systems.

Finally, this circuit incorporates all fundamental blocks of analog IC design, including differential pairs, current mirrors, Wilson current mirrors, and source followers. The entire design-simulation-verification process was performed using LTspice and an actual CMOS process model. This provides practical design experience and a foundation for future expansion into OPAMP or more complex multistage analog circuit design, offering significant educational value.

2. Theory and Design Results

A. Theory

<Current Mirror>



<Figure 1>

Figure 1 shows the circuit illustrating the basic operation of a MOS current mirror. The left transistor Q1 is used as a diode-connected MOSFET. The reference current (I_{REF}) is set by the resistor R and the supply voltage. At this point, Q1 has its gate and drain shorted together. This allows a current (I_{REF}) to flow, establishing the gate-source voltage (V_{GS1}). This circuit utilizes the characteristic of MOSFETs: transistors with the same process technology and the same drain-source resistance (W/L) will have the same drain-source voltage (V_{GS}) and thus carry the same current.
Since the gates of Q1 and Q2 are connected, Q2 also has the sameV_{GS1} as Q1. Assuming both transistors operate in the saturation region, the drain current is given by

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2$$

is given by, so the current ratio between Q1 and Q2, ignoring channel length modulation, is

$$I_2 = I_{REF}\frac{(W/L)_2}{(W/L)_1}$$

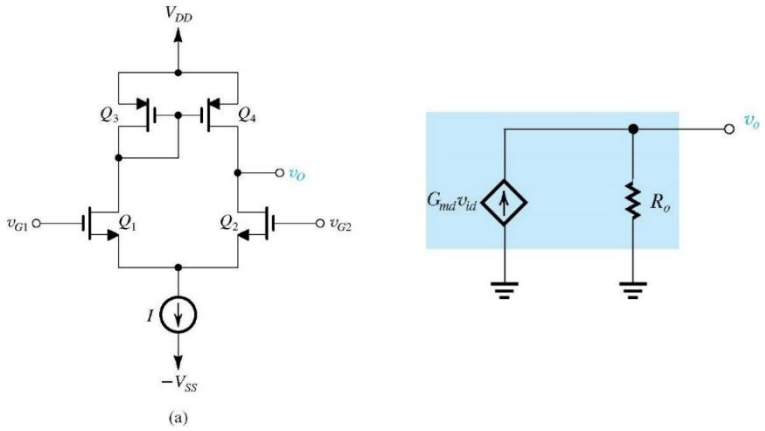
That is, by adjusting theW/L ratio of the two devices, an output currentI_2 of the desired magnitude can be obtained. This is the fundamental principle of the current mirror.

In the right circuit, the same principle is used to replicate current across multiple branches. Q3 receives a reference current in the same manner as Q1 and generates a mirrored currentI_3 in another direction (e.g., the negative power supply side). This current is then transmitted to the upper PMOS transistors Q4 and Q5, forming multiple current sources as shown inI_4, I_5 . Here, the current in each branch is determined by

$$I_3 = I_{REF}\frac{(W/L)_3}{(W/L)_1}, I_5 = I_4\frac{(W/L)_5}{(W/L)_4}$$

determined by the ratioW/L . This structure enables the creation of multiple nearly ideal constant current sources using only a single reference current. It is widely used in analog ICs for bias circuits, tail currents in differential pairs, active loads, and similar applications.

<fully differential amplifier>



<Figure 2>

The circuit in Figure 2 is a single-ended differential amplifier composed of an NMOS differential pair (Q1, Q2), a PMOS current-mirror active load (Q3, Q4), and a tail current source I at the bottom. The tail current I is always maintained constant, and the input differential voltage

$$v_{id} = v_{G1} - v_{G2}$$

$I/2 \pm \Delta I$. This current difference flows through the upper current mirror (Q3, Q4) to one output node (v_o), generating a large voltage gain.

From a small-signal perspective, the equivalent circuit for the differential input can be represented as a parallel combination of a current source$G_{md}v_{id}$ and an output resistorR_o (right diagram). Here,

$$A_{dm} = \frac{v_o}{v_{id}} \approx G_{md}R_o$$

The differential-mode gain is given by:G_{md} where is the sum of the transconductances (gm) of Q1 and Q2 or a similar value.R_o becomes a large value resulting from the parallel combination of the ro values of the upper and lower transistors. Due to the current-mirror active load, the output resistance becomes much larger than that of a simple resistor load, allowing a higher voltage gain to be achieved for the same gm.

Meanwhile, when the same common-mode signal is applied to both inputs, in the ideal case, identical currents flow through both sides of the differential pair, and symmetry is maintained in the mirror load. Consequently, almost no change occurs in the output node current. That is, the gain-A_c s for common-mode signals are very small, and accordingly,

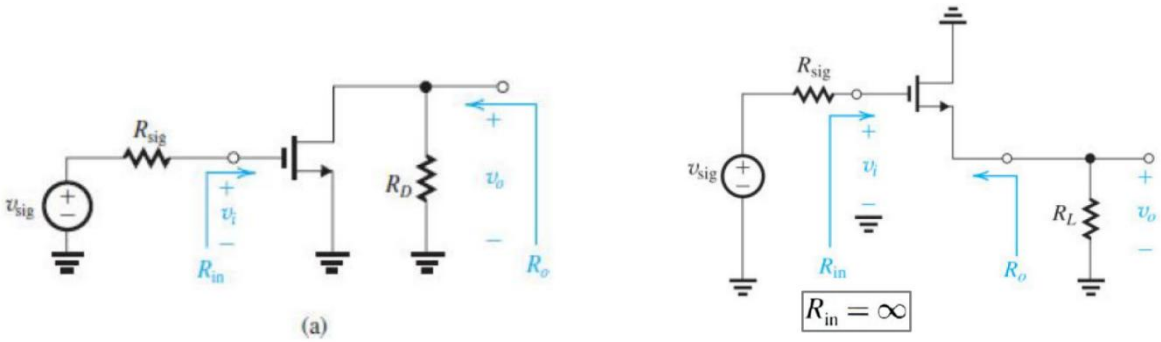
$$\text{CMRR} = \left| \frac{A_{dm}}{A_c} \right|$$

This becomes significant. Designing the tail current as an ideal constant current source and carefully matching Q1–Q4

further improves the CMRR.

In summary, this structure achieves high differential gain, large output resistance, and excellent CMRR simultaneously, thanks to the current-mirror active load and tail current source. Consequently, it is widely used as the first stage in multistage amplifiers.

<Common-source amplifier, source follower>



<Figure 3: Left: Common Source Amplifier, Right: Source Follower>

The left diagram shows a common source (CS) amplifier. The input signalv_{sig} is applied to the gate, the source is fixed to AC ground, and the drain is connected to a resistorR_D . In the small-signal model, the gate current is nearly zero, so the input resistanceR_{in} becomes theoretically very large. The small-signal gain of the CS amp is

$$A_v = \frac{v_o}{v_i} \approx -g_m R_D'$$

(whereR_D' is the parallel resistance ofR_D and the transistorr_o). Since the sign is negative, phase inversion occurs. Therefore, the CS configuration is the fundamental amplifier primarily used when high voltage gain is desired. However, because the output is at the drain node, the output resistanceR_o is relatively large, making it unsuitable for directly driving heavy (low-resistance) loads.

The diagram on the right shows a source follower (SF, common drain amplifier). The input is applied to the gate, the output is connected to the source, and the drain is connected to the power supply. The small-signal gain is

$$A_v \approx \frac{v_o}{v_i} \approx \frac{g_m R_L'}{1 + g_m R_L'} \approx 1$$

(whereR_L' is the parallel combination of the load andr_o). It ideally acts as a non-inverting buffer with a gain close to 1. Since the gate is isolated, the input resistance is very high ($R_{in} \approx \infty$). On the source side, the resistance seen is relatively low ($1/g_m$), resulting in a low output resistance. Consequently, the SF has almost no gain but is used as an output buffer that drives a low-impedance load while passing the preceding signal almost unchanged.

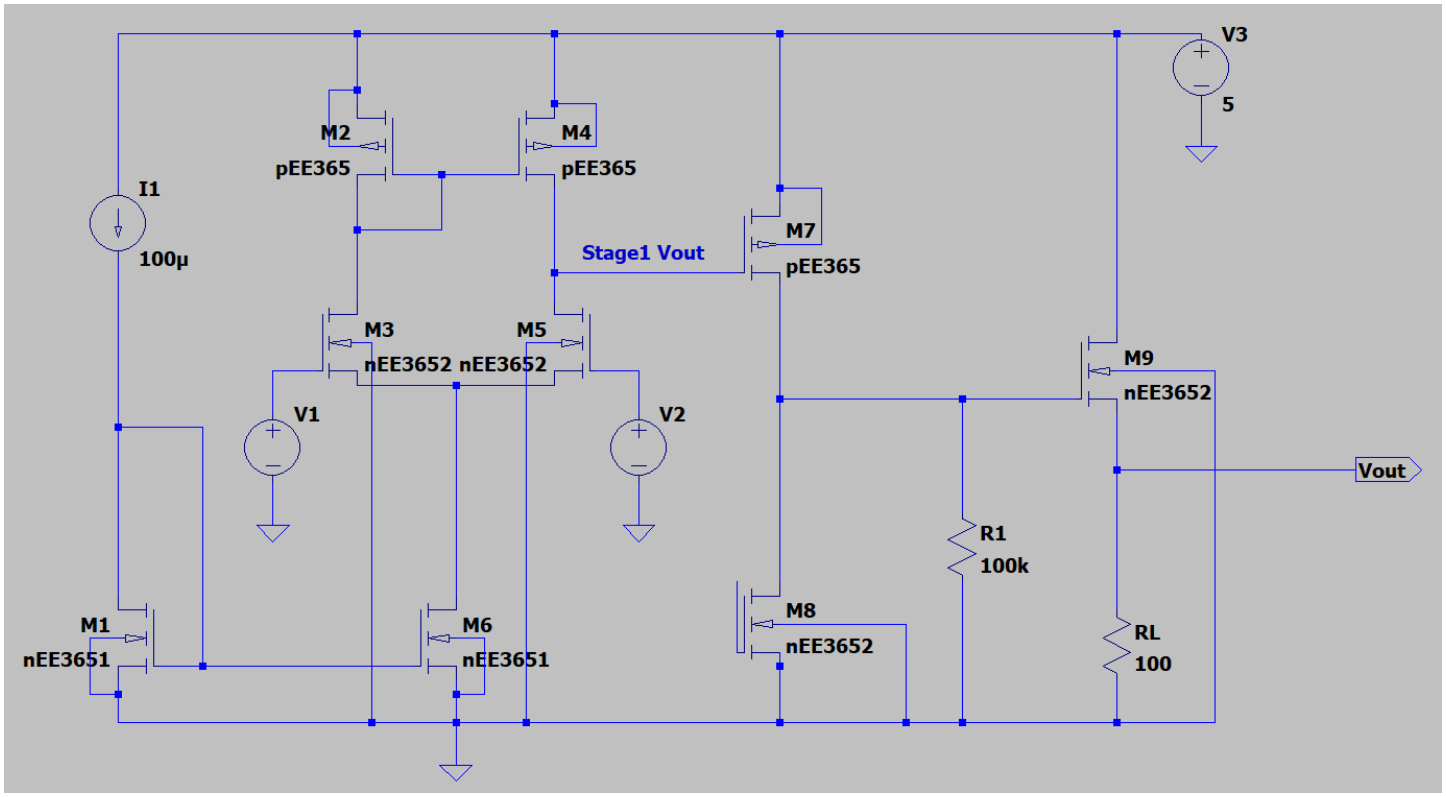
To summarize, the CS amplifier is a basic amplification structure that provides high gain, while the source follower is a buffer with a large output-to-input ratio (R_{in}) and a small input-to-output ratio (R_o). It is used as the final output stage in multistage amplifiers. By appropriately combining these two structures, it is possible to simultaneously achieve high gain and good load driving capability.

This is also why a source follower is typically placed as the final stage in multistage amplifiers. The large voltage gain generated by the preceding CS stages is preserved, while the final SF stage absorbs external load variations with its

smallR_o . Consequently, even when a heavy load is connected, the operating point and gain of the preceding stages remain largely unaffected. In other words, the SF provides load isolation and drive capability, simultaneously improving the entire circuit's linearity, stability, and output swing. This makes it the most suitable structure for the final output stage.

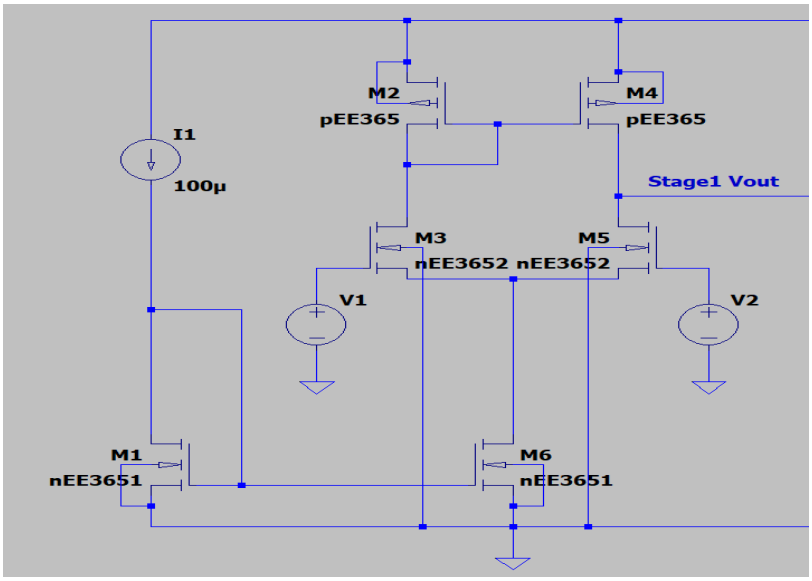
B. Concept Diagram or Operational Description of Each Circuit

<Overall Circuit Diagram> **The operating point is set so that all MOSFETs operate in the saturation region.**



<Figure 4>

<Stage 1 Diagram>

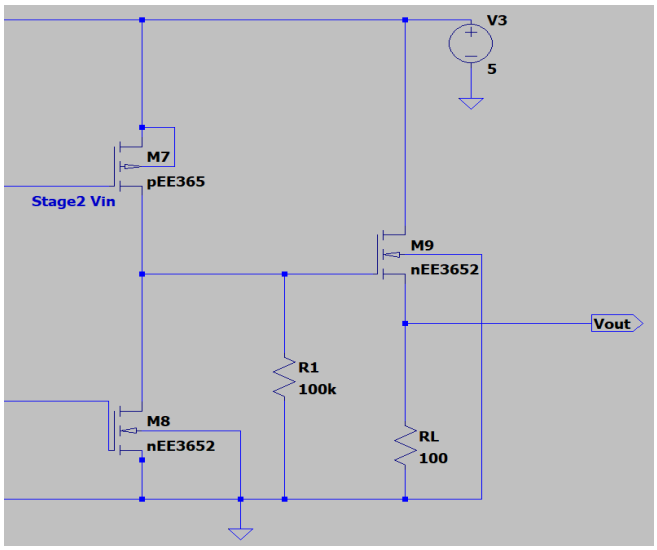


<Figure 5>

Figure 5 shows the Stage 1 differential amplifier circuit of this multistage amplifier. M3 and M5 form an NMOS differential pair, converting the small-signal input applied to the two inputs V1 and V2 into a current form. Ideally, the tail current of the differential pair remains constant overall, with current distributed to M3 and M5 based on the gate voltage difference between the two MOSFETs. M1 and M6, along with the ideal current source I1 (100μA), form the tail current source, supplying a nearly constant bias current to the differential pair. This tail current determines the operating point of the two input transistors, ensuring that the operating point and transconductance of Stage 1 remain largely unchanged despite variations in supply voltage or temperature (PVT variations).
The upper PMOS transistors M2 and M4 form a current-mirror active load. The current set on one branch (M2) is mirrored onto the other branch (M4), converting the current difference generated in the differential pair into a voltage swing at the single output node (Stage 1 Vout). The active load structure significantly increases the output resistance, enabling a large output voltage swing with only a small current change. This achieves high voltage gain in Stage 1.

In summary, Stage 1 functions as a high-gain differential amplifier utilizing a tail current source and a current-mirror active load. It suppresses the common-mode component of the input while significantly amplifying the differential component, passing it on to the next stage (Stage 2).

<Stage 2 Diagram>



<Figure 6>

Figure 6 shows the Stage 2 structure of this multistage amplifier. The Stage 2 Vin node on the left is the single output node from Stage 1, and this voltage is applied to the gate of PMOS M7. M7 operates as a PMOS active load with its drain connected to VDD (5V) and its source connected to the center node, regulating the center node current in response to changes in Stage 2 Vin.

The M8 transistor at the bottom is not a simple common-source amplifier, but rather an NMOS whose bias is supplied by the current mirror configured in Stage 1. That is, the current flowing through the drain-source of M8 becomes a nearly constant current mirrored from the current source in Stage 1. This current, in combination with M7, determines the operating point of Stage 2. With both stages coupled via the current mirror, the overall circuit bias is consistently maintained and the gain is stabilized. A resistor R1 (100 kΩ) is connected in parallel to the center node. R1 appropriately lowers the center node voltage in DC, thereby correcting the operating point of the M7–M8 combination. It also gently reduces excessively high open-loop gain, enhancing the circuit's linearity and stability.

The M9 on the right is an output buffer composed of an NMOS source follower, with its gate connected to the center node and its source connected to the output node Vout. The load resistor RL = 100 Ω simulates an actual external load. Thanks to the low output resistance provided by M9, sufficient voltage swing and drive capability are maintained even with this small load.

In summary, Stage 2 consists of a high-gain node formed by M8, biased by Stage 1's current mirror, and the PMOS active load M7 receiving the input signal, along with a source follower M9–RL structure outputting this signal with low impedance. It performs the role of significantly amplifying the signal amplified in Stage 1 and reliably delivering it to the load.

C. Circuit Simulation Results and Analysis

<Comparison of Theoretical Gain and Simulated Gain>

Stage 1 employs a differential pair + current-mirror active load structure, so the small-signal gain for a single output was approximated as follows.

$$A_1 \approx g_{m5}\,(r_{o4} \parallel r_{o5})$$

Here, `$g_{m5}$ ` is the transconductance of M5, and `$r_{o4}, r_{o5}$ ` is the output resistance of the upper PMOS load.

Theg_m of M5 was determined as

$$g_{m5} = \frac{2I_D}{V_{GS} - V_{th}} = \frac{2 \times 5 \times 10^{-5}}{(2.5\ \text{V} - 1.475\ \text{V}) - 1\ \text{V}} = \frac{0.0001}{0.025} = 4 \times 10^{-3}\ \text{A/V}$$

was calculated as . Furthermore, assuming the output resistance of the upper PMOS is$r_{o4} = r_{o5} = 6\ \text{M}\Omega$,

$$A_1 = 4 \times 10^{-3} \times 3\ \text{M}\Omega = 1.2 \times 10^4$$

and converting this to dB units gives

$$20\log_{10}(A_1) = 20\log_{10}(12{,}000) \approx 81.58\ \text{dB}$$

.Stage 2 has a structure where a common-source amplifier (M7–M8) and a resistorR_1 are connected in parallel. Therefore, the gain was approximated as

$$A_2 \approx g_{m7}\,(r_{o7} \parallel r_{o8} \parallel R_1)$$

. The transconductance of M7 was calculated as

$$g_{m7} = \frac{2I_D}{V_{GS} - V_{th}} = \frac{2 \times 5 \times 10^{-5}}{(5\ \text{V} - 3.982\ \text{V}) - 1\ \text{V}} = \frac{0.0001}{0.018} \approx 5.56 \times 10^{-3}\ \text{A/V}$$

was calculated as . The output resistance was set to$r_{o7} \parallel r_{o8} \approx 3\ \text{M}\Omega$, and when connected in parallel with$R_1 = 100\ \text{k}\Omega$,

$$r_{o,\text{eq}} = 3\ \text{M}\Omega \parallel 100\ \text{k}\Omega \approx 96{,}774\ \Omega$$

$$A_2 = g_{m7}\, r_{o,\text{eq}} = 5.56 \times 10^{-3} \times 96{,}774 \approx 538$$

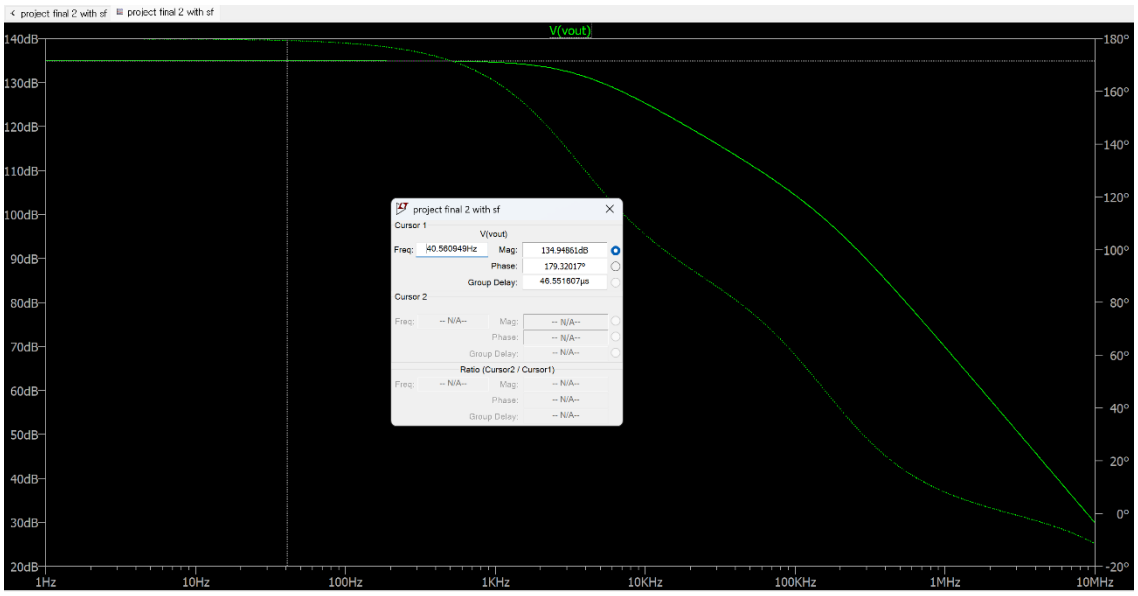
and expressed in dB as

$$20\log_{10}(A_2) = 20\log_{10}(538) \approx 54.62\ \text{dB}$$

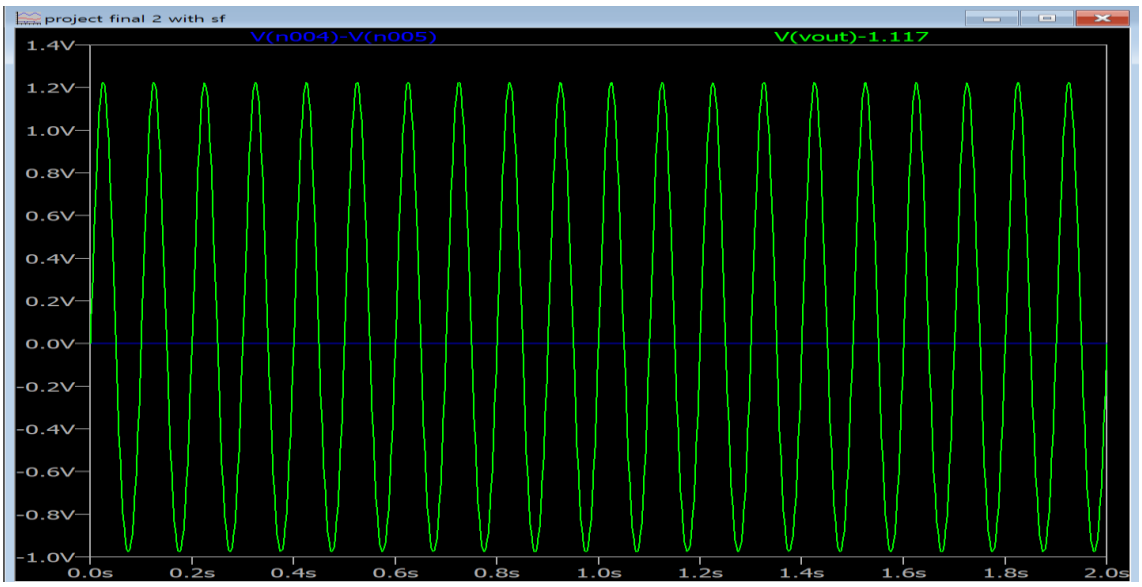
The overall gain of the multistage amplifier is the product of the gains of the two stages, so in dB units, it is expressed as a simple sum.

$$A_{\text{total,dB}} = 81.58\ \text{dB} + 54.62\ \text{dB} \approx 136.2\ \text{dB}$$

This is the total gain value calculated by approximating the voltage gain of the final stage, the source follower, as 1. Therefore, the theoretically calculated total voltage gain is approximately 136.2 dB. This value is very close to the 134.9 dB obtained from the subsequent LTspice simulation, confirming that the theoretical calculation and simulation results generally agree well. However, since the gain of the source follower is actually slightly less than 1, the overall gain in the simulations shown in <Figure 7> and <Figure 8> can be interpreted as appearing slightly lower than the theoretical value.

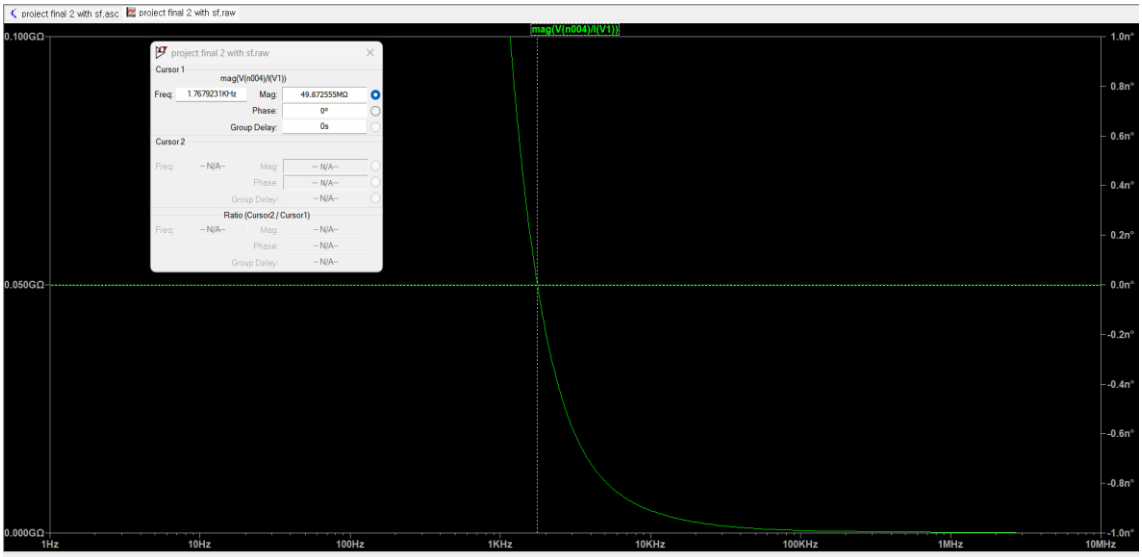


<Figure 7>



<Figure 8, input=V(n004)-V(n005) small signal$\pm 0.1uA$, V(out)-dc op point>

<Rin, input resistance>



<Figure 9>

The input resistance was determined in the AC analysis by applying a small signal to the input voltage source V1 and using the ratio of the input node voltage to current. In LTspice, the input voltage source was set to DC 2.5 V and AC 1 V, an AC sweep analysis was performed, and the probe expression was defined as V(n004)/I(V1). Here, n004 is the input gate node, and V1 is the input voltage source. Subsequently, the plot expression was set to mag(V(n004)/I(V1)) to observe the magnitude of the impedance versus frequency.

In <Figure 9>, the value read using the cursor at the mid-band frequency of approximately $f = 1.77$ kHz is

$$| R_{in} |=| \frac{V(n004)}{I(V1)} |\approx 4.99 \times 10^{7} \Omega$$

Therefore, the input resistance of this amplifier is formed at a very high level of approximately 50 MΩ in the intermediate frequency band.

This value significantly exceeds the task requirement of $R_{in} \geq 100$ kΩ . This high input resistance is interpreted as a result of the MOSFET gate structure, which ideally consumes almost no current.

Although the input impedance tends to decrease with increasing frequency due to Gate-Source and Gate-Drain Capacitance, simulation results confirm that it maintains values exceeding several MΩ across the entire bandwidth. This confirms its operation as a High Input Impedance amplifier with a practically very large input resistance.

<Calculation of 3dB Bandwidth from RC>

The 3-dB bandwidth was calculated using a single-pole approximation, assuming the dominant pole forms at the first-stage output node. First, the transconductance of M5 used in the first stage is as follows.

$$g_{m5} = \frac{2I_D}{V_{GS} - V_{th}} = \frac{2 \times 5 \times 10^{-5}}{(2.5\ \text{V} - 1.475\ \text{V}) - 1\ \text{V}} = 4 \times 10^{-3}\ \text{A/V}$$

If the output resistance of the upper PMOS load transistors M4 and M5 is set to

$$r_{o4} = r_{o5} = 6\ \text{MΩ}$$

, the equivalent resistance seen at the first-stage output node can be approximated as

$$R_{\text{eq}} \approx r_{o4} \parallel r_{o5} \approx 3\ \text{MΩ}$$

can be approximated as . The equivalent capacitanceC_{eq} is assumed to be dominated by the capacitanceC_{gd} seen from the second stage's M7 towards the first stage output. Using the value provided in the library,

$$C_{\text{eq}} \approx C_{gdo} \approx 15\ \text{pF} = 15 \times 10^{-12}\ \text{F}$$

. The resulting correction factor is

$$\tau = R_{\text{eq}} C_{\text{eq}} = 3 \times 10^{6}\ \Omega \times 15 \times 10^{-12}\ \text{F} = 45 \times 10^{-6}\ \text{s} = 45\ \mu\text{s}$$

This becomes, and in the single-pole approximation, the 3-dB frequency is

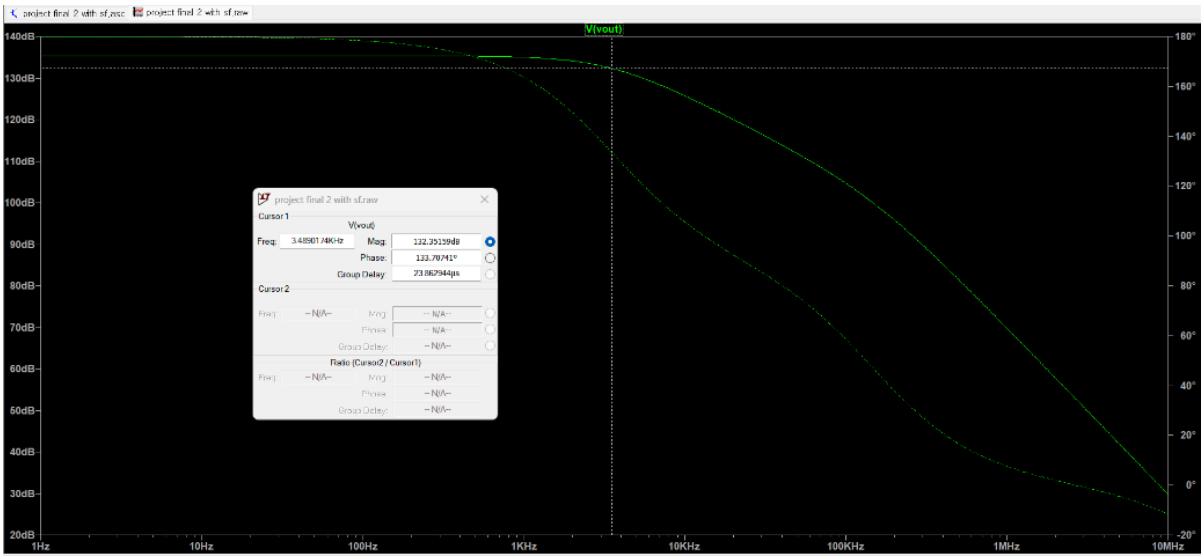
$$f_{\text{3dB}} = \frac{1}{2\pi\tau} = \frac{1}{2\pi \cdot 45 \times 10^{-6}} \approx 3.54 \times 10^{3}\ \text{Hz} \approx 3.5\ \text{kHz}$$

is calculated as

The high-frequency 3-dB bandwidth measured via AC analysis and Bode plot in LTspice (Figure 10 below)

$$f_{\text{3dB,sim}} \approx 3.489\ \text{kHz}$$

as shown in Figure 10. This value agrees very well with the theoretical value (approximately 3.5 kHz) obtained using the library's equivalent resistance between the$C_{gdo} = 15\ \text{pF}$ and the first-stage output node$R_{\text{eq}} \approx 3\ \text{M}\Omega$. Therefore, it can be concluded that the high-frequency bandwidth of this circuit is limited by the dominant pole formed by the gate–drain capacitanceC_{gd7} between the first-stage output node and the second-stage NMOS.



<Figure 10>

3. Discussion of Results and Issues

<Conclusion>

This design employs a differential input/single-ended output structure consisting of a first stage using a differential pair, a second stage common-source amplifier, and a source follower output buffer. The input is applied differentially to the two gates of the first-stage NMOS differential pair, and the output is acquired single-ended from the source terminal of the final source follower. Thus, it satisfies the requirement for a "differential input/single-ended output type."

Regarding the 3-dB bandwidth, the high-frequency 3-dB frequency measured from the AC analysis Bode plot was approximately$f_{\text{sim}} \approx 3.489\text{kHz}$. Meanwhile, calculating the dominant pole using the NMOS parameters from the model file (lib_EE365)$C_{gdo} = 15\text{pF}$, and the equivalent resistance at the first-stage output node$R_{\text{eq}} \approx 3M\Omega$, yielded a

theoretical 3-dB bandwidth of $f \approx 3.5$kHz , which agrees well with the simulation. This indicates that the Miller capacitance formed by the first-stage output node and the second-stage NMOS (C_{gd}) constitutes the dominant pole. The design satisfied the required 3-dB bandwidth specification of 100 Hz to 100 kHz.

The input resistance was determined by applying an AC voltage of 1 V to the input voltage source V1 during AC analysis, then measuring the magnitude of the ratio of input node voltage to current ($R_{in} = V(n004)/I(V1)$). At the mid-band frequency of approximately$1.77kHz$,$| R_{in} | \approx 4.99 \times 10^7 \Omega$ was measured, indicating an input resistance of approximately$50\text{M}\Omega$, which is very high. This characteristic arises because the MOSFET gate current is nearly zero, sufficiently exceeding the task requirement of$R_{in} \geq 100\text{k}\Omega$. Although impedance decreases across the entire frequency band due to gate-source and gate-drain capacitance as frequency increases, values exceeding several MΩ are maintained, confirming operation as a high input impedance amplifier.

For the load resistance condition, the resistor connected to the output stage (R_L) was designed to be 100 Ω. The DC analysis results showed that$V_{out} \approx 1.215$V and$I(R_L) \approx 12.15$mA , confirming again that$R_L \approx 100\Omega$. Therefore, the condition "Load resistance$R_L \leq 100\Omega$ " is satisfied. Thanks to the source follower structure, sufficient drive capability is ensured even with such a small load.

Regarding voltage gain, the theoretical gains for the first and second stages are calculated as$A_1 \approx 81.6$dB and$A_2 \approx 54.6$dB , respectively, yielding a total gain of$A_{V,\text{theory}} \approx 136$dB . The final output gain measured in the mid-band during AC analysis also appears at approximately 135–136 dB, closely matching the theoretical value of . This demonstrates that the approximationsg_m andr_o used in the design align well with the actual operating conditions. Regarding the requirement for "Overall Voltage Gain$A_{VM} \geq 50$dB ," the designed amplifier provides a gain significantly greater than this, thus fully satisfying the requirement.
For power consumption, the current flowing into the power supply VDD at the DC operating point was approximately $I_{DD} \approx 12.4$mA . Considering the supply voltage of 5 V, the total power consumption is $P_{\text{tot}} \approx 5V \times 12.4mA \approx 62mW$. This provides a significant margin below the task requirement limit of 500mW and aligns well with the design goal of achieving a low-power multistage amplifier.

<Issues and Improvement Directions>
While this circuit generally satisfies the project requirements well, several limitations and potential improvements exist. First, regarding power consumption, DC operating point simulation results indicate a supply current of approximately$I_{DD} \approx 12.4$ mA . Considering the supply voltage of 5 V, the total power consumption is about62 mW . While this is well within the task requirement of 500 mW, the absolute power consumption is somewhat high for a design emphasizing "low-power bias at the tens of μA level." To further improve power efficiency in the future, the bias current of each stage can be gradually reduced. Correspondingly, the W/L ratio of the MOSFETs can be adjusted to optimize the design. This approach maintains the required gain and bandwidth while lowering the overall power consumption.

Regarding frequency characteristics, AC analysis results show a high-frequency 3-dB bandwidth of approximately 3.5 kHz. While this falls within the 100 Hz to 100 kHz range required by the project, it indicates a limitation in that the practical upper frequency limit is not particularly high. This occurs because the output node of the first-stage differential amplifier possesses a very large output resistance. Combined with the MOSFET gate–drain capacitance, this forms a large RC time constant, causing the dominant pole to appear at a relatively low frequency. To widen the bandwidth,

the circuit can be modified by either reducing the equivalent resistance at the first-stage output node (e.g., a structure that lowers the output impedance instead of slightly reducing the first-stage gain) or optimizing the size of the second-stage input MOSFET to reduce unnecessarily large input capacitance.

Finally, regarding input signal magnitude and linearity, this circuit operates very well with extremely high gain for small differential inputs in the μV to several mV range. However, when the input differential voltage increases, current concentrates on one transistor of the first-stage differential pair, leading to significant nonlinear distortion. In essence, this structure is a high-gain amplifier optimized for the small-signal region, with a limited operating range for large-signal conditions. If linearity must be maintained for larger input signals, improvements can be made by adding a small source degeneration resistor to the differential pair source to widen the linear range, or by changing to a closed-loop structure using feedback in the subsequent stage to keep the actual applied input differential voltage small.

4. References

-Microelectronics 2 Lecture Materials by Professor Younghyun Lim, Week 6: Current Mirror <Figure 1>
-Microelectronics 2 Lecture Materials by Professor Lim Young-hyun, Week 10: Differential Amplifier <Figure 2>
- Microelectronics 2 Lecture Materials by Professor Younghyun Lim, Week 5: Amplifier <Figure 3>
-