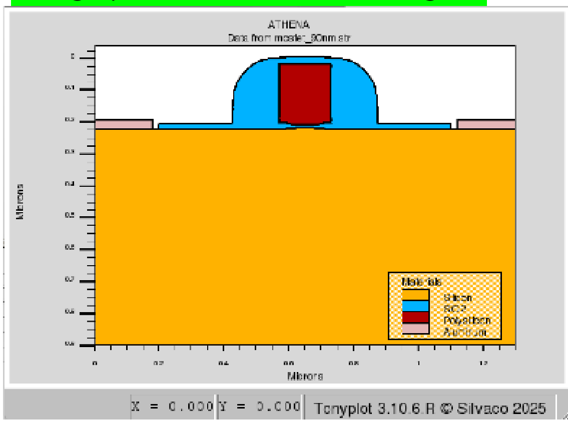
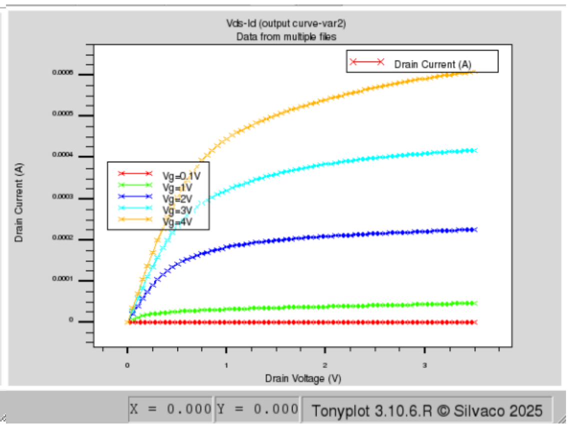
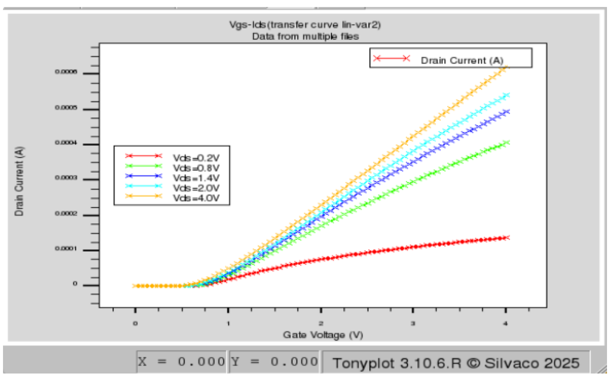
Semiconductor Fabrication 2023105155 Chanseung LEE/90nm NMOS 분석 (Optimization in Fabricating 90nm NMOS Transistors Using Silvaco-variation2)

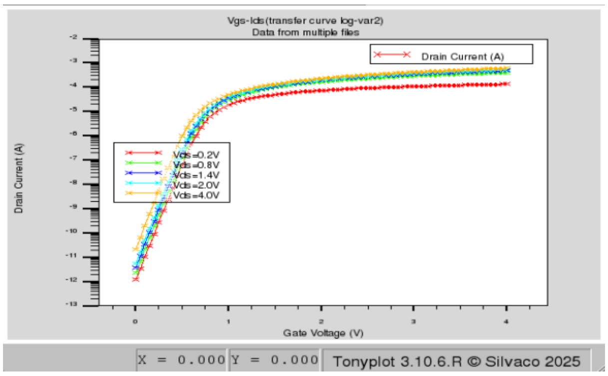
1. I-V graph and Athena device diagram





*The left section shows the structure of the 90nm NMOS formed by Silvaco Athena. A 10 nmgate oxide film and an n+ poly silicon gate are deposited on the P-type Si substrate, and there is an n+ S/D diffusion layer formed by As injection on both sides. The right ID-Vds curve is measured in the range of Vg=0~4V. As the Vg increases, the channel is reversed, and the current is proportional to the Vgs in the linear region, and after the pinch off, it transitions to the saturation region and the current increase rate decreases. The higher the Vg, the higher the inversion carrier concentration and the saturation current, which is explained by the relationship. The slight increase in the slope of the curve is due to channel length modulation and $I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2$velocity saturation.



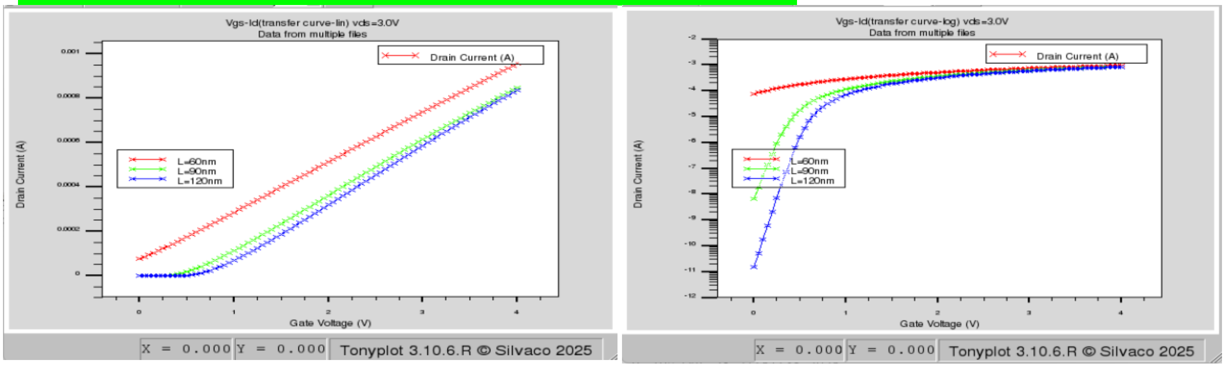


*The ID-Vg curve shows the change of drain current with the gate voltage and shows the typical NMOS characteristic of a rapid increase in current due to the reversal of the channel surface potential as the Vg increases. Vth is the point at which the current begins to increase on the linear scale, and in this simulation, it is about 0.9-1V. This value showed a large error from the Vth of variation 2 reported in the paper. This is because the detailed processing conditions were not sufficiently presented in the paper, so it was different from the simulation conditions.

*The subthreshold region is clearly visible on the log scale on the right, and the subthreshold swing(ss) is calculated as about 80-90 mV/dec from the slope of this section. This is consistent with the thickness of the oxide film and the capacitance ratio 1+Cdep/Cox relationship by channel doping.

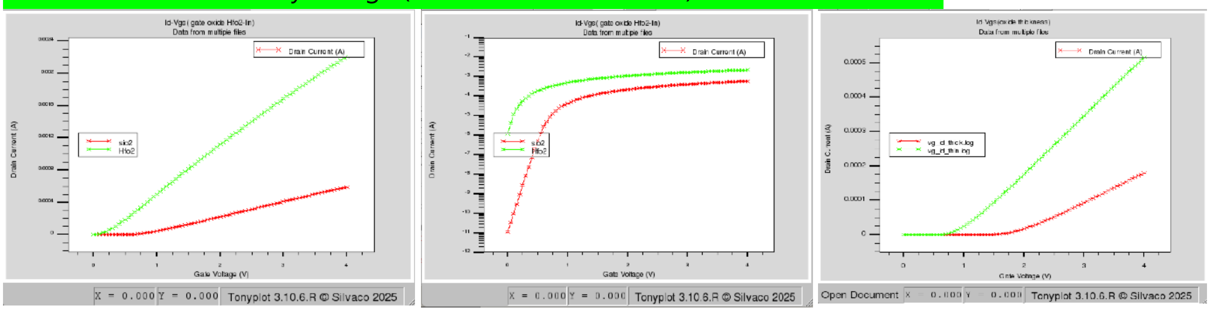
*Next, on the right log scale, the DIBL effect is observed in which the curve shifts to the left as the drain voltage increases. This is a phenomenon in a transistor with a relatively narrow channel, where the drain voltage lowers the channel barrier and reduces the Vth.

2. Channel Length Id-Vgs (Channel Length=60nm, 90nm, 120nm)



*The linear scale graph on the left directly shows the change in drain current with gate voltage, and the shorter the channel length, the higher the drain current flows in the same Vg. This Vth roll-off is more pronounced as the channel length becomes shorter, and in the short channel, in addition to the gate field, the drain field directly controls the channel potential, and the Vth gradually decreases as the length decreases. As a result, the current begins to flow early even at the smaller gate voltage. In addition, this critical voltage drop that occurs as the channel length decreases is closely related to the DIBL phenomenon. drain The field lowers the source-channel barrier, facilitating electron injection, which increases the current in the subthreshold region and worsens the SS properties. In the Log scale graph on the right, we can see that the off-current increases significantly in the short channel (60 nm) and the slope of the subthreshold region becomes gentler, which is also related to the punch-through phenomenon mentioned in the paper. As the channel is shortened, the drain potential passes through the lower part of the channel and combines with the source potential, weakening the gate's potential control ability, resulting in an increase in leakage current

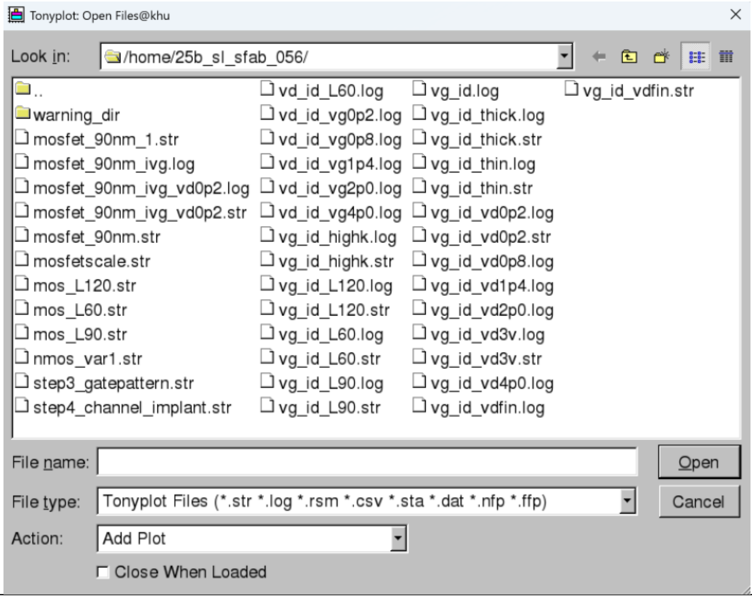
3.Gate Oxide Permittivity Id-Vgs (Sio2=3.9 and Hfo2=20) and oxide thickness

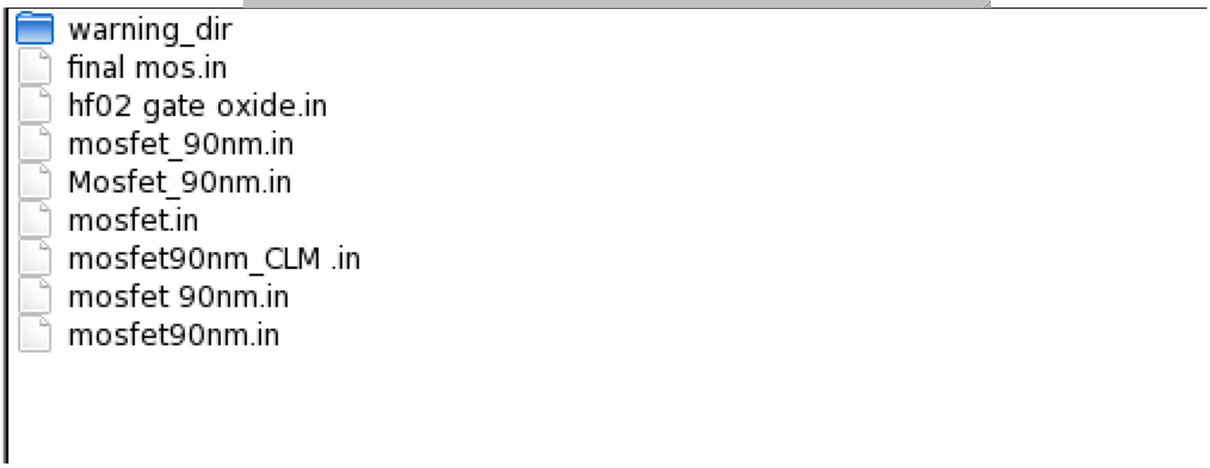


*HfO_2(ε=20) devices exhibit much larger drain currents at the same gate voltage compared to SiO_2(ε=3.9), because the high dielectric constant increases gate capacitance and makes channel reversal easier to form. As a result, Vth is lowered and gate control ability is improved, resulting in a significant increase in on-current. In addition, the slope of the subthreshol d region is steep, confirming that the SS characteristics have improved. However, even around Vg=0V, the current

does not drop completely to zero, but appears relatively large. This is due to the DIBL effect and some punch-through currents that occur at high Vds (3V). In other words, although the performance of the device was improved by increasing the gate dielectric constant, the disadvantage of increasing the leakage current of the off state under high drain field conditions also appeared. This disadvantagecan be solved by adjusting the gate EO T. Comparing the ID-Vgs characteristics of thin oxide film samples, the thin oxide film showed higher gate current and lower Vth. This is due to the fact that the oxide film thickness was changed by adjusting the diffuse time. It was confirmed that the thinner the oxide film, the increased the gate capacitance (Cox), and a larger drain current flowed at the same gate voltage.

Output File


Tonyplot: Open Files@khu
Look in:
/home/25b_sl_sfab_056/
..
warning_dir
mosfet_90nm_1.str
mosfet_90nm_ivg.log
mosfet_90nm_ivg_vd0p2.log
mosfet_90nm_ivg_vd0p2.str
mosfet_90nm.str
mosfetscale.str
mos_L120.str
mos_L60.str
mos_L90.str
nmos_var1.str
step3_gatepattern.str
step4_channel_implant.str
vd_id_L60.log
vd_id_vg0p2.log
vd_id_vg0p8.log
vd_id_vg1p4.log
vd_id_vg2p0.log
vd_id_vg4p0.log
vg_id_highk.log
vg_id_highk.str
vg_id_L120.log
vg_id_L120.str
vg_id_L60.log
vg_id_L60.str
vg_id_L90.log
vg_id_L90.str
vg_id.log
vg_id_thick.log
vg_id_thick.str
vg_id_thin.log
vg_id_thin.str
vg_id_vd0p2.log
vg_id_vd0p2.str
vg_id_vd0p8.log
vg_id_vd1p4.log
vg_id_vd2p0.log
vg_id_vd3v.log
vg_id_vd3v.str
vg_id_vd4p0.log
vg_id_vdfin.log
vg_id_vdfin.str
File name:
Open
File type:
Tonyplot Files (*.str *.log *.rsm *.csv *.sta *.dat *.nfp *.ffp)
Cancel
Action:
Add Plot
Close When Loaded


warning_dir
final mos.in
hf02 gate oxide.in
mosfet_90nm.in
Mosfet_90nm.in
mosfet.in
mosfet90nm_CLM .in
mosfet 90nm.in
mosfet90nm.in

Silvaco code-Mosfet athena and atlas for Id-Vgs, Id-Vds

```
go athena
line x loc=0.0 spac=0.1
line x loc=0.25 spac=0.008
line x loc=0.45 spac=0.008
line x loc=0.65 spac=0.015

line y loc=0.0 spac=0.002
line y loc=0.18 spac=0.006
line y loc=0.5 spac=0.04
line y loc=0.9 spac=0.12
init orientation=100 c.boron=1e15 space.mul=2
diffus temp=1000 time=30 dryo2 hcl=3
etch oxide thick=0.02
implant boron dose=3.0e13 energy=95 pearson
diffus temp=950 time=100 weto2 hcl=3
diffus temp=1000 time=50 dryo2 hcl=3
diffus temp=1200 time=200 nitro
diffus temp=1200 time=80 nitro
etch oxide all
diffus temp=1000 time=20 dryo2 hcl=3
etch oxide all

diffus temp=925 time=3 dryo2 press=1 hcl=3
implant boron dose=9.5e11 energy=10 pearson
depo poly thick=0.2 divi=10
etch poly left p1.x=0.56
method fermi compress
diffuse temp=900 time=5 weto2

implant phosphorus dose=3e13 energy=20 pearson
depo oxide thick=0.12 divisions=8
etch oxide dry thick=0.12

implant arsenic dose=5e15 energy=50 pearson
method fermi compress
diffuse temp=900 time=1 nitro

etch oxide left p1.x=0.2
```

```
deposit alumin thick=0.03 divi=2
etch alumin right p1.x=0.18

structure mirror right
electrode name=gate x=0.6 y=0.1
electrode name=source x=0.1
electrode name=drain x=1.2
electrode name=substrate backside
structure outfile="mosfet_90nm.str"

tonyplot "mosfet_90nm.str"
go atlas

mesh infile="mosfet_90nm.str"
models cvt srh print numcarr=2
contact name=gate n.poly
interface qf=3e10
method newton

solve init
solve vdrain=0.2
log outf=vg_id_vd0p2.log master
Solution name=gate vigget=0.0
solve name=gate vstep=0.05 vfinal=4.0
log off

solve init
solve vdrain=0.8
log outf=vg_id_vd0p8.log master
Solution name=gate vigget=0.0
solve name=gate vstep=0.05 vfinal=4.0
log off

solve init
solve vdrain=1.4
log outf=vg_id_vd1p4.log master
Solution name=gate vigget=0.0
solve name=gate vstep=0.05 vfinal=4.0
log off
```

```
solve init
solve vdrain=2.0
log outf=vg_id_vd2p0.log master
Solution name=gate vigget=0.0
solve name=gate vstep=0.05 vfinal=4.0
log off

solve init
solve vdrain=4.0
log outf=vg_id_vd4p0.log master
Solution name=gate vigget=0.0
solve name=gate vstep=0.05 vfinal=4.0
log off

Tonyplot -overlay -st
vg_id_vd0p2.log_vg_id_vd0p8.log_vg_id_vd1p4.log_vg_id_vd2p0.log_vg_id_vd4p0.logs
vg_id_vd4p0.people

go atlas
mesh infile="mosfet_90nm.str"
models cvt srh print numcarr=2
contact name=gate n.poly
interface qf=3e10
method climit=1e-4 maxtrap=10
solve init

solve vgate=0.1 outf=tmp_vg01
solve vgate=1.0 outf=tmp_vg10
solve vgate=2.0 outf=tmp_vg20
solve vgate=3.0 outf=tmp_vg30
solve vgate=4.0 outf=tmp_vg40

load infile=tmp_vg01
log outf=ivd_vg0p1.log master
solve vdrain=0.0
solve name=drain vstep=0.05 vfinal=3.5
log off
```

```
load infile=tmp_vg10
log outf=ivd_vg1.log master
solve vdrain=0.0
solve name=drain vstep=0.05 vfinal=3.5
log off

load infile=tmp_vg20
log outf=ivd_vg2.log master
solve vdrain=0.0
solve name=drain vstep=0.05 vfinal=3.5
log off

load infile=tmp_vg30
log outf=ivd_vg3.log master
solve vdrain=0.0
solve name=drain vstep=0.05 vfinal=3.5
log off

load infile=tmp_vg40
log outf=ivd_vg4.log master
solve vdrain=0.0
solve name=drain vstep=0.05 vfinal=3.5
log off
Tonyplot -overlay -st IVD_VG0P1.People IVD_VG1.People IVD_VG2.People IVD_VG3.People
IVD_VG4.People IVD_VG4.People
quit
```

Silvaco code-Mosfet athena and atlas for Channel length Modulation

 # channel 60nm

```
go athena
line x loc=0.0 spac=0.1
line x loc=0.25 spac=0.008
line x loc=0.45 spac=0.008
line x loc=0.65 spac=0.015
line y loc=0.0 spac=0.002
line y loc=0.18 spac=0.006
line y loc=0.5 spac=0.04
line y loc=0.9 spac=0.12

init orientation=100 c.boron=1e15 space.mul=2
```

```
diffus temp=1000 time=30 dryo2 hcl=3
etch oxide thick=0.02
implant boron dose=3.0e13 energy=95 pearson
diffus temp=950 time=60 weto2 hcl=3
etch oxide all
diffus temp=925 time=3 dryo2 press=1 hcl=3
implant boron dose=9.5e11 energy=10 pearson

depo poly thick=0.2 divi=10
etch poly left p1.x=0.57
method fermi compress
diffuse temp=900 time=5 weto2

implant phosphorus dose=3e13 energy=20 pearson
depo oxide thick=0.12 divisions=8
etch oxide dry thick=0.12
implant arsenic dose=5e15 energy=50 pearson
method fermi compress
diffuse temp=1000 time=10 nitro

etch oxide left p1.x=0.2
deposit alumin thick=0.03 divi=2
etch alumin right p1.x=0.18

structure mirror right
electrode name=gate x=0.6 y=0.1
electrode name=source x=0.1
electrode name=drain x=1.2
electrode name=substrate backside
structure outfile="mos_L60.str"
go atlas

mesh infile="mos_L60.str"
models cvt srh print
contact name=gate n.poly
interface qf=3e10
method newton autonr climit=5e-5

solve init
```

```
solve vdrain=3.0
log outf=vg_id_L60.log master
Solution name=gate vigget=0.0
solve name=gate vstep=0.05 vfinal=4.0
log off
save outf=vg_id_L60.str
quit
```

#channel 90nm

```
go athena
line x loc=0.0 spac=0.1
line x loc=0.25 spac=0.008
line x loc=0.45 spac=0.008
line x loc=0.65 spac=0.015
line y loc=0.0 spac=0.002
line y loc=0.18 spac=0.006
line y loc=0.5 spac=0.04
line y loc=0.9 spac=0.12

init orientation=100 c.boron=1e15 space.mul=2
diffus temp=1000 time=30 dryo2 hcl=3
etch oxide thick=0.02
implant boron dose=3.0e13 energy=95 pearson
diffus temp=950 time=60 weto2 hcl=3
etch oxide all

diffus temp=925 time=3 dryo2 press=1 hcl=3
implant boron dose=9.5e11 energy=10 pearson

depo poly thick=0.2 divi=10
etch poly left p1.x=0.555
method fermi compress
diffuse temp=900 time=5 weto2

implant phosphorus dose=3e13 energy=20 pearson
depo oxide thick=0.12 divisions=8
etch oxide dry thick=0.12
implant arsenic dose=5e15 energy=50 pearson
method fermi compress
diffuse temp=1000 time=10 nitro
```

```
etch oxide left p1.x=0.2
deposit alumin thick=0.03 divi=2
etch alumin right p1.x=0.18

structure mirror right
electrode name=gate x=0.6 y=0.1
electrode name=source x=0.1
electrode name=drain x=1.2
electrode name=substrate backside
structure outfile="mos_L90.str"
go atlas

mesh infile="mos_L90.str"
models cvt srh print
contact name=gate n.poly
interface qf=3e10
method newton autonr climit=5e-5

solve init
solve vdrain=3.0
log outf=vg_id_L90.log master
Solution name=gate vigget=0.0
solve name=gate vstep=0.05 vfinal=4.0
log off
save outf=vg_id_L90.str
quit
```

#channel 120nm

```
go athena
line x loc=0.0 spac=0.1
line x loc=0.25 spac=0.008
line x loc=0.45 spac=0.008
line x loc=0.65 spac=0.015
line y loc=0.0 spac=0.002
line y loc=0.18 spac=0.006
line y loc=0.5 spac=0.04
line y loc=0.9 spac=0.12

init orientation=100 c.boron=1e15 space.mul=2
```

```
diffus temp=1000 time=30 dryo2 hcl=3
etch oxide thick=0.02
implant boron dose=3.0e13 energy=95 pearson
diffus temp=950 time=60 weto2 hcl=3
etch oxide all

diffus temp=925 time=3 dryo2 press=1 hcl=3
implant boron dose=9.5e11 energy=10 pearson

depo poly thick=0.2 divi=10
etch poly left p1.x=0.54
method fermi compress
diffuse temp=900 time=5 weto2

implant phosphorus dose=3e13 energy=20 pearson
depo oxide thick=0.12 divisions=8
etch oxide dry thick=0.12
implant arsenic dose=5e15 energy=50 pearson
method fermi compress
diffuse temp=1000 time=10 nitro

etch oxide left p1.x=0.2
deposit alumin thick=0.03 divi=2
etch alumin right p1.x=0.18

structure mirror right
electrode name=gate x=0.6 y=0.1
electrode name=source x=0.1
electrode name=drain x=1.2
electrode name=substrate backside
structure outfile="mos_L120.str"
go atlas
mesh infile="mos_L120.str"
models cvt srh print
contact name=gate n.poly
interface qf=3e10
method newton autonr climit=5e-5
solve init
solve vdrain=3.0
```

```
log outf=vg_id_L120.log master
Solution name=gate vigget=0.0
solve name=gate vstep=0.05 vfinal=4.0
log off
save outf=vg_id_L120.str
quit
```

Silvaco code-Mosfet athena and atlas for Id-Vgs gate oxide Hfo2 reigon2 permittivity=20

```
go atlas
mesh infile="mosfet_90nm.str"
material region=2 permittivity=20
models cvt srh print numcarr=2
contact name=gate n.poly
interface qf=3e10
method newton autonr climit=5e-5
solve init
solve vdrain=3.0

log outf=vg_id_vdfin.log master
Solution name=gate vigget=0.0
solve name=gate vstep=0.05 vfinal=4.0
log off
save outf=vg_id_vdfin.str
tonyplot vg_id_vdfin.log
quit
```

Silvaco code-Mosfet athena for Id-Vgs gate oxide Thickness(Changing diffuse time 3s-→ 15s, output File Thick, Thin)

```
go athena
line x loc=0.0 spac=0.1
line x loc=0.25 spac=0.008
line x loc=0.45 spac=0.008
line x loc=0.65 spac=0.015

line y loc=0.0 spac=0.002
line y loc=0.18 spac=0.006
line y loc=0.5 spac=0.04
line y loc=0.9 spac=0.12
init orientation=100 c.boron=1e15 space.mul=2
diffus temp=1000 time=30 dryo2 hcl=3
etch oxide thick=0.02
```

```
implant boron dose=3.0e13 energy=95 pearson
diffus temp=950 time=100 weto2 hcl=3
diffus temp=1000 time=50 dryo2 hcl=3
diffus temp=1200 time=200 nitro
diffus temp=1200 time=80 nitro
etch oxide all
diffus temp=1000 time=20 dryo2 hcl=3
etch oxide all

diffus temp=925 time=15 dryo2 press=1 hcl=3
implant boron dose=9.5e11 energy=10 pearson
depo poly thick=0.2 divi=10
etch poly left p1.x=0.56
method fermi compress
diffuse temp=900 time=5 weto2

implant phosphorus dose=3e13 energy=20 pearson
depo oxide thick=0.12 divisions=8
etch oxide dry thick=0.12

implant arsenic dose=5e15 energy=50 pearson
method fermi compress
diffuse temp=900 time=1 nitro

etch oxide left p1.x=0.2
deposit alumin thick=0.03 divi=2
etch alumin right p1.x=0.18

structure mirror right
electrode name=gate x=0.6 y=0.1
electrode name=source x=0.1
electrode name=drain x=1.2
electrode name=substrate backside
structure outfile="mosfet_90nm.str"

tonyplot "mosfet_90nm.str"
```