Chanseung Lee

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Education

• **Kyung Hee University**, Republic of Korea

- B.S. in Applied Physics & Electronic Engineering 2023 – 2027 (expected)

• **Research Interests**

developing semiconductor-based photonic integrated circuits for next-generation quantum computers.

- Silicon Photonics: Towards integrated optical computers with strain-engineered on-chip lasers

- Quantum Photonics: Towards integrated quantum processors with strain-engineered 2D quantum devices

- Graphene Photonics: Towards graphene-integrated photonic circuits with strained graphene devices

• **Research Experience**

KAIST Q-Spin Laboratory (Quantum semiconductor Photonic Integrated Lab)
Advisor: Professor Donguk Nam Research Intern, Dec 2025 – Feb 2026

- Modeling strain-engineered optical & quantum behavior

- Exploring integration strategies for on-chip optical quantum computing

• **Projects**

- TCAD CMOS Process Simulation

Built full NMOS process flow (oxidation → implantation → annealing → metallization)
Simulated ID–VG, ID–VD, Vth, gm, ro using Silvaco ATLAS

- Three-Stage Analog Amplifier (LTspice)

Designed differential → gain → output stages - AC/DC/transient analysis and pole-zero extraction

• **Skills**

- TCAD (ATHENA, ATLAS)

- Python (numpy, matplotlib)

- LTspice (analog IC design)

- Semiconductor device physics, photonics, 2D materials