

## Chanseung Lee

[cslee20a@gmail.com](mailto:cslee20a@gmail.com)

### • Education

[Kyung Hee University](#), Republic of Korea

- B.S. in Applied Physics & Electronic Engineering 2023 – 2027 (expected)

### • Research Interests

Developing semiconductor-based photonic integrated circuits for next-generation quantum computers.

- Silicon Photonics: Towards integrated optical computers with strain-engineered on-chip lasers
- Quantum Photonics: Towards integrated quantum processors with strain-engineered 2D quantum devices

### • Research Experience

[Q-SPIN Laboratory](#) (Quantum semiconductor Photonic Integrated Lab), [KAIST](#)

Advisor: Professor Donguk Nam

Research Intern, Dec 2025 – Feb 2026

- Modeling strain-engineered optical & quantum behavior
- Exploring integration strategies for on-chip optical quantum computing

### • Projects

- TCAD CMOS Process Simulation [\[link\]](#)

Built full NMOS process flow (oxidation → implantation → annealing → metallization)

Simulated ID–VG, ID–VD, Vth, gm, ro using Silvaco ATLAS, ATHENA

- Three-Stage Analog Amplifier (LTspice) [\[link\]](#)

Designed differential → gain → output stages - AC/DC/transient analysis and pole-zero extraction

### • Skills

- TCAD (ATHENA, ATLAS)
- LTspice (analog IC design)
- Semiconductor device physics, photonics, 2D materials
- Semiconductor Fabrication, MEMS