MOSFET Transistor Measurement Report

Chanseung Lee 2023105155 Department of electronic engineering

Ⅰ. Abstract

This experiment was conducted to experimentally verify the key operating principles and characteristics of MOSFETs learned in this semester's Semiconductor Engineering course and to deepen understanding. The experiment utilized the MS TECH PROBE STATION to establish a stable probing environment and employed CLARIUS software to precisely measure and analyze current-voltage characteristics.

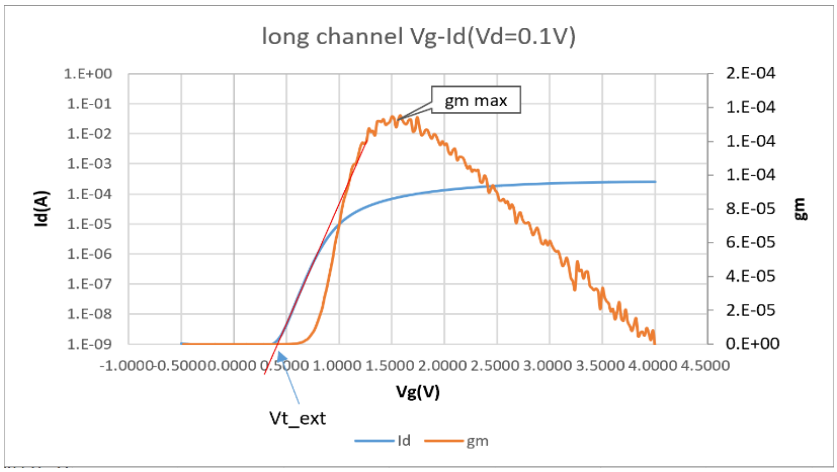
The transistor gate channel lengths were set to two values: 0.35 μm and 10 μm. The gate width was fixed at 10 μm for all transistors. Measured parameters included threshold voltage (Vt_ext, Vt_lin, Vt_sat), subthreshold swing (SS), off-state leakage current (Ioff), saturation drain current (Idsat), gate-induced drain leakage (GIDL), and drain-induced barrier lowering (DIBL). Data points were acquired by sweeping Vg from -0.5V to 4V and Vd up to 3.3V in 0.02V increments. From these, transconductance (gm) calculations and Vt extrapolation were performed. Additionally, body bias (Vb = 0V, -0.5V, -1V) is applied to observe how the threshold voltage changes.

Through this experiment, we expect to directly verify the physical concepts of semiconductor devices learned theoretically and gain a more concrete and intuitive understanding of MOSFET characteristics by analyzing the actual measurement results.

Ⅱ. Experimental Results and Analysis (Since the source voltage is 0V throughout this experiment, Vgs=Vg and Vds=Vd are used)

A. Long Channel MOSFET

This experiment analyzes the electrical characteristics of a Long Channel MOSFET with a gate channel length of 10 μm and a gate width of 10 μm. Based on the measured I–V data, key device parameters such as Threshold Voltage, Subthreshold Swing, and Saturation Current are extracted and interpreted using concepts learned in semiconductor engineering theory.



<Figure 1 Vg-Id with gm at Vd=0.1V>

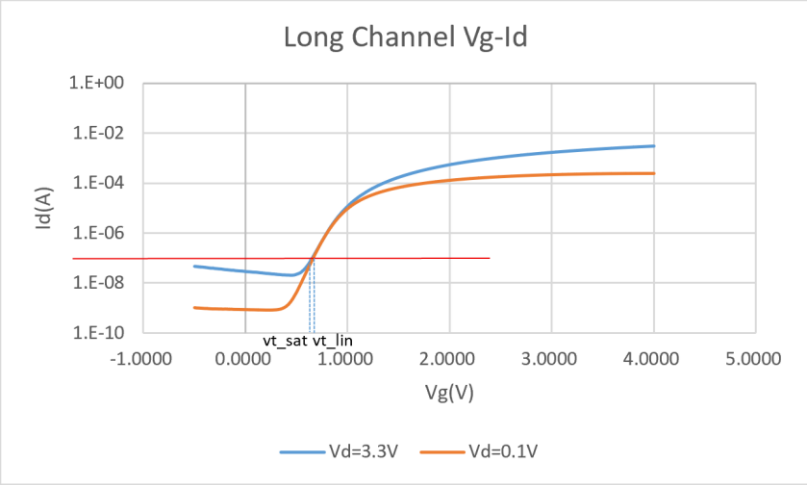
The figure below shows the Vg-Id graph and the gm (transconductance) graph for the long Channel MOSFET.

The first set of measurements was performed on a long-channel MOSFET with a gate-channel length of 10 μm and a gate width of 10 μm. The drain voltage (Vd) was set to 0.1V and 3.3V, respectively, while the gate voltage (Vg) was varied to measure the drain current (Id) and transconductance (gm). The measured Vg–Id characteristics were plotted on a logarithmic scale to visualize the linear region in the subthreshold region. The threshold voltage (Vt_ext) was extracted by extrapolating a straight line from this region.

At Vd = 0.1 V, gm exhibited a maximum value around Vg ≈ 1.50 V, indicating the voltage range where the device enters a strong inversion state. By extrapolating this to find the Vg value where Id becomes zero, and using this to calculate Vt_ext, Vt_ext was derived to be approximately 0.4 V. Theoretically, the MOSFET's Vt of approximately 0.4–0.5 V corresponds to the point where inversion occurs in the MOS structure and the channel forms. This was also confirmed experimentally.

Consequently, this Long Channel MOSFET was confirmed to operate most actively around a Vg of approximately 1.5V, with a threshold voltage of about 0.4V.

Next, based on the graph below, we determined the Vt_lin and Vt_sat values to understand the DIBL phenomenon of this device. The graph showing Vt_lin and Vt_sat is as follows.



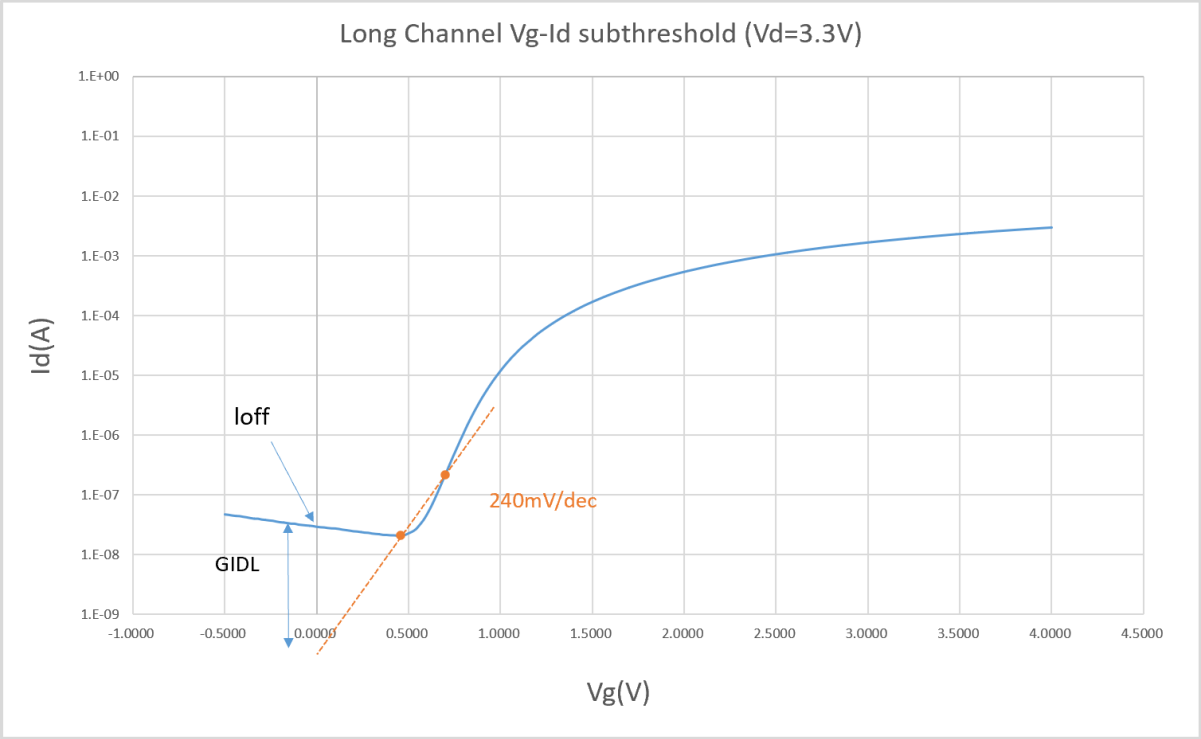
<Figure 2>

The graph above shows that the Vt_lin and Vt_sat values at 100nA/um are nearly identical. Since this device is a long channel MOSFET, it theoretically exhibits a very small DIBL effect. DIBL can be calculated using the following equation.

$$DIBL = \frac{Vt\_lin - Vt\_sat}{Vd\_sat - Vd\_lin}$$

According to this formula, the difference between the measured Vt_lin and Vt_sat values is very small, so the numerator can be approximated as zero. Therefore, the DIBL effect of this device can be considered nearly zero. This result is a natural consequence for long-channel MOSFETs. It also aligns with the theory that the channel length is sufficiently long such that even when the drain voltage increases, the energy barrier on the drain side does not decrease.

Next, graphs for subthreshold swing, GIDL, and leakage current (Ioff) were extracted from the Vg-Id graph described above. The graphs are as follows.



<Figure 3>

Figure 3 shows the Vg–Id curve of a long channel MOSFET measured at Vd = 3.3 V on a logarithmic scale. This graph was created to analyze the subthreshold swing (SS), off-state leakage current (Ioff), and gate-induced drain leakage (GIDL) characteristics by examining current changes in the subthreshold region.

First, the Id increase region in the subthreshold region appears relatively linear, and the subthreshold swing can be calculated from the slope of this region. The slope obtained from the linear region marked on the graph was approximately 240 mV/dec. This value is significantly larger than the ideal value of 60 mV/dec, suggesting that SS may have increased due to process defects, oxide quality, or bulk conduction paths, despite the long channel structure. SS is an indicator of the switching characteristics near the device threshold; a smaller value indicates superior switching performance.

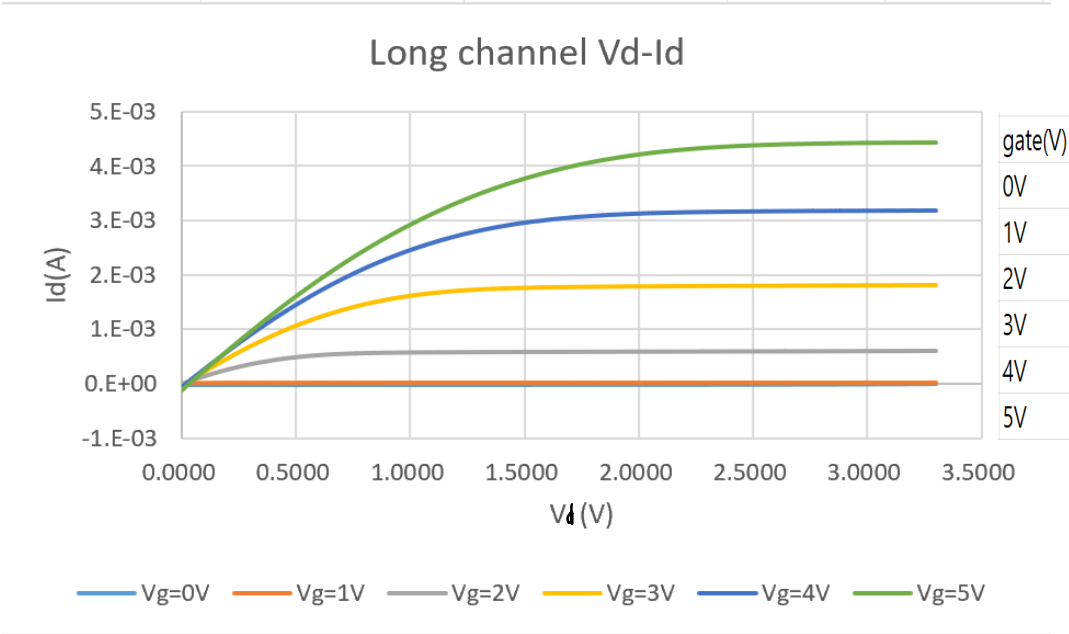
Next, the off-state leakage current (Ioff) is defined as the drain current when Vg is 0 V. In this experiment, it was measured at approximately 1.5×10^{-7} A ( ). This represents the residual current

when the MOSFET is off and is a very important metric for low-power circuits. Ideally, this value should be below several nA; however, the measured value is relatively large. This could be due to leakage paths, thermoelectric current, or weak subthreshold control.

Additionally, GIDL is a phenomenon where drain current increases again when Vg is applied at a negative voltage. This graph also shows Id rising around Vg = -0.5 V. This is interpreted as occurring because the strong drain voltage (Vd = 3.3 V) increases the electric field between the gate and drain, causing band-to-band tunneling and increasing leakage current. GIDL is a leakage mechanism that can be problematic, especially in high-voltage operating environments. To suppress it, methods such as improving the gate insulator or employing a LDD (Lightly Doped Drain) structure are utilized.

Overall, this graph confirms that the device exhibits a relatively gradual current increase characteristic in the subthreshold region, while Ioff and GIDL are also somewhat large. This suggests that despite the long channel structure, there is room for improvement in leakage current control, and the overall characteristics can vary depending on the device process and structural design.

Next, the drain current characteristics of the MOSFET transistor were analyzed as a function of drain voltage. Measurements were taken by incrementing the gate voltage from 0V to 5V in 1V steps. The corresponding saturated-region drain current (Id,sat) values for each gate voltage were also separately compiled for comparison. The relevant graphs are presented below.



gate(V)	Id,sat(A)
0V	25.9449E-9
1V	14.8252E-6
2V	602.9102E-6
3V	1.8167E-3
4V	3.1815E-3
5V	4.4350E-3

<Figure 4>

The graph and table clearly show that the saturation current (Id,sat) of the drain current (Id) increases nonlinearly as the gate voltage (VG) increases. First, at Vg=0 V, almost no current flows, with only a leakage current level of approximately 25.94 nA observed. However, when Vg increases to 1 V, the saturation current Id,sat rises sharply to about 14.83 μA ( ), indicating that a channel has

formed and current begins to flow substantially. Subsequently, the current reaches approximately 602.91 μA at Vg=2 V, about 1.82 mA at Vg=3 V, 3.18 mA at Vg=4 V, and 4.44 mA at Vg=5 V.

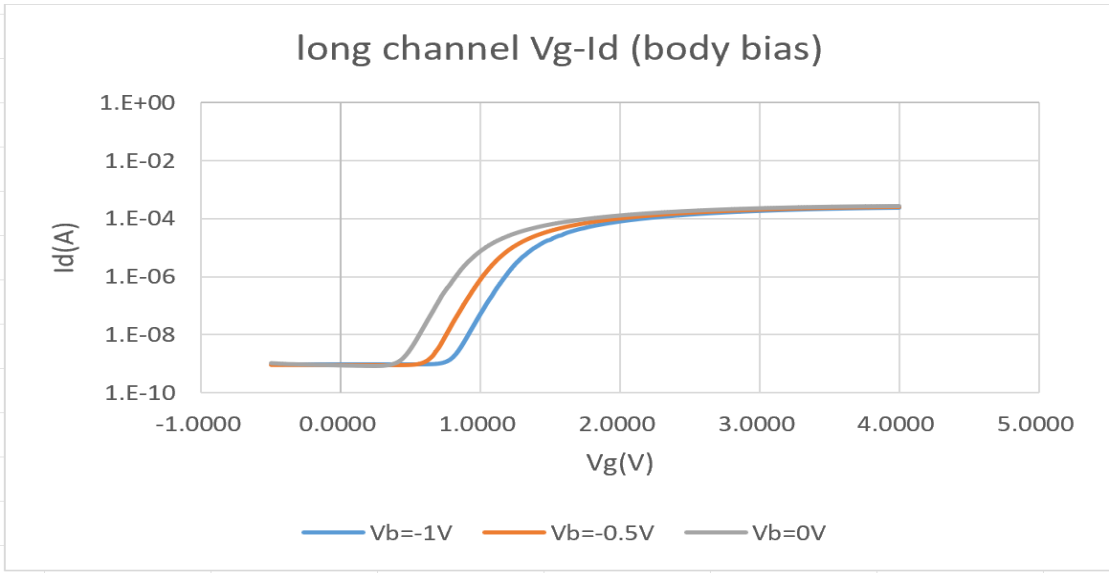
This increase occurs because, according to the operating principle of the MOSFET, as the gate voltage rises, the number of electrons in the channel increases, allowing more drain current to flow. Notably, each curve exhibits a saturation form that flattens out after a certain drain voltage, indicating entry into the saturation region. The drain current remains nearly constant during this phase, and the Id value measured in this region is defined as Id,sat.

Therefore, this experiment enabled quantitative analysis of the MOSFET's Vd–Id characteristic curve and confirmed through actual data how changes in gate voltage affect saturation current and mode transitions.

Finally, the body bias effect was verified by applying a voltage to the MOSFET's body terminal. Theoretically, applying a negative bias to the body terminal increases the potential difference between the body and source, expanding the depletion region and consequently raising the threshold voltage.

The physical principle behind this phenomenon is as follows: When negative body bias is applied, holes within the body are attracted toward the body terminal. Consequently, more fixed negative charge forms near the channel. This requires a stronger electric field from the gate to form the channel, resulting in an increased threshold voltage.

The graph in <Figure 5> below experimentally demonstrates this threshold voltage change with body bias. The figure shows that the highest threshold voltage occurs at the blue curve with the highest negative voltage (Vb = -1V). Therefore, this confirms the pattern where the threshold voltage increases as the body voltage decreases.

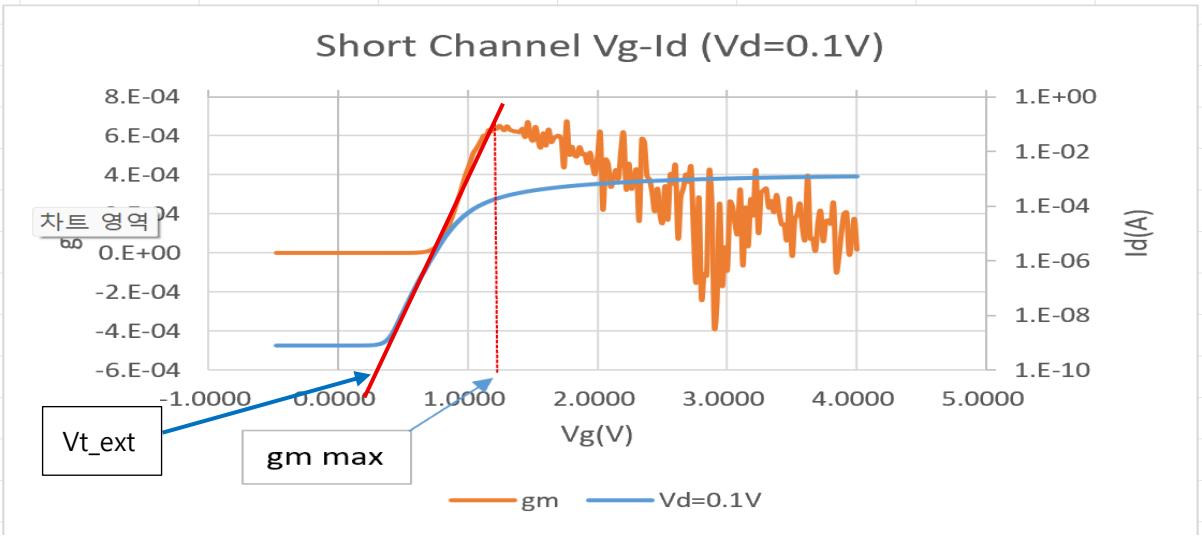


<Figure 5>

B. Short Channel MOSFET

For the Short Channel MOSFET, we analyze the electrical characteristics of a MOSFET with a gate channel length of 0.35μm and a gate width of 10 μm. Based on the measured I–V data, we extract key device parameters such as Threshold Voltage, Subthreshold Swing, and Saturation Current, as in the previous experiment, and interpret them using concepts learned from semiconductor engineering theory.

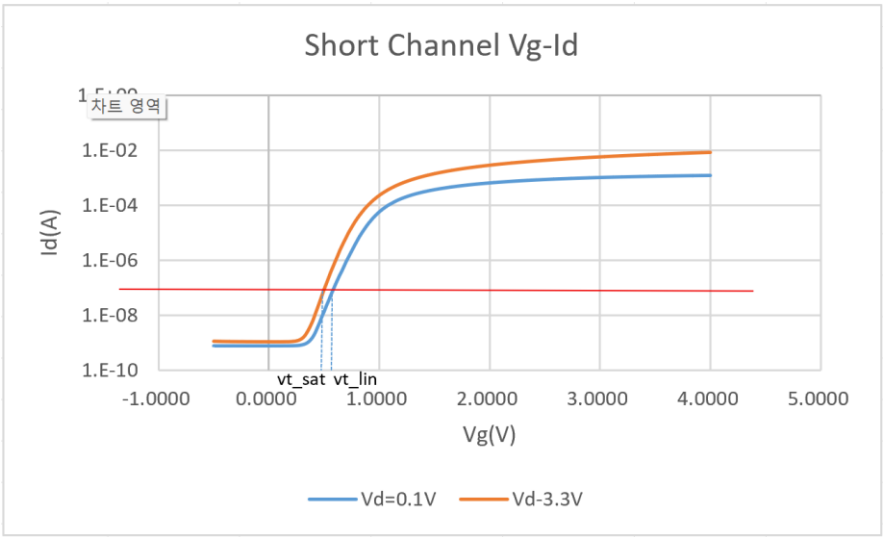
The graph below shows the Vg-Id curve when Vd = 0.1V.



<Figure 6>

At Vd = 0.1 V, gm reached its maximum value around Vg ≈ 1.30 V, indicating the voltage range where the device enters a strong inversion state. By extrapolating this, the Vg value where Id becomes zero was determined. Subtracting 0.05 V from this value yielded Vt_ext ≈ 0.3 V.

Next, based on the above graph, Vt_lin and Vt_sat values were determined to characterize the DIBL effect in this device. The graph showing Vt_lin and Vt_sat is as follows.



<Figure 7>

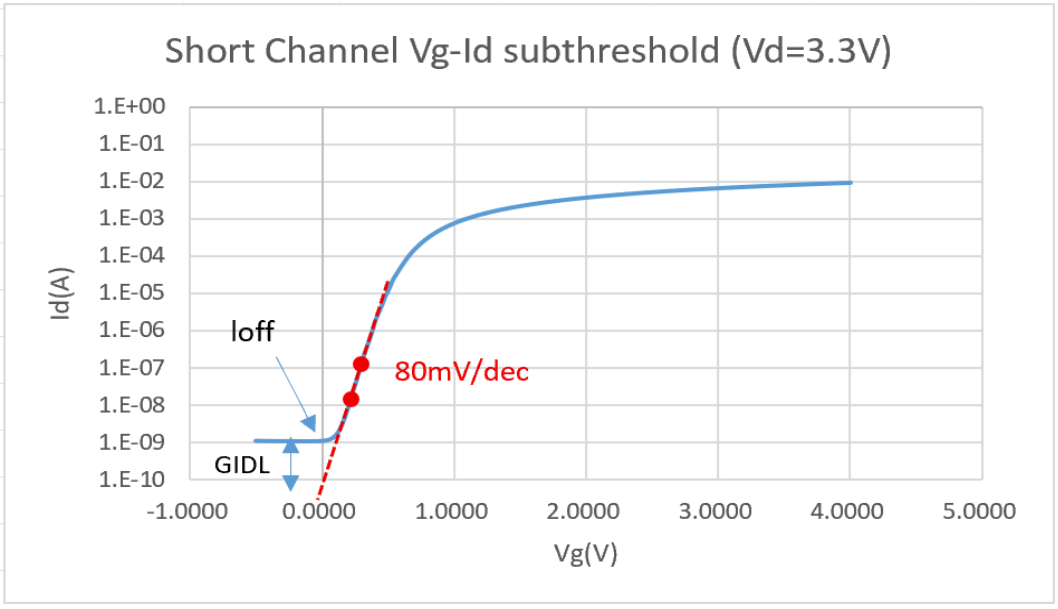
Based on the data from the graph above, the extracted values for Vt_sat and Vt_lin are Vt_sat=0.72V and Vt_lin=0.84V. Since the data did not show a perfect10^{-7} , these values were extracted from nearby points. These two parameters are crucial for observing the DIBL effect in this device, specifically the Short Channel TR. Using these two values, DIBL is calculated as follows.

$$DIBL \approx \frac{Vt_{lin} - Vt_{sat}}{Vd_{sat} - Vd_{lin}} = \frac{120mV}{3.2V} = 37.5mV/V$$

This is a quantitative indicator of the phenomenon where the threshold voltage decreases as the drain voltage increases in a short channel MOSFET. Through the above calculation, it was confirmed to have a value of approximately 37.5mV/V. This figure indicates the degree of the short channel effect present in this device. A smaller DIBL value signifies that the gate maintains better control over the channel. Transistors with DIBL values below 100 mV/V are generally considered high-performance, and this transistor sufficiently meets that criterion.

Therefore, the observed DIBL value in this experiment indicates that the MOSFET exhibits a certain degree of short channel characteristics and that the threshold voltage varies with drain voltage. This analysis provides an important benchmark for future device design and optimization, and this characteristic becomes increasingly critical as device scaling progresses.

Next, we extract the Vg-Id graph at Vd=3.3V to analyze key parameters of this device: subthreshold swing, Ioff, and GIDL current. The corresponding graph is shown below.



<Figure 8>

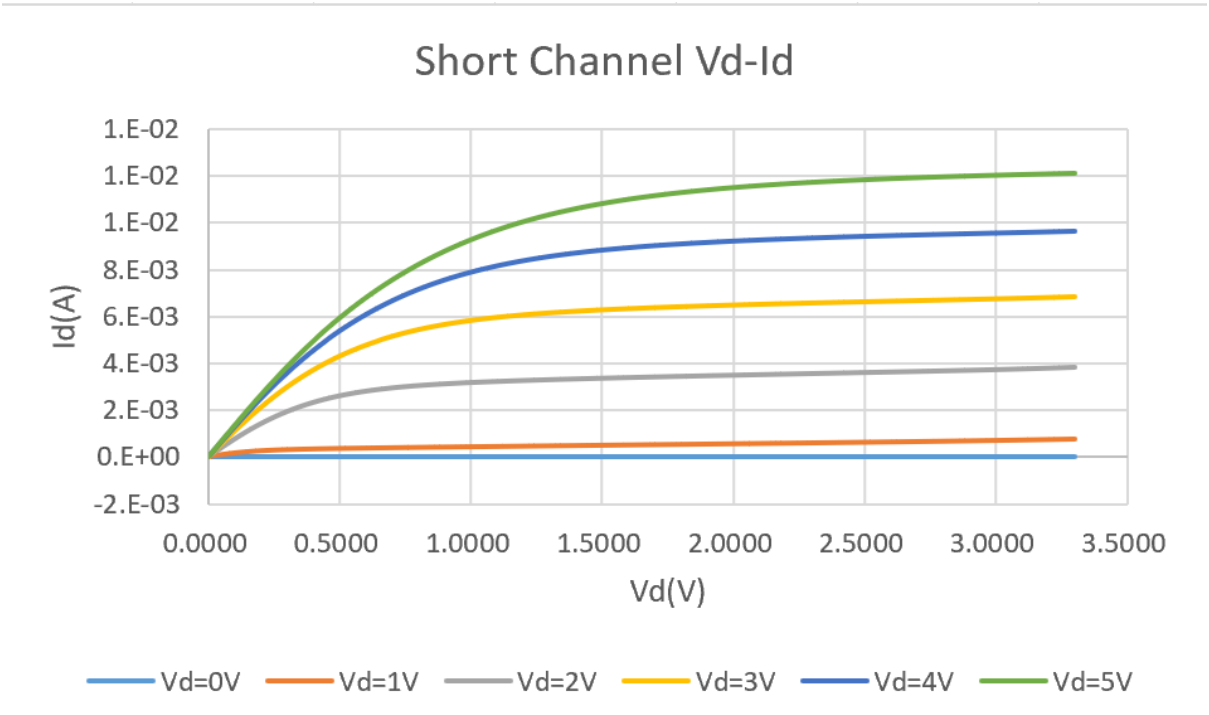
Three key parameters can be identified from the graph above. First, the Subthreshold swing (SS) can be extracted from the region where the current increases exponentially, showing a slope of approximately 80 mV/dec. This is larger than the theoretical SS value of 60 mV/dec for an ideal

MOSFET but represents an improvement over Long Channel MOSFETs. This indicates the device's gate control capability is limited and carrier control in the channel is degraded beyond thermal limits. Possible causes for this increased SS include short channel effects, trap states, and body bias effects.

Furthermore, GIDL (Gate-Induced Drain Leakage) current, as defined above, is tunneling current generated at the drain edge due to strong electric fields when the gate voltage approaches low values. The phenomenon where current appears in the negative gate voltage region in the graph is attributed to GIDL, significantly impacting the device's leakage current characteristics. It is a major factor increasing standby power consumption, especially in high-voltage operating environments.

Finally, Ioff (off-state leakage current) is defined as the drain current when the gate voltage is 0V. In the graph, it appears at approximately 0.10^{-9} A. This value is directly related to the circuit's standby power consumption and plays a crucial role in ensuring power efficiency and stability in the off state. A smaller Ioff value indicates lower leakage current, which is advantageous for low-power system design.

Next, the Vd-Id data for the Short Channel TR was extracted and plotted graphically.



<Figure 9>

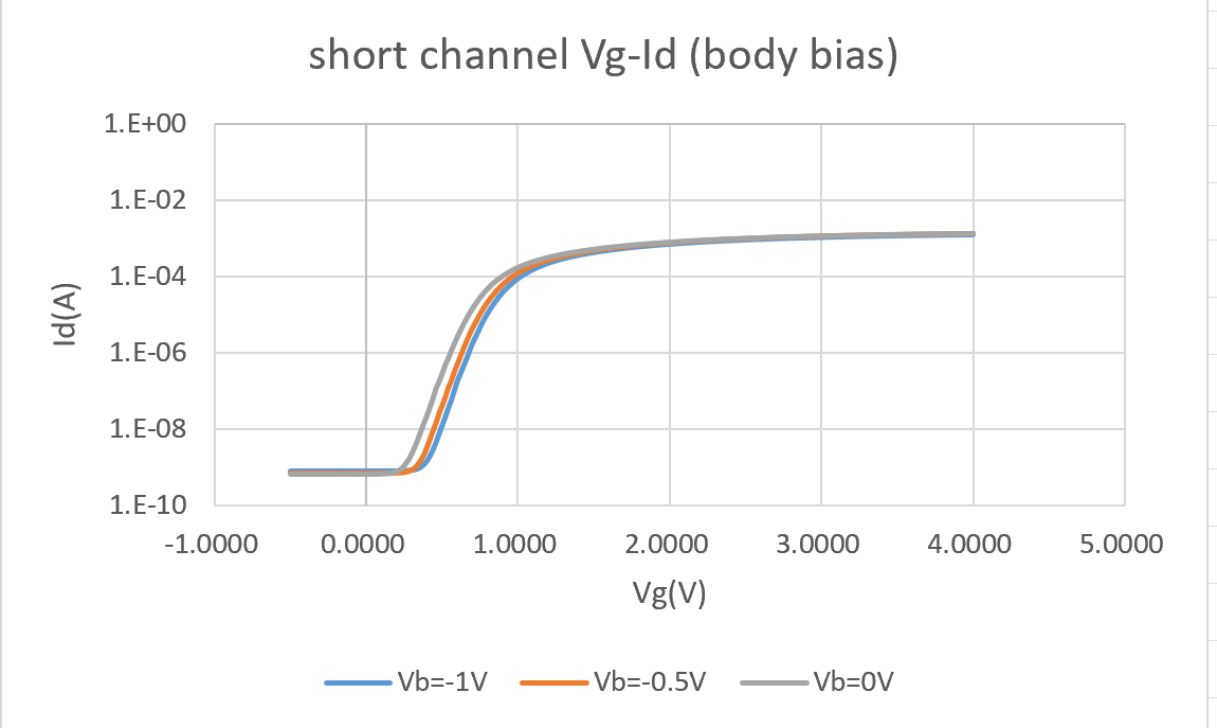
This graph shows the variation in drain current (Id) measured by changing the drain voltage (Vd) for each gate voltage (Vg) while varying Vg from 0V to 5V in 1V increments in a Short Channel MOSFET.

Overall, Id tends to increase sharply as Vg increases. This is based on the physical principle that a higher gate voltage strengthens channel inversion and enhances current carrier mobility.

As Vd increases, Id initially rises linearly. Beyond a certain Vd, the rate of increase slows, indicating entry into the saturation region. However, due to the short channel effect, Id does not become completely flat in saturation but continues to increase gradually. This phenomenon is associated with channel length modulation, where increasing drain voltage reduces part of the channel length.

That is, while an ideal long-channel device should maintain a constant Id in the saturation region, the short-channel device in this experiment exhibits a saturation current that depends on the drain voltage and increases gradually as the effective channel length decreases. This is one of the representative current-voltage characteristics of short-channel MOSFETs and is an important consideration in digital circuit design or when analyzing the output resistance characteristics of analog circuits.

Finally, similar to the long-channel MOSFET, the body bias effect was verified by applying body bias to the short-channel MOSFET. The measurement results are as follows.



<Figure 10>

The graph above shows the Vg-Id characteristics when voltages (Vb) of 0V, -0.5V, and -1V are applied, respectively. As Vb decreases, i.e., as a more negative voltage is applied, the curve shifts to the right, showing a tendency for the threshold voltage to increase. This is a typical phenomenon due to the body bias effect: applying a negative voltage to the body lowers the potential in the body region, requiring a higher gate voltage to satisfy the inversion condition.

Therefore, at the same drain voltage, when Vb is -1V, current begins to flow at a higher Vg than when Vb is 0V, and the onset of current increase is delayed. This indicates an increase in the threshold voltage and demonstrates that the device's operating point can be controlled via body bias.

In conclusion, it was experimentally confirmed that body bias is an effective method for controlling the threshold voltage even in short-channel MOSFETs.

Ⅲ. Conclusion

Through this experiment, we quantitatively verified the characteristic changes of MOSFETs according to channel length and directly analyzed the device's electrical behavior not only theoretically but also through actual measurements. This experience significantly aided in gaining a more intuitive understanding of the fundamental operating principles of semiconductor devices. It was also a meaningful learning process, as it provided hands-on practice with various basic device characterization techniques, such as threshold voltage extraction, subthreshold swing calculation, and leakage current analysis.

Future research should consider variations in device characteristics due to various external variables, such as oxide thickness and temperature, in addition to channel length. This will enhance analytical capabilities under conditions closer to actual process environments. Furthermore, expanding the understanding of structural improvement techniques (LDD, FinFET, GAA, etc.) to mitigate experimentally verified short channel effects like DIBL and GIDL, and comparing predictive modeling using simulation tools (TCAD, etc.) with experimental results, could also be important research directions.

As a student, I believe it is crucial to develop an integrated perspective that connects these device characteristics to circuit-level applications. Moving beyond merely understanding individual device parameters, I plan to continue my studies by grasping how these characteristics impact actual circuits and expanding my understanding to encompass semiconductor design, process technology, and system-level concepts.