ME910X1 – mPCIe

Hardware Design Guide

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Contents

1 Applicability Table 4
2 Introduction 5
2.1 Scope 5
2.2 Audience 5
2.3 Contact Information, Support 5
2.4 Conventions 5
2.5 Terms and Conditions 6
3 General Product Description 7
3.1 Overview 7
3.2 Product Variants and Frequency Bands 7
3.3 Target Market 7
3.4 Main Features 8
3.5 TX Output Power 8
3.6 RX Sensitivity 9
3.7 Mechanical Specifications 9
3.7.1 Dimensions 9
3.7.2 Weight 9
3.8 Temperature Range 9
4 Pins Allocation 10
4.1 Pin-out 10
5 Power Supply 13
5.1 Power Supply Requirements 13
5.2 Power Consumption 13
5.3 General Design Rules 13
5.3.1 Electrical Design Guidelines 13
1.1.1.1. +5V Source Power Supply Design Guidelines 14
1.1.1.2. +12V Source Power Supply Design Guidelines 14
5.3.2 Thermal Design Guidelines 15
5.3.3 Power Supply PCB Layout Guidelines 16
6 Electrical Specification 19
6.1 Absolute Maximum Ratings – Not Operational 19
6.2 Recommended Operating Conditions 19
7 Digital Section 20
7.1 Logic Levels 20
7.1.1 Absolute Maximum Ratings 20
7.1.2 Operating Range Digital Signals (CMOS 1.8V) 20
7.1.3 Operating Range – Sim Card Pads @2.95V 21
7.2 Power On 21
7.3 Unconditional Restart 24
7.4 Power OFF Procedure 26
7.5 Control Signals 27
7.5.1 W_DISABLE_N and PERST_N 27
7.5.2 LED_WWAN_N 27
7.6 Hardware Interfaces 28
7.6.1 USB Port 28

7.6.2 Serial Port 29
1.1.1.3. RS232 Level Translation 30
7.7 SIM Interface 31
8 RF SECTION 33
8.1 Bands Variants 33
8.2 TX and RX Characteristics 33
8.3 Antenna Requirements 33
8.3.1 Antenna Connectors 33
8.3.2 Main GSM/LTE Antenna Requirements 34
8.3.3 GNSS Antenna Requirements 34
1.1.1.4. Combined GNSS Antenna 35
1.1.1.5. Linear and Patch GNSS Antenna 35
9 Mechanical Design 36
9.1 Mechanical Dimensions 36
9.2 Mechanical Drawing 36
9.2.1 Top View 36
9.2.2 Bottom View 37
9.2.3 Side View 37
10 Application PCB Design 38
10.1 Recommended Footprint for the Application 38
11 EMC Recommendations 39
12 Packing System 40
12.1 Tray 40
12.2 Tray Drawing 42
13 Conformity Assessment Issues 43
13.1 Declaration of Conformity 43
14 Reference Table of RF Bands Characteristics 44
15 Acronyms and Abbreviations 46
16 Related Documents 47
17 Document History 48

1 Applicability Table

Table 1: Applicability Table

Products
ME910C1-WW
ME910G1-WW

2 Introduction

2.1 Scope

This document describes some hardware solutions useful to develop a product with the Telit ME910X1 Mini PCIe Adapter (mPCIe)..

2.2 Audience

This document is intended for system integrators that are using the Telit ME910X1 Mini PCIe Adapter in their products.

2.3 Contact Information, Support

For technical support and general questions, e-mail:

- TS-EMEA@telit.com
- TS-AMERICAS@telit.com
- TS-APAC@telit.com
- TS-SRD@telit.com
- TS-ONEEDGE@telit.com

Alternatively, use: https://www.telit.com/contact-us/

For Product information and technical documents, visit: https://www.telit.com

2.4 Conventions

Note:	Provide advice and suggestions that may be useful when integrating the module.
Danger:	This information MUST be followed, or catastrophic equipment failure or personal injury may occur.
Warning:	Alerts the user on important steps about the module integration.

All dates are in ISO 8601 format, that is YYYY-MM-DD.

2.5 Terms and Conditions

Refer to https://www.telit.com/hardware-terms-conditions/.

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3 General Product Description

3.1 Overview

This document presents possible and recommended hardware solutions useful for developing a product with the Telit ME910X1-mPCIe module.
ME910X1-mPCIe is a Telit platform for Mini PCIe applications, such as M2M applications, and tablet PC, based on the following technologies:

- LTE / WCDMA networks for data communication
- Designed for industrial grade quality

In its most basic use case, the ME910X1-mPCIe can be applied as a wireless communication front-end for mobile products, offering mobile communication features to an external host CPU through its rich interfaces. ME910X1-mPCIe can further support customers' software applications and security features. ME910X1-mPCIe provides a software application development environment with sufficient system resources to create rich on-board applications. Thanks to a dedicated application processor and embedded security resources, product developers and manufacturers can create products that guarantee fraud prevention and tamper evidence without extra effort for additional security precautions.
ME910X1-mPCIe hardware is available in different board and band variants as listed in section 3.2 Product Variants and Frequency Bands.

3.2 Product Variants and Frequency Bands

ME910X1 modules bands combinations are listed below:

Table 2: Product Variants and Frequency Bands

Product	2G Band	4G Band	Region
ME910C1-NA		2, 4, 12	North America
ME910C1-WW	2, 3, 5, 8	1, 3, 5, 8, 18, 19, 26, 28	World Wide
ME910G1-WW	2, 3, 5, 8	B1, B2, B3, B4, B5, B8, B12, B13, B18, B19, B20, B25, B26, B27, B28, B66, B71, B85	World Wide

For details information about frequencies and bands, refer to Chapter 14 Reference Table of RF Bands Characteristics

3.3 Target Market

ME910X1-mPCIe can be used for a wide variety of applications, where low power consumption and low cost are required while sufficient data rates are achieved:

- Applications using the mPCIe connector
- Notebook PC
- M2M applications

3.4 Main Features

Table 3: Main Features

Function	Features
Modem	Multi-RAT cellular modem for voice and data communication LTE FDD Catx data rates per the module variant used. Carrier aggregation is not supported GSM/GPRS/EDGE (when available) Regional variants with optimal choice of RF bands coverage of countries and MNOs State-of-the-art GNSS solution with GPS/GLONASS/BeiDou/Galileo/QZSS receiver
USIM ports – dual voltage	Class B and Class C support Hot-swap support Clock rates up to 4 MHz
Application processor	Application processor to run customer application code • Flash + DDR are large enough to allow for customer's software applications
Interfaces	USB2.0 – USB port is typically used for: Flashing of firmware and module configuration Production testing Accessing the Application Processor's file system AT command access High-speed WWAN access to an external host Diagnostic monitoring and debugging Communication between Java application environment and an external host CPU NMEA data to an external host CPU Peripheral Ports – I2S, UART GPIOs Antenna ports
Form factor	Full-Mini Card 52 pin, 50.95mm x 30mm x 1mm.
Environment and quality requirements	The entire module is designed and qualified by Telit for satisfying the environment and quality requirements.
Single supply module	The module generates all its internal supply voltages.
RTC	No dedicated RTC supply, RTC is supplied by 3V3_AUX

3.5 TX Output Power

Table 4: TX Output Power

Technology	Power (dBm)
2G LB	32 (when available)
2G HB	29 (when available)
4G FDD	23 @1RB

3.6 RX Sensitivity

Table 5: RX Sensitivity

Technology	Sensitivity (dBm)
2G	-107 (when available)
4G FDD (BW=5 MHz)	-102

3.7 Mechanical Specifications

3.7.1 Dimensions

The overall dimensions of the ME910X1-mPCIe family are:

- Length: 50.95 mm, +0/-0.3mm
- Width: 30 mm, +0/-0.3mm
- Thickness:
  - **ME910G1-mPCIe:** 3.4 mm, +/-0.15mm (Version with SIM holder : 4.9 mm, +/-0.15mm)
  - **ME910C1-mPCIe:** 3.2 mm, +/-0.15mm (Version with SIM holder : 4.7 mm, +/-0.15mm)

3.7.2 Weight

The nominal weight of the mPCIe card is about 7 grams.

3.8 Temperature Range

Table 6: Temperature range

Case	Range	Note
Operating Temperature Range	–20°C ~ +55°C	The module is fully functional(*) in all temperature ranges, and it fully meets the 3GPP specifications.
	–40°C ~ +85°C	The module is fully functional (*) in all temperature ranges. However, there may be some performance deviations in this extended range relative to 3GPP requirements, which means that some RF parameters may deviate from the 3GPP specification in the order of a few dB. For example, receiver sensitivity or maximum output power may be slightly degraded
Storage and non-operating Temperature Range	–40°C ~ +105°C	Storage temperature is not intended for mPCIe in his transport tray, which cannot be heated over 65°C.

Note: Functional: The module can make and receive calls, data connections, and SMS

4 Pins Allocation

4.1 Pin-out

ME910X1 mPCIe Pinout follows the mPCIe specification [4]

Table 7: Pin-out

Pin	Signal	I/O	Function	Type	Comment
Power Supply					
2	3V3_AUX	-	3.3V Main Power Supply	Power	
39	3V3_AUX	-	3.3V Main Power Supply	Power	
41	3V3_AUX	-	3.3V Main Power Supply	Power	
52	3V3_AUX	-	3.3V Main Power Supply	Power	
4	GND	-	Ground		
9	GND	-	Ground		
15	GND	-	Ground		
18	GND	-	Ground		
21	GND	-	Ground		
26	GND	-	Ground		
27	GND	-	Ground		
29	GND	-	Ground		
34	GND	-	Ground		
35	GND	-	Ground		
37	GND	-	Ground		
40	GND	-	Ground		
43	GND	-	Ground		
50	GND	-	Ground		
USB Interface					
36	USB D-	I/O	USB differential Data (-)		
38	USB D+	I/O	USB differential Data (+)		
UART					
3	UART_RX	I	Serial data input (RX) from DTE	1.8V	See note
5	UART_TX	O	Serial data output (TX) to DTE	1.8V	See note
17	UART_RTS	O	Output Request to Send a signal (RTS) to DTE	1.8V	See note
19	UART_CTS	I	Input for Clear To Send signal (CTS) from DTE	1.8V	See note
I2S – Digital Voice Interface (DVI)					
45	PCM_CLK	I/O	Digital Audio Interface (BIT Clock)	1.8V	Only for ME910G1-WW RESERVED for others

Pin	Signal	I/O	Function	Type	Comment
47	PCM_TX	O	Digital Audio Interface (TX Out of the card)	1.8V	Only for ME910G1-WW RESERVED for others
49	PCM_RX	I	Digital Audio Interface (RX Into the card)	1.8V	Only for ME910G1-WW RESERVED for others
51	PCM_SYNC	I/O	Digital Audio Interface (Frame_Sync)	1.8V	Only for ME910G1-WW RESERVED for others
16	REF_CLK	O	Reference clock for external Codec	1.8V	Reserved
SIM Card Interface					
8	SIMVCC	I/O	External SIM signal SIM Power Supply	1.8 / 3V	
10	SIMIO	I/O	External SIM signal Data I/O	1.8 / 3V	
12	SIMCLK	O	External SIM signal Clock	1.8 / 3V	
14	SIMRST	O	External SIM signal Reset	1.8 / 3V	
Miscellaneous Functions					
1	WAKE_N	O	Active Low output signal Wake Up signal to the host system	3V3_AUX	
6	1V5	O	1V5 Power Supply	Power	Not Used
20	W_DISABLE_N	I	Active Low Input Signal: Shutdowns Wireless disabling (Flight mode)	3V3_AUX	Already has an internal 100K PU to 3V3_AUX
22	PERST_N	I	Active Low Input Signal Shutdowns	3V3_AUX	Should be externally PU to 3V3_AUX
24	3V3	-	3.3V Digital Power Supply	Power	Not Used
28	1V5	O	1V5 Power Supply	Power	Not Used
42	LED_WWAN_N	O	Open Drain circuitry LED driving, for module's status indication		LED should be PU externally in series to 3V3_AUX
48	1V5	O	1V5 Power Supply	Power	Not Used
Reserved					
7	Reserved	-			
11	Reserved	-			
13	Reserved	-			
16	Reserved	-			
23	Reserved	-			
25	Reserved	-			
30	Reserved	-			

Pin	Signal	I/O	Function	Type	Comment
31	Reserved	-			
32	Reserved	-			
33	Reserved	-			
44	Reserved	-			
46	Reserved	-			

Warning: Reserved pins must be left floating.

Warning: 3V3 and 1V5 Power Supply at Connector are not used on the board.

They can be left connected to existing power or disconnected.

Note: UART pins are NOT available only in the following P/N:

- MEPCHC1WW05T080100

5 Power Supply

The power supply circuitry and board layout are a very important part of the full product design and strongly reflect on the product overall performances, so please read carefully the requirements and guidelines that will follow for a proper design.

5.1 Power Supply Requirements

The external power supply must be connected to the 3V3_AUX signal and must fulfill the following requirements:

Table 8: Power Supply Requirements

Parameter	Values
Nominal Supply Voltage	3.3V
Supply Voltage Range	3.0V ~ 3.6V
Max ripple on the module input supply	30mV

Note: The Operating Voltage Range MUST never be exceeded; care must be taken when designing the power supply section of the application to avoid having an excessive voltage drop.

If the voltage drop exceeds the limits it could cause a Power Off of the module.

The Overshoot voltage (regarding the MAX Extended Operating Voltage) and drop in voltage (regarding the MIN Extended Operating Voltage) MUST never be exceeded.

The “Extended Operating Voltage Range” is intended as the worse case between this document and those related to the module mounted and can only be used in non-standard mPCIe application, custom design, with complete assumption and application of the HW User Guide [1] [5]suggestions.

5.2 Power Consumption

For the complete power consumption specification, refer to the specific Module’s HW User Guide [1] [5].

5.3 General Design Rules

The principal guidelines for the Power Supply Design embrace three different design steps:

- The electrical design
- The thermal design
- The PCB layout.

5.3.1 Electrical Design Guidelines

The electrical design of the power supply depends strongly on the power source where this power is drained.

- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)

1.1.1.1. +5V Source Power Supply Design Guidelines

- The desired output for the power supply is 3.3V. Since there is not much difference between the input and the output voltage values, and a linear regulator can be used.
- When using a linear regulator, a proper heat sink shall be necessary to dissipate the generated heat.
- Since 5V is generally supplied directly from USB, be careful not to have more than 10uF at input and that USB supplies an appropriate amount of current, about 1A.
- A Bypass low ESR capacitor of adequate capacity must be provided to cut the current absorption peaks close to the Module, a 100µF capacitor is usually suitable.
- Make sure the low ESR capacitor on the power supply output is rated at least 10V.

An example of the linear regulator with 5V input and 3A@3V3 output is shown here below.

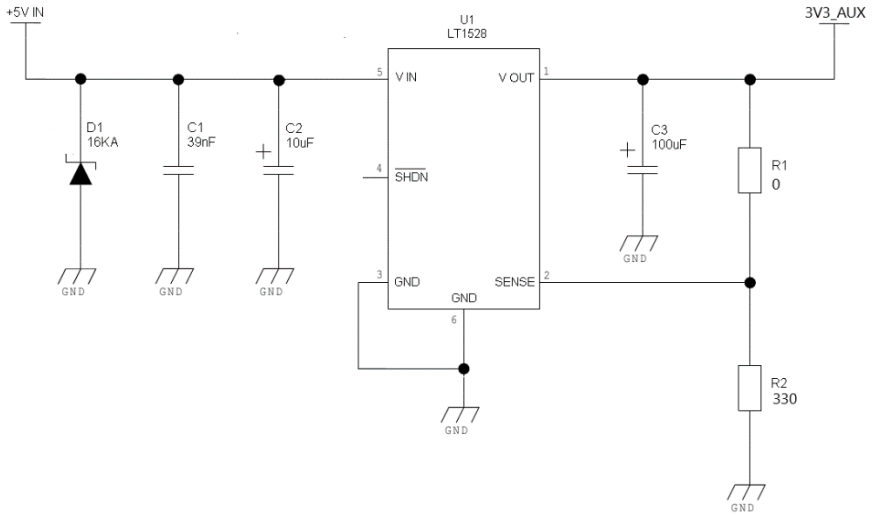


Figure 1: Linear regulator with 5V input and 3.3V output

1.1.1.2. +12V Source Power Supply Design Guidelines

- The desired output for the power supply is 3.3V. Due to the large difference between the input and output voltage values together with the current sinked, the linear regulator in the example above is capable but not efficient at a high current sink and should not be used. A switching power supply will be preferable due to its better efficiency.
- When using a switching regulator, a 500kHz or more switching frequency regulator is preferable because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peak absorption.
- In any case the frequency and Switching design selection are related to the application to be developed since the switching frequency could also generate EMC interferences.
- For a car PB battery the input voltage can rise up to 15.8V and this should be kept in mind when choosing components: all components in the power supply must withstand this voltage.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF capacitor is usually suitable.
- Make sure the low ESR capacitor on the power supply output is rated at least 10V.
- For Car applications, a spike protection diode should be inserted close to the power input to clean the supply from spikes.

An example of a switching regulator with VIN=4V-36V input and 2.5A@3V3 output is shown here below.

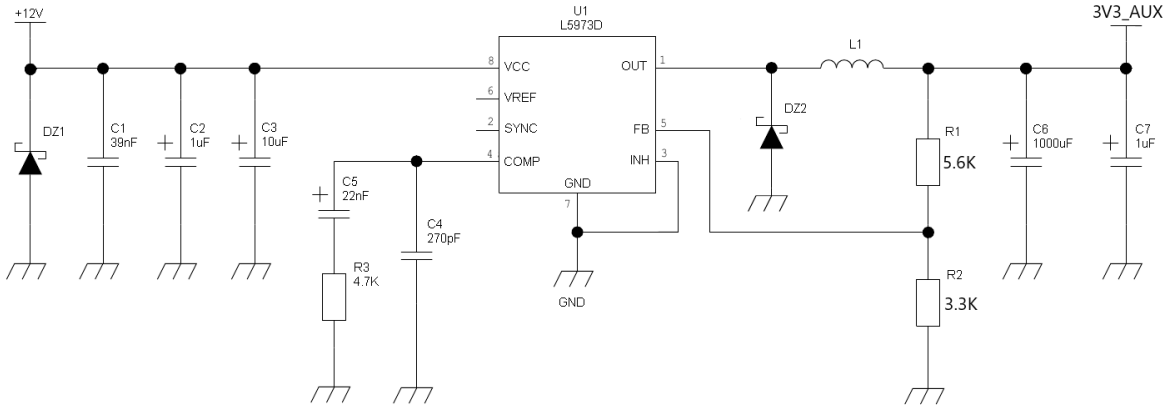


Figure 2 Switching regulator with 4V-36V input and 3.3V output

5.3.2 Thermal Design Guidelines

The thermal design of the application board and the power supply heat sink should be done with the following specifications:

- Typical LTE average current consumption during ME910X1 mPCIe transmission at a maximum Power level and the minimum input voltage: 700 mA
- Average current during idle (USB enabled): 30 mA
- Average current during idle (USB disabled): 5 mA
- Average current during airplane mode (USB disabled): 2 mA

Considering the very low current during Idle, especially if the Power Saving function is enabled, it is possible to consider from the thermal point of view that the device absorbs a significant current mainly during the Data session. In LTE mode, the ME910X1 mPCIe emits RF signals continuously during transmission. Therefore, special attention must be paid to how to dissipate the heat generated.

The ME910X1 mPCIe card is designed to distribute the heat from the module IC's to the entire PCB increasing as much as possible the heat dissipation.

For best performance, the application board copper layers should be used to dissipate the heat out of the mPCIe card.

To ensure proper thermal flow from the mPCIe card to the application board, the mPCIe card's bottom side should be thermally connected to the application's board top side via an appropriate thermal pad.

The area that the thermal pad is attached to on the application board must be designed as a large ground pad (with the solder mask exposed).

Note: The average consumption during transmissions depends on the input voltage and the power level at which the device is requested to transmit by the network. The average current consumption hence varies significantly.

5.3.3 Power Supply PCB Layout Guidelines

Some ME910X1 versions have GSM capabilities. The GSM system is designed in such a way that the RF transmission is not continuous, otherwise it is packed into bursts at a base frequency of about 216 Hz, and the related current peaks can be as high as about 2.4A. The average current should be considered 1A. Therefore, the power supply must be designed to withstand these current peaks and average without large voltage drops; this means that both the electrical design and the board layout must be designed for this current flow. If the voltage drop during the peak current absorption is too high, the device may even shutdown due to the input supply voltage drop.

Note: The electrical design for the Power supply should be made so that it is capable of a peak current output of at least 2.4 A.

As seen in the electrical design guidelines the power supply shall have a low ESR capacitor on the output to help during the current peaks and protect the supply,

especially DC/DC, from positive and negative spikes. Negative spikes can damage the module. The placement of this component is crucial for the correct functioning of the circuitry. A misplaced component can be useless or can even decrease the power supply performance.

- The Bypass low ESR capacitor must be placed close to the Telit ME910X1-mPCIe power input pads or in the case, the power supply is a switching type it can be placed close to the inductor to cut the ripple provided the PCB trace from the capacitor to the ME910X1-mPCIE is wide enough to ensure a dropless connection even during the 2A current peaks.
- A protection diode must be placed close to the input connector where the power source is drained.
- The PCB traces from the input connector to the power regulator IC must be wide enough to ensure that no voltage drops occurs when a 2A current peak is absorbed.
- Any PCB power traces to the ME910X1-mPCIE and the Bypass capacitors must be wide enough to ensure no significant voltage drops occurs. This is for the same reason as previous point. Try to keep this trace as short as possible.
- To reduce the EMI due to switching, it is important to keep the mesh involved very small; therefore the input capacitor, the output diode (if not embodied in the IC) and the regulator must form a very small loop. This is done to reduce the radiated field (noise) at the switching frequency (100-500 kHz usually).
- A ground island around Switching regulator components on top layer but well connected to the common system ground plane in inner layer can help to reduce noise distribution and consequent spurious generation.
- The placement of the power supply on the board should be done in such a way as to guarantee that the high current return paths in the ground plane are not overlapped by any noise-sensitive circuitry as the microphone amplifier/buffer or earphone amplifier.
- The power supply input cables should be kept separate from noise-sensitive lines such as microphone/earphone cables.
- The insertion of an EMI filter on 3V3_AUX pins is suggested in those designs where antenna is placed close to the battery or supply lines.
- A ferrite bead-like Murata BLM18EG101TN1 or Taiyo Yuden P/N FBMH1608HM101 can be used for this purpose, they are a good low band pass filters with a frequency cut of about 100MHz.

The below figure shows the recommended circuit:

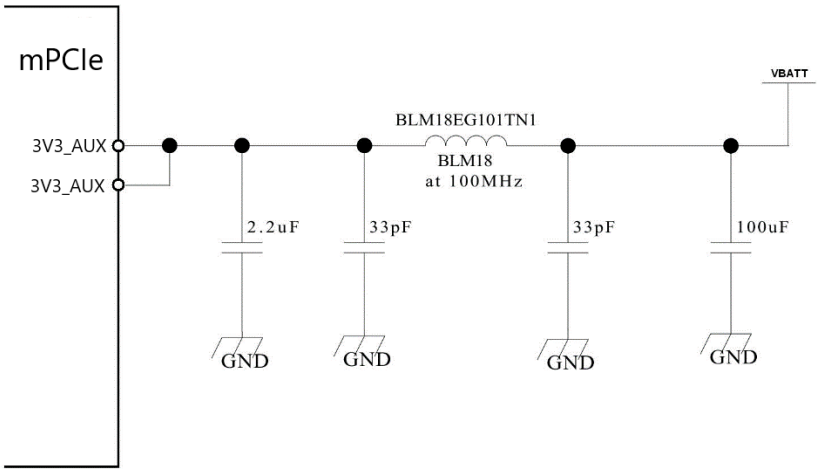


Figure 3: Power supply EMI filtering recommended circuit

6 Electrical Specification

6.1 Absolute Maximum Ratings – Not Operational

Warning: A deviation from the value ranges listed below may harm the module.

Table 9: Absolute Maximum Ratings – Not Operational

Symbol	Parameter	Min	Max	Unit
3V3_AUX	Main Supply Voltage at pins 3V3_AUX	-0.5	4.2	[V]

6.2 Recommended Operating Conditions

Table 10: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Tamb	Ambient temperature	-40	+25	+85	[°C]
3V3_AUX	Main Supply Voltage at pins 3V3_AUX	3.0	3.3	3.6	[V]
I3V3_AUX	Peak current to be used to dimension decoupling capacitors at pins 3V3_AUX	-	-	2400	[mA]

7 Digital Section

7.1 Logic Levels

All digital signals are powered from the internal module's VIO power bank, VIO=1.8V.

All control signals are powered from the external 3V3_AUX power bank, 3V3_AUX=3.3V.

7.1.1 Absolute Maximum Ratings

Table 11: Absolute Maximum Rating digital signals (CMOS 1.8V)

Parameter	Min	Max
Input High Voltage on digital signals (CMOS 1.8) with respect to ground when 3V3_AUX is supplied	-0.3V	2.1V
Input High Voltage on digital signals (CMOS 1.8) with respect to ground when 3V3_AUX is not supplied	-0.3V	0.3V

Table 12: Absolute Maximum Rating for control signal

Parameter	Min	Max
Input Voltage on control signals with respect to ground when 3V3_AUX is supplied	-0.3V	5V
Input Voltage on control signals with respect to ground when 3V3_AUX is not supplied	-0.3V	0.3V

7.1.2 Operating Range Digital Signals (CMOS 1.8V)

Table 13: Operating range digital signals (CMOS 1.8V)

Parameter	Min	Max
Input High Voltage	1.2V	1.85V
Input Low Voltage	0V	0.6V
Output High Voltage	1.4V	1.8V
Output Low Voltage	0V	0.45V
Pull-Up Resistance	10kΩ	390kΩ
Pull-Down Resistance	10kΩ	390kΩ
Input Capacitance	--	5pF
Input Leakage Current	-1uA	+1uA
Drive Strength	2mA	3mA

7.1.3 Operating Range – Sim Card Pads @2.95V

Table 14: Operating Range SIM Card Pads

Parameter	Min	Max
Input High Level	2.1V	3.1V
Input Low Level	-0.3V	0.55V
Output High Level	2.25V	3.1V
Output Low Level	0V	0.4V
Input Leakage Current	-10uA	10uA
Pull-Up Resistance	10kΩ	100kΩ
Pull-Down Resistance	10kΩ	100kΩ
Input Capacitance		5pF

7.2 Power On

The ME910X1-mPCIe will automatically Power ON as soon as VBATT applies to the module and W_DISABLE_N and PERST_N are HI. The module is ready for use after the HW power Up and the SW initialization process completes. For this reason, it is impossible to access ME910X1-PCIe during the initialization state.

As shown below the ME910X1-mPCIe becomes operational (in the Activation state) at least 20 seconds after power is applied:

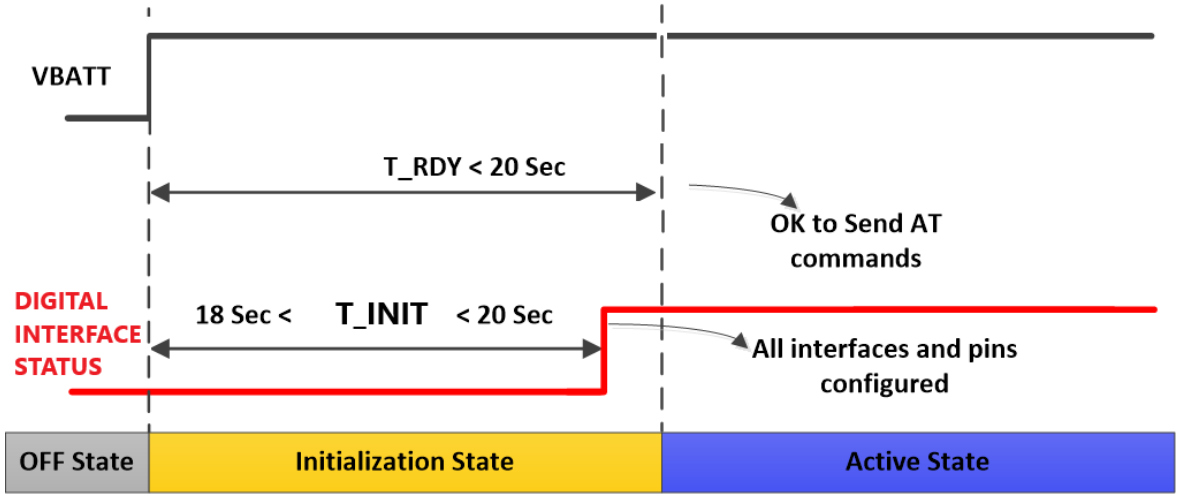


Figure 4: Power On Timing Diagram

Note: To Turn ON the ME910X1-mPCIe module give the 3V3_AUX and release both the PERST_N and W_DISABLE_N pins, they must not be asserted Low.

The following flow chart shows the proper "MODEM TURN ON" procedure:

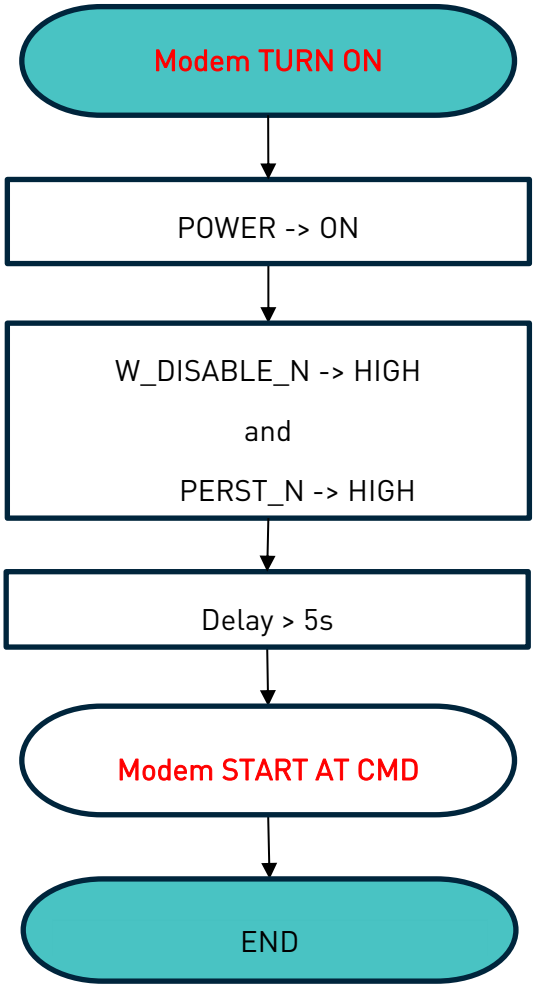


Figure 5: MODEM TURN ON" Procedure

The following flow chart shows the proper "MODEM START AT COMMAND" procedure:

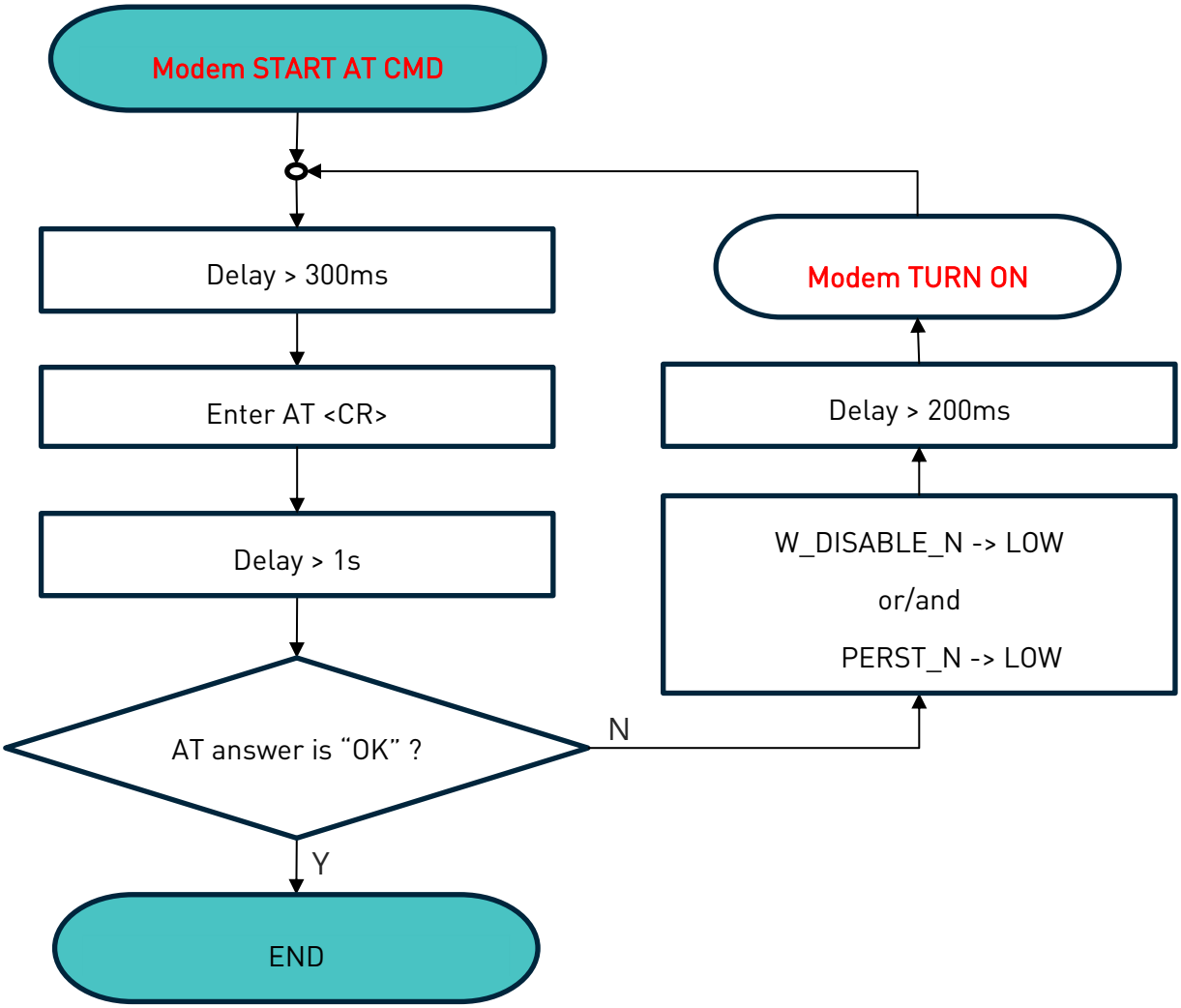


Figure 6: MODEM START AT COMMAND" Procedure

7.3 Unconditional Restart

To unconditionally restart the ME910X1-mPCIe, the signals PERST_N and W_DISABLE_N must be tied low for at least 200 milliseconds and then released.

The unconditional hardware restart must always be implemented on the application board as the software must be able to use it as an emergency exit procedure.

The hardware unconditional restart must not be used during normal operation of the device since it does not detach the device from the network. It should be kept as an emergency exit procedure to be performed in the rare case that the device gets stuck waiting for some network or SIM responses.

W_DISABLE_N and PERST_N are in open drain configuration.

PERST_N needs an external pull-up resistor to 3V3_AUX.

W_DISABLE_N have already an internal pull-up 100K resistor to 3V3_AUX.

Table 15: W_DISABLE_N and PERST_N Pin Description

Signal	Function	I/O	Pin
W_DISABLE_N	Active Low, unconditional shutdown	I	20
PERST_N	Active Low, unconditional shutdown	I	22

Warning: The W_DISABLE and PERST_N signals are hardware unconditional SHUTDOWN and should not be used during normal device shutdown operation as it does not detach the device from the network and can harm the memory content.

It shall be kept as an emergency exit procedure.

To use W_DISABLE_N and PERST_N as Unconditional Hardware Shutdown first Safety Prepare the module to it, by using the AT commands: AT#SYSHALT for ME910C1 mPCIe and AT#SHDN for ME910G1 mPCIe. See AT command [2] [6].

Failure to follow the recommended Power OFF and RESTART procedure will void the warranty.

The following flow chart shows the proper “MODEM RESTART” procedure:

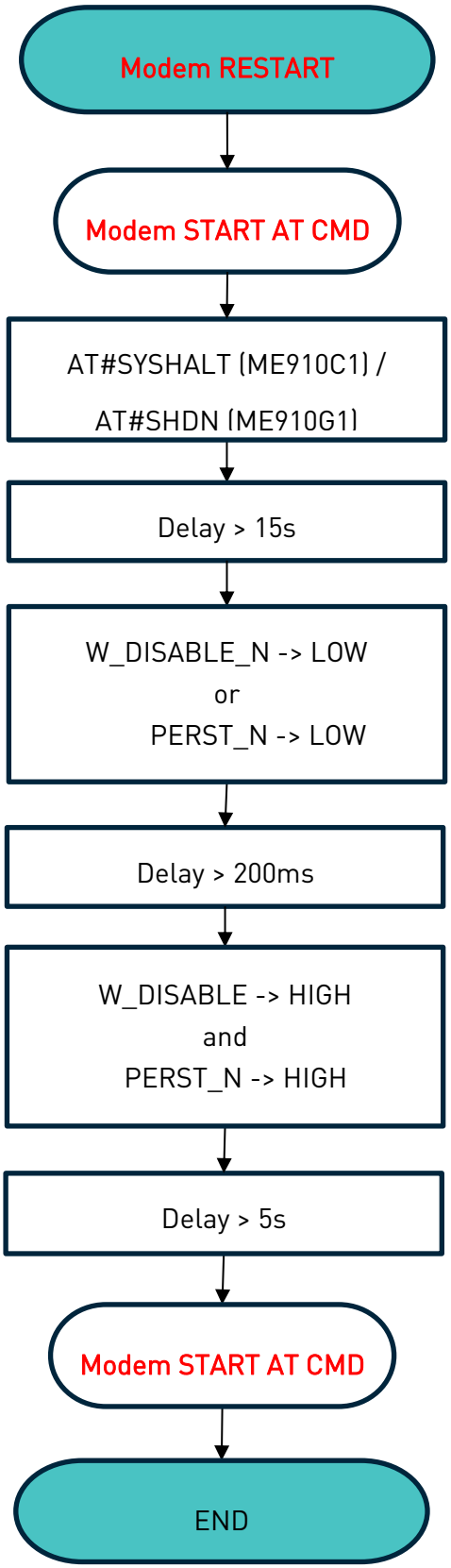


Figure 7: MODEM RESTART” procedure

7.4 Power OFF Procedure

To turn OFF the ME910X1-mPCIe module, the W_DISABLE_N and/or PERST_N signals must be asserted Low.

For proper shutdown operation with correct network detach and memory access disabled, first prepare the module to shutdown by using AT#SYSHALT command for ME910C1 mPCIe and AT#SHDN command for ME910G1 mPCIe.

The duration of the finalization state can differ according to the current status of the module, so a fixed value cannot be defined.

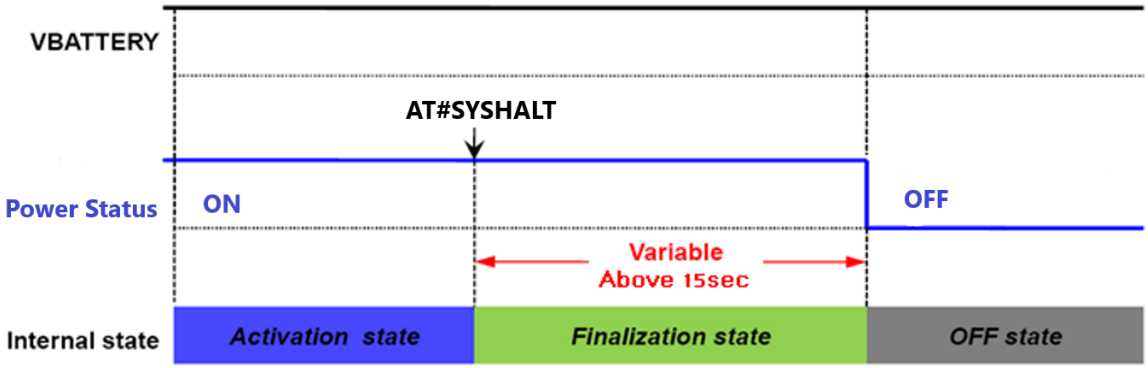


Figure 8 Shutdown using AT#SYSHALT Command

Warning: The W_DISABLE and PERST_N signals are hardware unconditional SHUTDOWN and must not be used during normal shutdown operation of the device since it does not detach the device from the network and can harm the memory content.

It shall be kept as an emergency exit procedure.

To use W_DISABLE_N and PERST_N as Unconditional Hardware Shutdown first Safety Prepare the module to it, by using the AT commands: AT#SYSHALT for ME910C1 mPCIe and AT#SHDN for ME910G1 mPCIe. See AT command [2] [6].

7.5 Control Signals

Table 16: Control Signals

Pin	Signal	I/O	Function	Type
1	WAKE_N	O	Open Drain Output Signal Wake Up signal to the host	3V3_AUX
20	W_DISABLE_N	I	Active Low Input Signal Shutdown Wireless disabling (Airplane mode)	3V3_AUX
22	PERST_N	I	Active Low Input Signal Shutdown	3V3_AUX
42	LED_WWAN_N	O	Open Drain Output Signal LED driving, for module's status indication	3V3_AUX

Table 17: Control Signal Operating Levels

Parameters	Min	Max
Input High Voltage	2.0	3V3_AUX
Input Low Voltage	-0.5V	0.8V
Output High Voltage	3V3_AUX -0.5V	3V3_AUX
Output Low Voltage	3V3_AUX -0.5V	3V3_AUX

7.5.1 W_DISABLE_N and PERST_N

W_DISABLE_N and PERST_N are both used to unconditionally shutdown the mPCIe. Whenever one of these signals is pulled low, the module shutdowns. After releasing both signals the module restarts. The module has already an internal Power On Reset control and do not need other external components.

Note: Do not use W_DISABLE_N and PERST_N to power cycle without first preparing the module to shutdown.

For more details refer to section 7.4.Power OFF Procedure

7.5.2 LED_WWAN_N

LED_WWAN_N is driven by the module according the PCI Express Mini Card Electromechanical Specification Revision 2.1. If desired, LED behavior can be configured by adjusting software settings [2][6]. The LED circuit driver is in an Open Drain configuration. LED can be directly connected to LED_WWAN_N through a PU series resistor to 3V3_AUX.

Note: This LED_WWAN_N signal is not active by default.

Refer to AT#SLED description in the AT Command User Guide [2][6].

7.6 Hardware Interfaces

The table below summarize all hardware interfaces available.

Table 18: Hardware Interfaces

Interface	ME910X1-mPCIe
USB	USB2.0
UART	HS-UART (up to 4 Mbps)
Audio I/F	I2S/PCM
USIM	Dual voltage (1.8V/2.85V)
Antenna ports	2 for Cellular, 1 for GNSS

7.6.1 USB Port

The ME910X1-mPCIe module includes a Universal Serial Bus (USB) transceiver, which operates at USB high-speed (480 Mbits/sec). It can also operate with USB full-speed hosts (12 Mbits/sec).

It is compliant with the USB 2.0 specification and can be used for control and data transfers as well as for diagnostic monitoring and firmware update.

The USB port is typically the main interface between the ME910X1-mPCIe module and OEM hardware.

The table below lists the USB interface signals:

Table 19: USB Interface

Signal	Pin No	Usage
USB_D-	36	Minus (-) line of the differential, bi-directional USB signal to/from the peripheral device
USB_D+	38	Plus (+) line of the differential, bi-directional USB signal to/from the peripheral device

Note: The USB_D+ and USB_D- signals have a clock rate of 480 MHz. Signal traces must be routed carefully. Minimize trace lengths, number of vias, and capacitive loading. The impedance value should be as close to 90 Ohms differential as possible and well isolated from other digital signals.

Note: Even if USB communication is not used, it is still highly recommended to place an optional USB connector on the application board. At least test points of the USB signals are required since the USB physical communication is needed in case of SW update.

7.6.2 Serial Port

The serial port is typically a secondary interface between the ME910X1-mPCIe module and OEM hardware.

Several configurations can be designed for the serial port on the OEM hardware.

The most common configurations are:

- RS232 PC com port
- Microcontroller UART

Depending on the serial port interfaces on the OEM hardware, you will need an extra components for voltage level translation. It is important to satisfy the condition in which during Shutdown, OFF or Power cycling, any external signals should be floating to avoid module's latchup and damage.

When mPCIe UART is directly connected to a PC an RS232 translator is necessary, see more details in 1.1.1.3 RS232 Level Translation.

The levels for the UART are CMOS 1.8V as described in 7.1 Logic Levels

List of the signal interconnections between RS232 and UART in the ME910X1-mPCIe:

Table 20: Modem Serial Port 1 Signals

RS232 Pin No.	Signal	mPCIe Pin No.	UART Function	Notes
2	RXD <-> UART_TX	5	Transmit Line	ME910X1-mPCIe UART Output transmit line
3	TXD <-> UART_RX	3	Receive Line	ME910X1-mPCIe UART Input receive line
5	GND	4,9,15....	Ground	Ground
7	RTS <-> UART_CTS	19	Request to Send	ME910X1-mPCIe UART Input controlling the Hardware flow control
8	CTS <-> UART_RTS	17	Clear to Send	ME910X1-mPCIe UART Output controlling the Hardware flow control

Note: To avoid a back-powering effect, it is recommended to prevent any High logic level signal from being applied to the digital pins of the module when it shutdowns, during OFF or Power Cycling.

Note: For minimum implementations, only the TXD and RXD lines need to be connected. The other lines can be left open if the host software allows it and is correctly set.

1.1.1.3. RS232 Level Translation

To interface the ME910X1-mPCIe UART with an RS232 PC COM Port, a voltage level translator is required. This level translator must:

- Invert the electrical signal in both directions
- Change the level from V_{IO} level to RS232 level: from 0/1.8V to +15/-15V.

The RS232 UART 16450, 16550, 16650 & 16750 chipsets accept signals with lower levels on the RS232 side (EIA/TIA-562), allowing a lower voltage-multiplying ratio on the level translator. Note that the negative signal voltage must be less than 0V and therefore some sort of level translation is always required.

The simplest way to translate the levels and invert the signal is by using a single chip-level translator. There are a multitude of them, differing in the number of drivers and receivers and in the levels (be sure to get a true RS232 level translator, not an RS485 or other standards).

By convention, the driver is the level translator from the UART V_{IO}, in our case V_{IO}=1.8V, to the RS232 level. The receiver is the translator from the RS232 levels to the V_{IO} levels of the UART.

To translate the whole set of control lines of the UART, the following is required:

- 1 driver
- 1 receiver

Note: The digital input lines operate at 1.8V CMOS.

Use a level voltage translator to properly interface with them.

RS232 Level Adaption Circuitry Example:

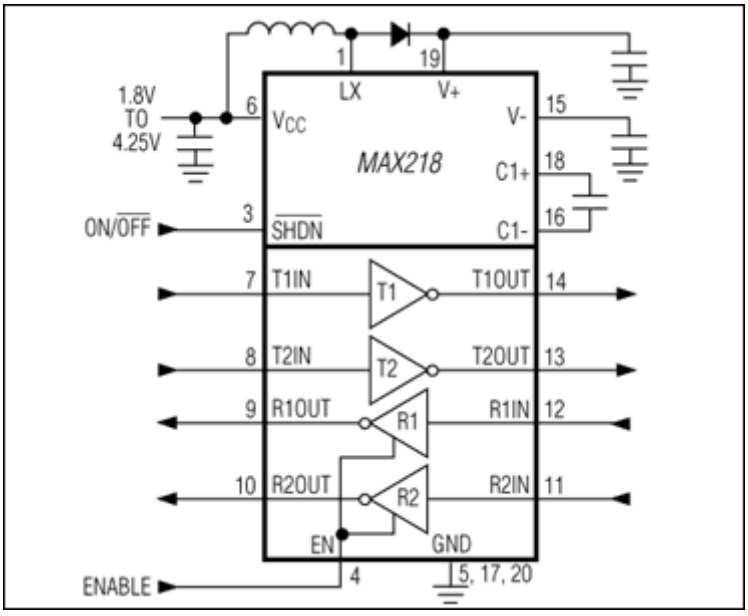


Figure 9: UART Level Adapter Example

Note: In case of high-speed access, higher than 1Mbps, the lines should be designed carefully to avoid signal degradation and noise generation.

The RS232 serial port lines are usually connected to a DB9 connector as shown in the figure below. Signal names and directions are named and defined from the DTE point of view. RS232 Serial Port Lines Connection Layout:

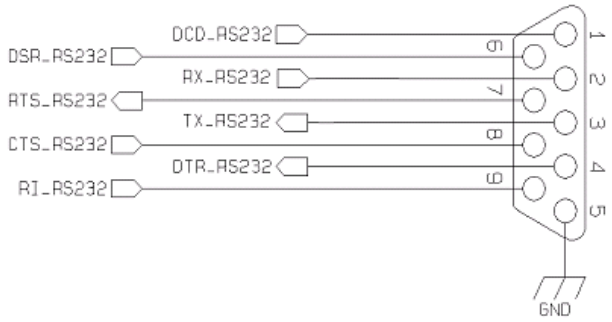


Figure 10: RS232 DB-9 pinout

7.7 SIM Interface

The SIM pins provide the connections necessary to interface to a SIM holder located at the host device. The Voltage levels over this interface comply with 3GPP standards.

The SIMIN line is not at the connector and is internally grounded.

Note: In this mPCIE variants, onboard SIM holders and eSIM are not mounted.

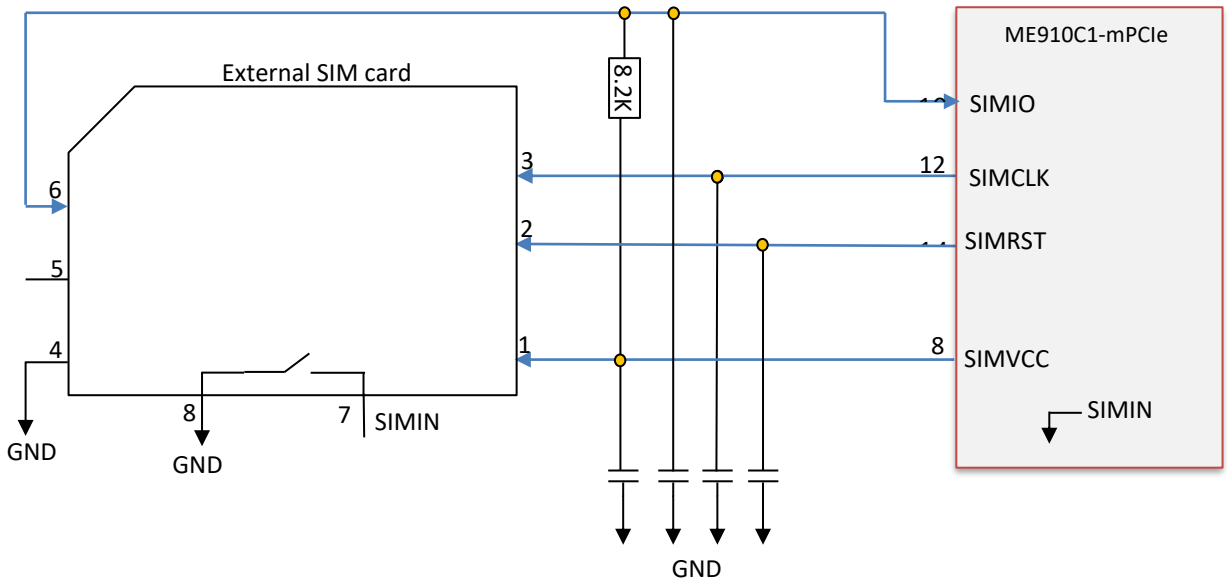


Figure 11: SIM Interface

Table 21: SIM Interface Signals

Pin	Signal	I/O	Function	Type
8	SIMVCC	O	External SIM signal – Power supply for the SIM	1.8 / 3V
10	SIMIO	I/O	External SIM signal – Data I/O	1.8 / 3V
12	SIMCLK	O	External SIM signal – Clock	1.8 / 3V
14	SIMRST	O	External SIM signal – Reset	1.8 / 3V

8 RF SECTION

8.1 Bands Variants

Please refer to the table provided in section 3.2 Product Variants and Frequency Bands.

8.2 TX and RX Characteristics

For more information, refer to the Module's Hardware User guide.

8.3 Antenna Requirements

8.3.1 Antenna Connectors

The ME910X1 Mini PCIe adapter is equipped with a set of 50 Ω RF U.FL. connectors from Hirose U.FL-R-SMT-1.

The available connectors are:

- Main RF antenna (ANT)
- GNSS Antenna (GPS)

See the picture on the right for their position on the interface.

The presence of all the connectors is depending on the product characteristics and supported functionalities.

For more information about mating connectors search for RF U.FL female cable up to 3GHz.

For example the U.FL-LP-xxx from Hirose

https://www.hirose.com/

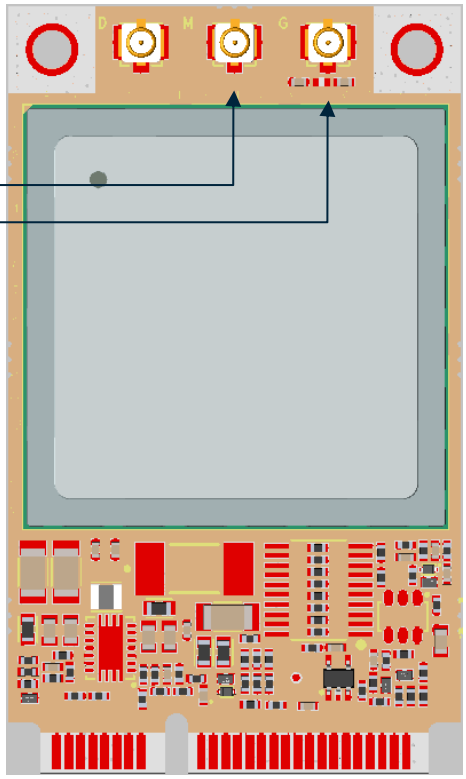


Figure 12 U.FL Antenna Connectors

The antenna connection is one of the most important aspects in the full product design as it strongly affects the product overall performances, so please read carefully and follow the requirements and the guidelines for a proper design.

The ME910X1-mPCIe adapter is provided with three RF connectors.

The available connectors are:

- Main RF antenna (ANT)
- GNSS Antenna (GPS)

Connecting cables between the module and the antenna must have 50 Ω impedance.

If the impedance of the module is mismatched, RF performance is reduced significantly.

If the host device is not designed to use the module's diversity or GPS antenna, terminate the interface with a 50Ω load.

8.3.2 Main GSM/LTE Antenna Requirements

The antenna for the ME910X1-mPCIe device must meet the following requirements:

Table 22: Main Antenna Requirements

Item	Value
Frequency range	The customer must use the most suitable antenna bandwidth for covering the frequency bands provided by the network operator while using the Telit module. The bands supported by each variant of the ME910X1 module family are provided in section 3.2 Product Variants and Frequency Bands.
Gain	Gain < 3 dBi
Impedance	50 Ohm
Input power	> 33 dBm(2 W) peak power in GSM > 24 dBm average power in WCDMA & LTE
VSWR absolute max	≤ 10:1 (limit to avoid permanent damage)
VSWR recommended	≤ 2:1 (limit to fulfill all regulatory requirements)

8.3.3 GNSS Antenna Requirements

ME910X1 mPCIe board does not supports an active antenna. If you want to use an active antenna, the bias circuit should be done externally.

In case of GNSS active antenna, It is recommended to follow:

- An external active antenna (17dB typ. Gain, GPS only)
- An external active antenna plus GNSS pre-filter (17dB typ. Gain)

Note: The external GNSS pre-filter is required for the GLONASS application.

The GNSS pre-filter must meet the following requirements:

Source and load impedance = 50 Ohm

- Insertion loss (1575.42–1576.42 MHz) = 1.4 dB (Max)
- Insertion loss (1565.42–1585.42 MHz) = 2.0 dB (Max)
- Insertion loss (1597.5515–1605.886 MHz) = 2.0 dB (Max)

Note: It is recommended to add a DC block to the customer's GPS application to prevent damage to the ME910X1-mPCIe module due to unwanted DC voltage

1.1.1.4. Combined GNSS Antenna

The use of a combined RF/GNSS antenna is NOT recommended. This solution can generate an extremely poor GNSS reception. Furthermore, the combination of antennas requires an additional diplexer, which adds significant power loss in the RF path.

1.1.1.5. Linear and Patch GNSS Antenna

Using this type of antenna introduces at least 3 dB of loss compared to a circularly polarized (CP) antenna. Having a spherical gain response instead of a hemispherical gain response can aggravate the multipath behavior and create poor position accuracy.

Note:	For detailed information about GPS operating modes and RF signal requirements, refer to the Module's Hardware User Guide.

9 Mechanical Design

9.1 Mechanical Dimensions

The ME910X1-mPCIe overall dimensions are:

- Length: 50.95 mm
- Width: 30 mm
- Thickness:
- **ME910G1-mPCIe:** 3.4 mm, +/-0.15mm (Version with SIM holder : 4.9 mm, +/-0.15mm)
- **ME910C1-mPCIe:** 3.2 mm, +/-0.15mm (Version with SIM holder : 4.7 mm, +/-0.15mm)
- Weight: 7 gm

9.2 Mechanical Drawing

9.2.1 Top View

The figure below shows the mechanical top view of the ME910X1-mPCIe, dimensions are in mm.

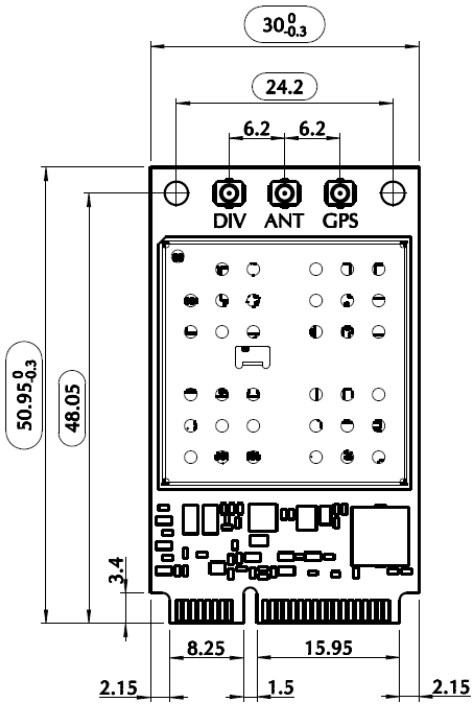


Figure 13 ME910X1-mPCIe Top View

9.2.2 Bottom View

The figure below shows mechanical top view of the ME910X1-mPCIe, dimensions are in mm.

The figure also depicts the eSIM and SIM holder, although by default they are not mounted.

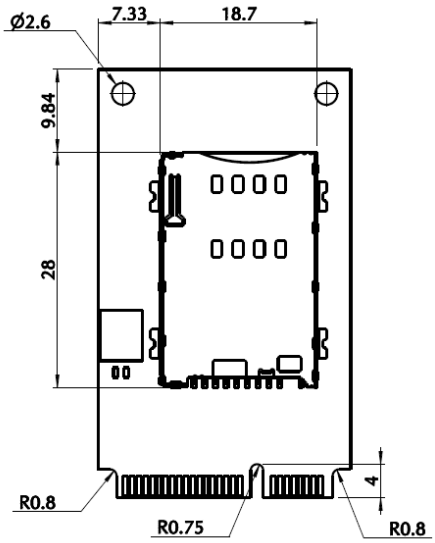


Figure 14: ME910X1-mPCIe Bottom View

9.2.3 Side View

The figures below show the two different mechanical side views of the ME910G1-mPCIe and ME910C1-mPCIe, dimension are in mm.

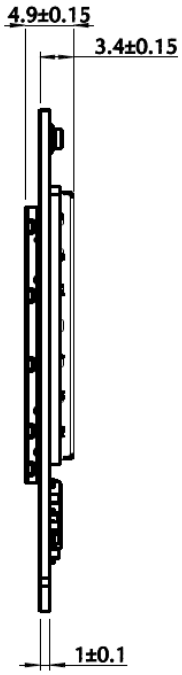


Figure 15: ME910G1-mPCIe Side View

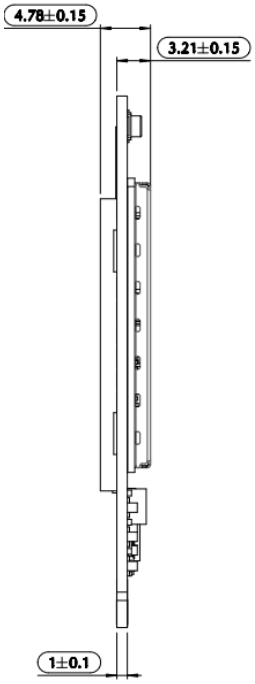


Figure 16: ME910C1-mPCIe Side View

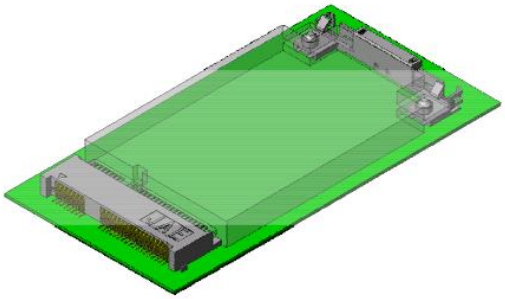
10 Application PCB Design

The ME910X1-mPCIe modules are designed to be compliant with a standard lead-free SMT process.

10.1 Recommended Footprint for the Application

ME910X1-mPCIe modules fits any full mPCIe 52 pin socket and latch connectors compliant with PCI Express Mini Card Electromechanical Specification Revision 2.1.

Given below is an example of board connector (MM60-52B1-E1-R650, JAE) and latch (MM60-EZH059-B5-R650, JAE) footprint for reference only:



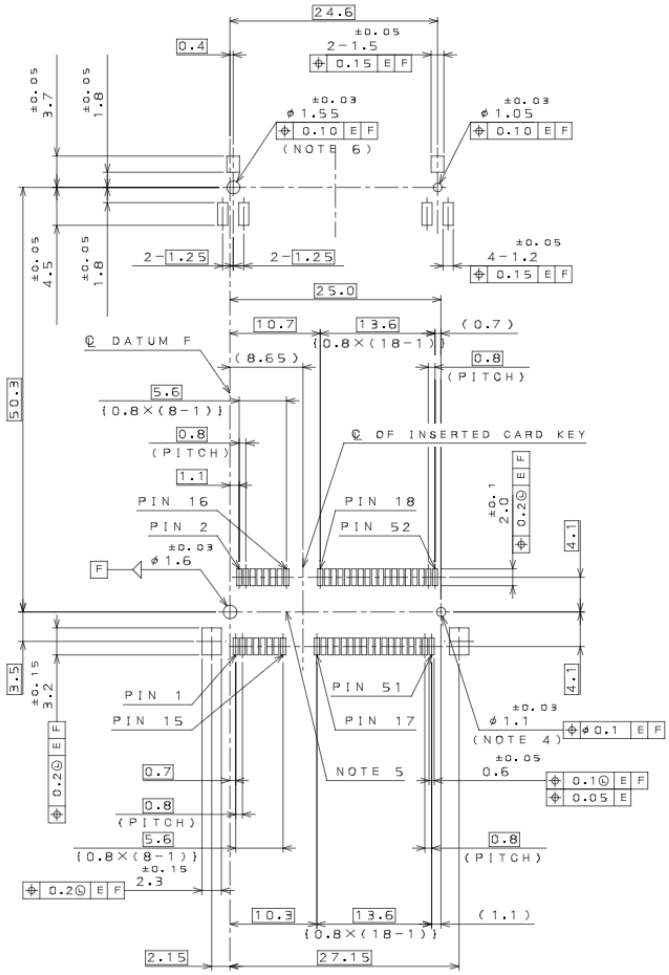


Figure 17: ME910X1-mPCIe Footprint Reference

11 EMC Recommendations

All ME910X1-mPCIe signals are provided with some EMC protection. However, the accepted level differs according to the specific pin.

Table 23: EMC Recommendations

Pad	Signal	I/O	Function	HBM	CDM
All Pins					
	All pins		All functions	2KV	500V
Antenna					
	Antenna connectors	Analog I/O	Antenna connectors	2KV	500V

Appropriate series resistors must be considered to protect the input lines from overvoltage.

12 Packing System

12.1 Tray

The ME910X1-mPCIe modules are packaged on trays of 20 pieces each:

Table 24: Tray Packing

Modules per Tray	Trays per Envelope	Modules per Envelope	Envelopes per Carton Box	Modules per Box
20	5 + 1 empty	100	5	500

Table 25: Packing Quantities

Order Type	Quantity
Minimum Order Quantity (MOQ)	20
Standard Packing Quantity (SPQ)	500

Tray organization is shown in the figure below.

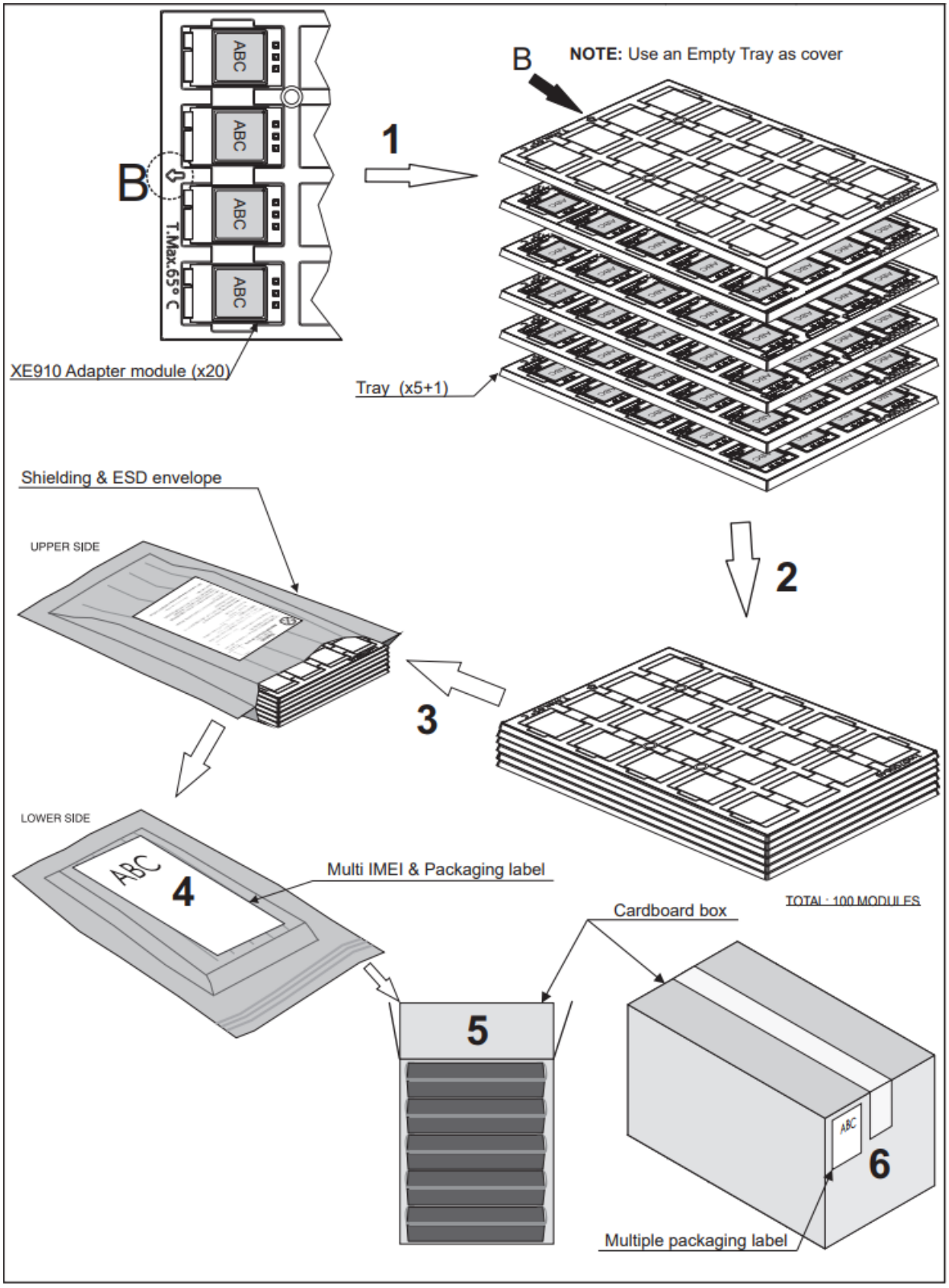


Figure 18: ME910X1-mPCIe Tray Organization

12.2 Tray Drawing

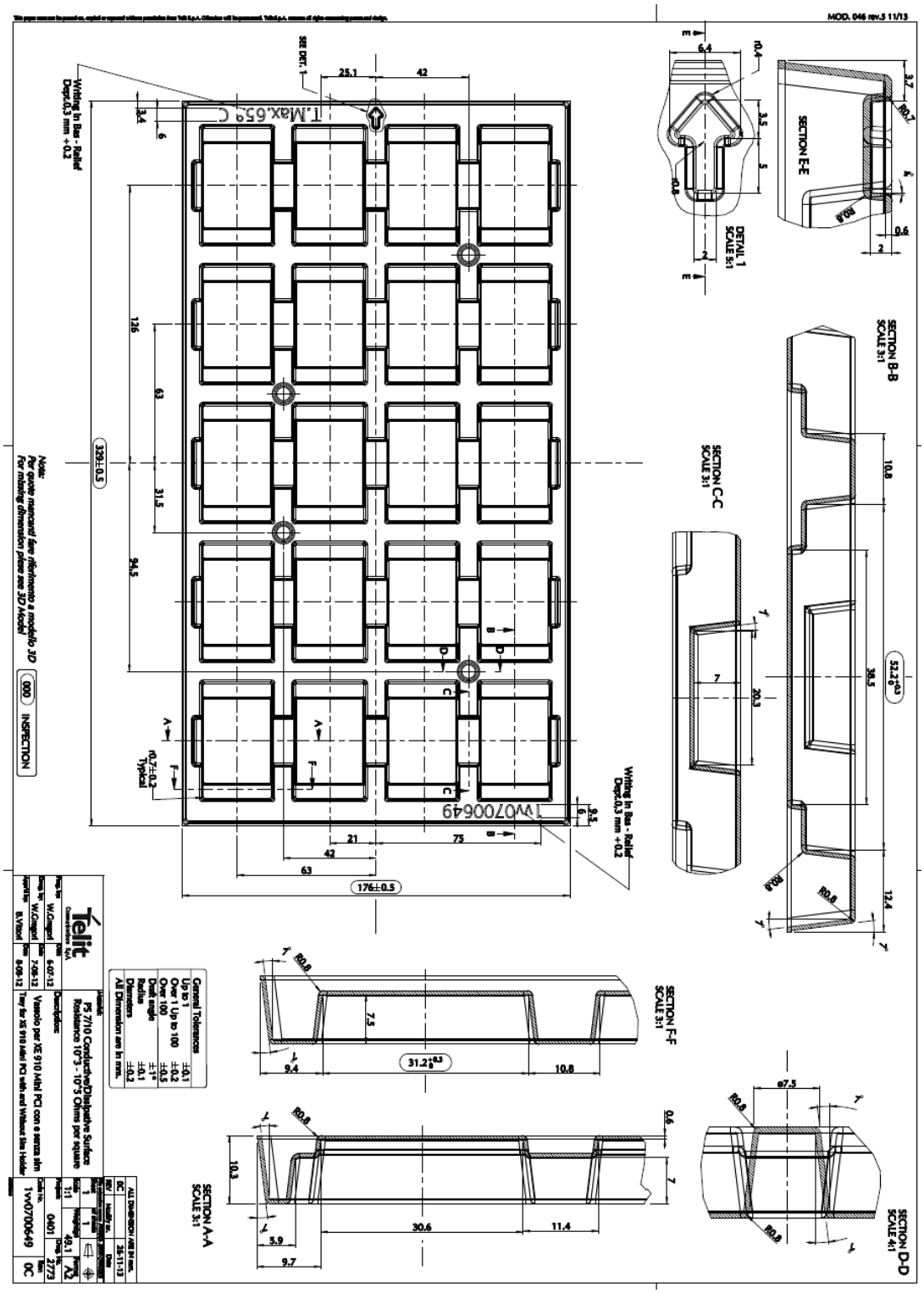


Figure 19: ME910X1-mPCIe Tray Drawing

Warning: These trays can withstand a maximum temperature of 65°C.

13 Conformity Assessment Issues

13.1 Declaration of Conformity

Hereby, Telit Communications S.p.A declares that the ME910C1-mPCIe is in compliance with Directive 2014/53/EU.

The full text of the EU declaration of conformity is available at the following internet address: https://www.telit.com/red

14 Reference Table of RF Bands Characteristics

Table 26: Reference Table of RF Bands

Mode	Freq. Tx (MHz)	Freq. Rx (MHz)	Channels	Tx-Rx Offset
PCS 1900	1850.2 ~ 1909.8	1930.2 ~ 1989.8	512 ~ 810	80 MHz
DCS 1800	1710 ~ 1785	1805 ~ 1880	512 ~ 885	95 MHz
GSM 850	824.2 ~ 848.8	869.2 ~ 893.8	128 ~ 251	45 MHz
EGSM 900	890 ~ 915	935 ~ 960	0 ~ 124	45 MHz
	880 ~ 890	925 ~ 935	975 ~ 1023	45 MHz
LTE 2100 – B1	1920 ~ 1980	2110 ~ 2170	Tx: 18000 ~ 18599 Rx: 0 ~ 599	190 MHz
LTE 1900 – B2	1850 ~ 1910	1930 ~ 1990	Tx: 18600 ~ 19199 Rx: 600 ~ 1199	80 MHz
LTE 1800 – B3	1710 ~ 1785	1805 ~ 1880	Tx: 19200 ~ 19949 Rx: 1200 ~ 1949	95 MHz
LTE AWS – B4	1710 ~ 1755	2110 ~ 2155	Tx: 19950 ~ 20399 Rx: 1950 ~ 2399	400 MHz
LTE 850 – B5	824 ~ 849	869 ~ 894	Tx: 20400 ~ 20649 Rx: 2400 ~ 2649	45 MHz
LTE 2600 – B7	2500 ~ 2570	2620 ~ 2690	Tx: 20750 ~ 21449 Rx: 2750 ~ 3449	120 MHz
LTE 900 – B8	880 ~ 915	925 ~ 960	Tx: 21450 ~ 21799 Rx: 3450 ~ 3799	45 MHz
LTE 1800 – B9	1749.9 ~ 1784.9	1844.9 ~ 1879.9	Tx: 21800 ~ 2149 Rx: 3800 ~ 4149	95 MHz
LTE AWS+ – B10	1710 ~ 1770	2110 ~ 2170	Tx: 22150 ~ 22749 Rx: 4150 ~ 4749	400 MHz
LTE 700a – B12	699 ~ 716	729 ~ 746	Tx: 23010 ~ 23179 Rx: 5010 ~ 5179	30 MHz
LTE 700c – B13	777 ~ 787	746 ~ 756	Tx: 23180 ~ 23279 Rx: 5180 ~ 5279	-31 MHz
LTE 700PS – B14	788 ~ 798	758 ~ 768	Tx: 23280 ~ 23379 Rx: 5280 ~ 5379	-30 MHz
LTE 700b – B17	704 ~ 716	734 ~ 746	Tx: 23730 ~ 23849 Rx: 5730 ~ 5849	30 MHz
LTE 800 – B19	830 ~ 845	875 ~ 890	Tx: 24000 ~ 24149 Rx: 6000 ~ 6149	45 MHz
LTE 800 – B20	832 ~ 862	791 ~ 821	Tx: 24150 ~ 24449 Rx: 6150 ~ 6449	-41 MHz
LTE 1500 – B21	1447.9 ~ 1462.9	1495.9 ~ 1510.9	Tx: 24450 ~ 24599 Rx: 6450 ~ 6599	48 MHz
LTE 1900+ – B25	1930 ~ 1995	1850 ~ 1915	Tx: 26040 ~ 26689 Rx: 8040 ~ 8689	80 MHz

Mode	Freq. Tx (MHz)	Freq. Rx (MHz)	Channels	Tx-Rx Offset
LTE 850+ – B26	814 ~ 849	859 ~ 894	Tx: 26690 ~ 27039 Rx: 8690 ~ 9039	45 MHz
LTE 700 – B28A	703 ~ 733	758 ~ 788	Tx: 27210 ~ 27510 Rx: 9210 ~ 9510	55 MHz
LTE 700 – B28	703 ~ 748	758 ~ 803	Tx: 27210 ~ 27659 Rx: 9210 ~ 9659	55 MHz
LTE AWS-3 – B66	1710 ~ 1780	2210 ~ 2200	Tx: 131972-132671 Rx: 66436-67335	400 MHz
LTE600 – B71	663 ~ 698	617 ~ 652	Tx: 133122-133471 Rx: 68568-68935	46 MHz
LTE TDD 2600 – B38	2570 ~ 2620	2570 ~ 2620	Tx: 37750 ~ 38250 Rx: 37750 ~ 38250	0 MHz
LTE TDD 1900 – B39	1880 ~ 1920	1880 ~ 1920	Tx: 38250 ~ 38650 Rx: 38250 ~ 38650	0 MHz
LTE TDD 2300 – B40	2300 ~ 2400	2300 ~ 2400	Tx: 38650 ~ 39650 Rx: 38650 ~ 39650	0 MHz
LTE TDD 2500 – B41M	2555 ~ 2655	2555 ~ 2655	Tx: 40265 ~ 41215 Rx: 40265 ~ 41215	0 MHz

15 Acronyms and Abbreviations

Table 27: Acronyms and Abbreviations

Acronym	Definition
CDM	ESD – Charged Device Model
CLK	Clock
CMOS	Complementary Metal – Oxide Semiconductor
DTE	Data Terminal Equipment
ESR	Equivalent Series Resistance
GPIO	General Purpose Input Output
HBM	ESD – Human Body Model
HS	High Speed
I/O	Input Output
mPCIe	Mini PCIe Adapter
PCB	Printed Circuit Board
RED	Radio Equipment Directive
RTC	Real Time Clock
SIM	Subscriber Identification Module
UART	Universal Asynchronous Receiver Transmitter
UMTS	Universal Mobile Telecommunication System
USB	Universal Serial Bus
VSWR	Voltage Standing Wave Radio
WCDMA	Wideband Code Division Multiple Access

16 Related Documents

For current documentation and downloads, refer to https://dz.telit.com/.

Table 28: Related Documents

S.no	Doc Code	Document Title
1	1VV0301351	ME910C1 Hardware User Guide
2	80529ST10815A	ME910C1 AT Command User Guide
3	1VV0301483	mPCIe_IFBD_HW_USER_GUIDE
4		PCI Express Mini Card Electromechanical Specification Revision 2.1
5	1VV0301593	ME910G1 Hardware User Guide
6	80617ST10991A	ME910G1 AT Command User Guide

17 Document History

Table 29: Document History

Revision	Date	Changes
5	2024-11-29	Remove section 11.3 – Moisture sensitivity
4	2022-07-27	Updated board thickness and dimension under section 2.7.1 Dimensions, 8.2.1 Top View, 8.2.2 Bottom View and 8.2.3 Side View
3	2022-05-18	Chapter6.3 and 6.4 using AT#SHDN for ME910G1
2	2022-01-14	Minor changes on the languagand updated to the new template Legal Notices updated
1	2020-02-11	Document revision
0	2019-12-17	First issue

From Mod.0818 Rev.15