WOLKITE UNIVERSITY

COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

Digital Logic Design (EENG2042) Final Examination

PART I: MULTIPLE CHOICES (25%) ***Put your answer only on space provided.***

1. A feature that distinguishes the ***J-k flip-flop from the S-R flip-flop*** is the:-

A) Preset input B) Type of clock signal C) Toggle condition D) Reset input

2. Which of the following is combinational circuit?

A) Flip-flop B) Counter C) Register D) None of the above

3. Which of the following gates has the exact ***inverse output of the OR gate*** for all possible input combinations? A) NOT B) X-NOR C) X-OR D) None of the above

4. On a Karnaugh map, grouping the **0's** produces

A) A sum-of-product expression C) AND-OR logic circuits

B) A "don't care" condition D) None of the above

5. The ***time interval required for input data to be present before the triggering edge of the clock pulse.*** A) Set-up time B) Hold time C) Propagation delay time D) None of the above

6. A ***group of flip-flops*** (memory device) that can be used to ***store more than one bit o***f information is: A) Register B) Encoder C) Latch D) Decoder

7. A combinational circuit which is used to change ***a decimal number into an equivalent BCD*** number is: A) Demultiplexer B) Multiplexer C) Encoder D) Decoder

8. How many ***select lines*** will a ***16 to 1 multiplexer*** will have: A) 5 B) 4 C)2 D) 1

9. In a ***4-variable K-map, a 3-variable product term*** is produced by:

A) an 8-cell group of 1s C) a 4-cell group of 0s

B) a 2-cell group of 1s D) a 4-cell group of 1s

10. A ***4-bit parallel adder*** can add:

A) Two 4-bit binary numbers C) Four bits in a sequence

B) Two 2-bit binary numbers D) Four bits at a time

11. A combinational circuit which is used to ***send data coming from a single source to multiple destinations*** is: A) Demultiplexer B) Multiplexer C) Encoder D) Decoder

12. ***How many different states*** does a ***3-bit asynchronous counter*** have? A)2 B)3 C)4 D)8

13. In a sequential logic circuit, what is the ***purpose of a clock signal***?

A) To synchronize the operation of flip-flops C) To control the input signals

B) To provide power to the circuit D) To generate the output

14. Which logic gate produces an output that is ***true*** only when all inputs are ***false***?

A) AND B) OR C) NAND D) NOR

15. Which of the following is combinational circuit?

A) Flip-flop B) Counter C) Register D) None of the above

16. What is the primary ***difference between a latch and a flip-flop***?

A) Latches are level-sensitive, while flip-flops are edge-triggered

B) Latches have multiple outputs, while flip-flops have only one output

C) Latches are asynchronous, while flip-flops are synchronous

D) There is no difference, they are synonyms

17. How many variables can a ***4-input Karnaugh map represent***? A) 2 B) 4 C) 8 D) 16

18. What is the main ***disadvantages of asynchronous sequential circuits***?

A) Higher power consumption C) Difficulty in analysis and design.

B) Propagation delay D) Limited scalability

19. The output of a ***JK flip-flop when both inputs are high*** is __.

A) 0 B) 1 C) Toggle D) No change

20. A flip-flop that ***changes state on the falling edge*** of the clock is called __.

A) Positive edge-triggered C) Level-triggered

B) Negative edge-triggered D) Bistable

21. In an ***asynchronous counter, the clock input of each flip-flop*** is connected to __.

A) The output of the previous flip-flop C) The enable signal

B) A common clock signal D) The input data signal

22. What logic function is the ***sum output of a half-adder***?

A) AND B) NAND C) Exclusive-NOR D) Exclusive-OR

23. The ***modulus*** of a counter refers to __.

A) The number of states in its cycle C) The clock frequency

B) The maximum count it can reach D) The number of flip-flops used

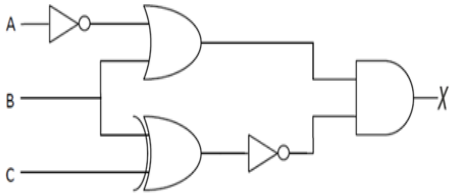
24. How many output lines does a ***3-to-8 decoder*** have? A) 2 B) 4 C) 8 D) 16

25. Which combinational circuits is used to convert ***BCD to seven-segment display*** format?

A) Adder B) Multiplexer C) Encoder D) Decoder

PART II: WORKOUTS (25%)

1. Consider the combinational circuit in the figure below. ***(3pts)***



A) Derive ***Boolean expressions*** for the output ***X*** as function of the inputs (A, B, and C) and simplify using ***only*** Boolean algebra techniques.

B) Find ***minimal POS*** expression using ***K-map*** simplification methods.

C) Draw the ***logic diagram of*** minimal ***POS*** expression.

2. A Boolean expression is mapped in the K-map shown below. ***(4pts)***

AB \ CD	00	01	11	10
00	1			1
01	1	1		1
11	1	1		1
10	1		1	1

A) Find the ***simplest Boolean expression (SOP)*** in terms of the variables A, B, C, and D

B) Draw the ***logic diagram*** for ***simplified SOP*** expressions using only ***NOR*** gates only.

3. ***Three sensors*** are attached to a ***printing device***, with ***three alarms*** attached to ***the sensors***. The ***1st sensor, "A",*** detects if the device needs ***ink.*** The ***2nd sensor, "B",*** detects if the device needs ***repair***. The ***3rd sensor, "C",*** detects if the device should ***jam (block paper***). Design a ***simplified logic circuit*** for which an ***alarm sounds if two or more problems occur***.

(3pts)

A	B	C	Alarm 1	Alarm 2	Alarm 3
0	0	0	0	0	0
0	0	1	1	1	0
0	1	0	1	0	1
0	1	1	1	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	1	1
1	1	1	1	1	1

4. What is ***a Demultiplexer***? ***Draw the logic circuit for a 1-to-4 Demultiplexer.*** ***(3pts)***

5. Design a combinational circuit that converts ***3-bit binary number*** A***, B, and C*** into its Gray-***code*** equivalent $\boldsymbol{X, Y, and\ Z}$.

   (3pts)

6. Draw a **truth table** and **logic diagram** for Positive edge triggered **J-K Flip-Flop**. ***(3pts)***

7. Implement the **X-NOR** logic expression using ***NAND gates only***: ***(2pts)***

8. What is the ***difference*** between: ***(2pts)***

   A) Demultiplexer and a decoder B) Combinational circuit and Sequential circuit

9. For S-R Flip-Flop waveforms shown below, ***draw the timing diagram*** showing the output ***Q and*** $\boldsymbol{\overline{Q}}$ you would expect to see if the flip-flop is initially ***RESET***. ***(2pts)***