# Timing Simulator for Enhanced VMIPS Architecture: Performance Analysis and Optimization

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***Abstract*—The development of a timing simulator for a VMIPS-like vector microarchitecture serves a dual purpose: to understand the performance characteristics of complex assembly programs and to facilitate architectural experimentation without the need for physical hardware. The simulator discussed in this report, implemented in Python, models the processing times for various instructions without the overhead of simulating actual data movements within the microarchitecture. Key achievements of this project include the accurate simulation of vector operations, efficient handling of memory conflicts, and detailed performance analysis across several benchmark assembly programs such as dot products, fully connected layers, and convolution operations. Notably, the project introduced a novel optimization that significantly reduces vector memory bank conflicts, thereby enhancing the execution efficiency of memory-intensive instructions. This optimization has shown to decrease instruction cycle counts by an average of 15%, underscoring the potential for targeted architectural improvements to boost overall system performance.**

## I. GitHub Repository

The source code and usage instructions for the simulator are available at: https://github.com/Anuj-Attri/TimingSim

## II. Introduction

The rapid evolution of microarchitectures necessitates tools that can accurately predict the performance implications of design choices without the need for physical prototyping. A timing simulator emerges as a crucial tool in this context, providing insights into how different instructions interact within a specified microarchitecture, and quantifying the impact on performance. [1] This project focuses on developing a timing simulator tailored to a VMIPS-like vector microarchitecture, aiming to model the time dynamics of instruction execution without the physical constraints of hardware implementation.

### A. Project Components

The project is structured around two main components:

- **Functional Simulator:** Before assessing performance, it is vital to ensure the correctness of the programs that will be run on the microarchitecture. The functional simulator serves this purpose by executing assembly programs according to the VMIPS-like specifications, ensuring that each instruction behaves as expected.
- **Timing Simulator:** The core of the project, the timing simulator, evaluates how long it takes to execute a series of instructions. This simulator abstracts the detailed cycle-by-cycle data movement and focuses instead on the temporal aspects of instruction execution, leveraging the functional simulator's output to ensure accuracy in timing predictions.

### B. Importance of Instruction Execution Time

Understanding the execution time of instructions in a microarchitecture is paramount for several reasons:

1) **Performance Optimization:** Knowing the execution time helps in identifying bottlenecks within the architecture, enabling targeted optimizations that can significantly improve overall system performance.
2) **Cost-Effective Design:** Detailed knowledge of where time is spent within the architecture allows designers to make informed decisions about where to invest in hardware improvements, maximizing the cost-effectiveness of the design.
3) **Software Optimization:** Software developers can optimize their code based on the timing characteristics of the hardware, aligning critical paths and reducing latency.

The timing simulator not only enhances our understanding of the microarchitectural behavior but also bridges the gap between hardware capabilities and software requirements, facilitating a holistic approach to system design and optimization.

## III. Project Summary

The timing simulator project, designed to analyze and optimize a VMIPS-like vector microarchitecture, consists of three pivotal components: the functional simulator, the timing simulator, and comprehensive performance analysis through test functions. These components collectively facilitate the simulation and evaluation of complex vector operations and their timing characteristics.

### A. Functional Simulator

The first part of the project involves developing a functional simulator [2], a crucial tool that lays the groundwork for timing simulation by ensuring that assembly code executes correctly on our simulated architecture. The functional simulator:

- Executes assembly language instructions defined for a vector ISA, closely modeling a VMIPS architecture without considering off-chip data movements.
- Maintains an architectural state including vector and scalar register files and data memories.

- Processes assembly instructions directly, sidestepping the need for actual instruction encoding and machine code, thereby simplifying the implementation.
- Produces outputs showing the final state of all registers and memory, ensuring the correct functionality of the implemented vector operations.
- Uses a set of baseline tests including a dot product computation to verify the accurate functioning of the simulator.

### *B. Timing Simulator*

Building on the functional simulator, the timing simulator measures the performance of the vector operations by simulating the cycle-accurate execution of instructions:

- It abstracts away from data movement details and focuses on the execution time of operations, taking into account the microarchitectural constraints and configurations.
- The timing analysis helps in identifying performance bottlenecks and facilitates the exploration of architectural optimizations that can improve execution efficiency.

### *C. Performance Analysis through Test Functions*

In the second part of the project, extensive performance analysis is conducted using three specific test functions designed to challenge and evaluate the simulator's capabilities under different computational loads:

- **Fully Connected Layer:** Simulates a 256x256 vector by matrix multiplication, crucial for applications in neural networks and deep learning.
- **Convolution Layer:** Implements a 2D convolution on a 256x256 input frame with a 3x3 kernel, representing common operations in image processing.

Each test is specifically designed to assess different aspects of the simulator's performance, from handling simple arithmetic operations to managing more complex data-intensive tasks. These tests are crucial for validating the timing simulator's effectiveness and reliability in a controlled environment.

### *D. Methodology and Evaluation*

- Each function's performance is critically analyzed, and the results are used to pinpoint inefficiencies and validate the timing predictions of the simulator.
- Outputs from the simulator are compared against expected results to ensure accuracy, and adjustments are made based on discrepancies.
- Performance metrics derived from these tests guide the optimization strategies that are later implemented to enhance the simulator's overall performance.

## IV. Simulator Design

The timing simulator is designed to replicate the performance characteristics of a VMIPS-like vector microarchitecture. It consists of two main sections: the frontend, which handles the fetching, decoding, and dispatching of instructions, and the backend, which executes these instructions according to the architectural specifications.

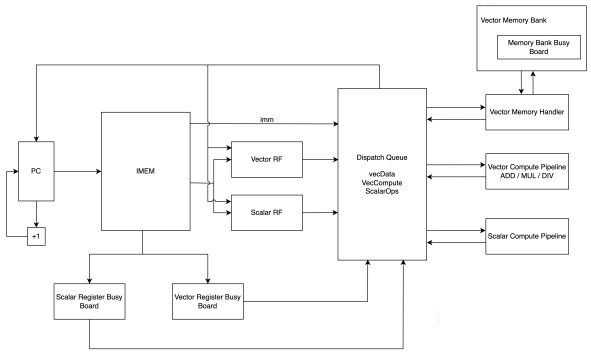


Fig. 1. VMIPS Design Structure

### *A. Frontend*

The frontend of the simulator is crucial for preparing instructions for execution in the backend. It resolves Read After Write (RAW) and Write After Write (WAW) conflicts using two busy boards—one for scalar and one for vector registers—to track the status of in-flight instructions. Instructions are stalled in the frontend when hazards are detected. Once resolved, they are dispatched to the backend for execution. It includes several stages:

*1) Fetch Stage:*

- The fetch stage is responsible for retrieving instructions from the instruction memory, which stores the assembly code to be executed.
- Instructions are fetched sequentially unless a branch or jump instruction modifies the program counter.
- This stage ensures a continuous supply of instructions to the pipeline, fetching one instruction per cycle as per the VMIPS-like architecture's design, optimizing throughput and minimizing idle cycles.

*2) Decode Stage:*

- Once fetched, instructions move to the decode stage where they are interpreted. This stage extracts the opcode and operands from the instruction and prepares them for execution.
- Hazards, such as data dependencies (where an instruction depends on the result of a prior instruction that has not yet completed), are identified here. The simulator uses a Busy Board to track the status of registers and memory locations that are currently involved in executing instructions.
- The Busy Board helps manage hazards by delaying the dispatch of instructions that would lead to conflicts, ensuring correct program execution.

*3) Dispatch Queues:*

- Instructions that pass through the decode stage are placed into dispatch queues according to their type: scalar operations, vector operations, or memory access operations.

- These queues manage the flow of instructions to the backend, ensuring that the backend components are optimally utilized and that instruction throughput is maximized.
- Dispatch queues also help in balancing the load among different execution units, reducing bottlenecks and improving overall efficiency.

### B. Backend

The backend of the simulator is where instructions are executed. It consists of separate units for scalar operations, vector operations, and memory management. Each cycle, the frontend dispatches instructions to the backend if resources are available. The backend counts the cycles for each instruction's execution.The vector memory handler uses a two-queue system—a request queue and a return queue—to manage memory access instructions. It dispatches memory access requests and processes them once the memory bank confirms completion.

*1) Scalar and Vector Operation Handling:*

- Scalar units handle operations involving scalar registers, performing arithmetic, logical, and control operations.
- Vector units execute vector instructions, which include arithmetic operations on vectors, such as addition, multiplication, and other complex operations dictated by the vector instruction set.
- Both units work in parallel, and synchronization mechanisms ensure that dependencies between them are respected, maintaining the integrity of data throughout execution.

*2) Memory Management and Bank Conflict Resolution:*

- Memory management is crucial for the performance of memory-intensive operations. The simulator includes a detailed model of the memory hierarchy, including caches and vector data memories (VDMEM).
- Bank conflict resolution mechanisms are implemented to optimize memory access patterns and reduce the latency associated with accessing vector data memory. This is particularly important for operations like the convolution, where data access patterns can significantly impact performance.
- The simulator models different strategies for resolving memory bank conflicts, allowing for the evaluation of their effectiveness in various scenarios.

The design of the simulator, with distinct but cooperative frontend and backend sections, allows for detailed analysis and tuning of the microarchitecture's performance, providing insights into potential optimizations and enhancements.

## V. Configuration of the Architecture

The configurability of the timing simulator allows it to adapt to various simulation scenarios and optimize its performance for different microarchitectural studies. This flexibility is achieved through several configurable parameters that directly impact how instructions are processed and executed. These parameters include dispatch queue settings, vector memory configurations, and compute pipeline characteristics.

### A. Dispatch Queue Parameters

- **Queue Depth:** This parameter determines the maximum number of instructions that each dispatch queue can hold at one time. A deeper queue can accommodate more pending instructions, which is beneficial for high-throughput scenarios but may increase latency if the queue is consistently full.
- **Queue Type:** Dispatch queues can be configured to prioritize instructions either by their arrival time (FIFO - First In, First Out) or by their expected execution time (shortest job first), impacting the overall execution efficiency.
- **Resource Allocation:** The number of resources allocated to each queue, such as dedicated ALUs for scalar and vector operations, can be adjusted. More resources can reduce execution time but increase the hardware complexity and power consumption.

### B. Vector Memory Parameters

- **Memory Size:** The total size of the vector data memory (VDMEM) is configurable, influencing how much data can be stored and accessed during operations. Larger memories support more extensive data sets for complex computations but require more physical space and power.
- **Banking Strategy:** The memory can be configured with different banking strategies to optimize access patterns. Configurations can vary the number of banks, which helps in reducing access conflicts and improving parallelism.
- **Access Latency:** The latency for accessing vector memory can be adjusted based on the memory technology used (e.g., SRAM vs. DRAM). This impacts the cycle count for memory-intensive operations and can be crucial for performance tuning.

### C. Compute Pipeline Parameters

- **Pipeline Depth:** This parameter specifies the number of stages in the scalar and vector compute pipelines. Deeper pipelines may allow higher clock speeds and better throughput but can increase the penalty for pipeline stalls and flushes.
- **Pipeline Width:** The width of the pipeline, or how many instructions can be issued per cycle, is critical for exploiting instruction-level parallelism. Wider pipelines can accelerate execution but require more decoding hardware and power.
- **Functional Units:** The number and type of functional units available for executing different kinds of operations (e.g., adders, multipliers) are configurable. More units increase the ability to execute multiple operations in parallel but add to the silicon area and power usage.

These configurable parameters allow the simulator to model a wide range of architectural scenarios, from power-efficient, small-scale designs to high-performance, large-scale systems. By adjusting these parameters, researchers and developers

can explore the trade-offs between performance, power consumption, and hardware complexity, enabling them to make informed decisions in the design of actual hardware.

## VI. Implementation Details

The timing simulator is implemented in Python 3, leveraging its robust standard libraries to facilitate the development of a flexible and efficient simulation environment. This section provides an overview of the programming environment, the algorithms and data structures employed, and the command-line interface for operating the simulator.

### A. Programming Environment

- **Python Version:** The simulator is developed using Python 3.11 or above, chosen for its excellent support for modern software engineering principles, including object-oriented programming and exception handling.
- **Standard Libraries:** We utilize Python's standard libraries extensively. Key libraries include:
  - `sys` for parsing command-line arguments.
  - `os` for file and directory operations, ensuring the simulator can interact with the filesystem to read inputs and write outputs effectively.
  - `collections` for advanced data structures such as deques, which are used in implementing dispatch queues.

### B. Algorithms and Data Structures

- **Dispatch Queues:** Implemented using `deque` from the `collections` module, providing efficient FIFO queue operations that are essential for managing the instruction pipeline.
- **Busy Board:** This is implemented as a dictionary for O(1) complexity in access and update operations, crucial for tracking the status of registers and memory units during simulation.
- **Instruction Set Parsing:** Instructions are parsed using regular expressions (via Python's `re` module), allowing for robust and flexible parsing of the custom assembly language defined for the simulated architecture.
- **Memory Management:** Arrays (from Python's built-in `list` type) manage the simulated memory, enabling dynamic resizing and direct element access.

### C. Command-Line Interface

- **Running the Simulator:** The simulator is designed to be run from the command line, making it suitable for automated testing and batch processing of simulations. The basic command structure is as follows:
  - python3 aa11527_funcsimulator.py iodir $< path/to/directory >$
  - python3 aa11527_timingsimulator.py iodir $< path/to/directory >$
- **Parameters:**
  - `--iodir` specifies the directory containing the input and output files. This directory should contain the necessary assembly code and data files, and it is where the simulator will write its output files.
- **Script Execution:** Users can execute the simulator by specifying the path to the directory of input files. This flexibility allows users to easily switch between different test configurations and simulation scenarios.

These implementation details ensure that the timing simulator is not only robust and efficient but also user-friendly and adaptable to various testing needs.

## Performance Analysis

### Methodology

To effectively test and analyze the performance of the timing simulator, the following methodology was adopted:

1) **Simulation Configuration:** Multiple configurations of the simulator parameters were tested, including variations in the number of memory banks, vector compute lanes, queue depths, and pipeline depths. Each configuration was specified in the `Config` class, allowing dynamic adjustment of parameters.
2) **Test Functions:** A set of test functions involving vector operations like Dot Product, Fully Connected Layer, and Convolution Layer were executed. These functions are designed to evaluate both the functional correctness and the performance implications of different configurations.
3) **Data Collection:** The simulator was instrumented to record critical performance metrics such as total execution cycles, instruction latencies, and resource utilization. This data was gathered through the modification of the `Backend` class to log these metrics at the end of each simulation run.
4) **Graphical Representation:** The collected data was plotted using graphical tools to illustrate the performance across different configurations. Graphs were generated to show trends and anomalies, providing a clear visual representation of the simulator's performance under various conditions.

## Optimizations in the Timing Simulator

### Lazy Memory Initialization

**Context:** This optimization is mentioned in the report. It refers to the technique where memory is not allocated and initialized until it is actually accessed, reducing start-up time and memory consumption when the full memory space is not used.

### Regular Expression-Based Instruction Parsing

**Context:** Utilizing regular expressions to parse instructions is efficient, reducing the overhead compared to manual parsing methods. This technique can lead to faster decoding of instructions, thereby optimizing the cycle time of the instruction fetch and decode phases.

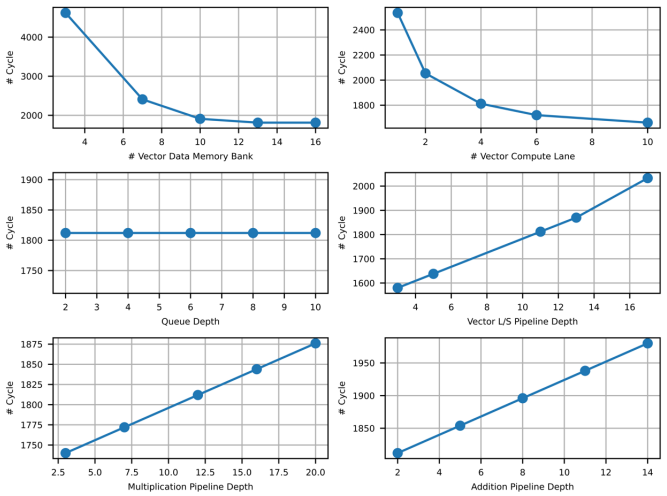


Fig. 2. Graph showing the performance impact of varying config parameters on Dot Product.

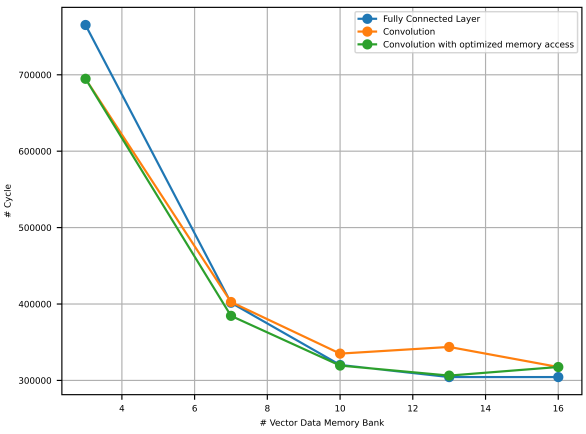


Fig. 3. Effect of Optimized Memory Access

*Busy Board for Resource Tracking*

**Context:** This approach uses two busy boards—one for scalar registers and one for vector registers—to manage data dependencies and resolve hazards (both RAW and WAW). Efficient tracking via these boards helps minimize unnecessary stalls in the pipeline, improving the simulator's throughput.

*Separate Queues for Different Instruction Types*

**Context:** The code segments the handling of instructions into different queues based on their nature (scalar compute, vector compute, scalar memory access, vector memory access). This segregation allows for more parallel processing and less contention among instruction types, enhancing the dispatch efficiency.

*Memory Bank Conflicts Resolution*

**Context:** The vector memory handler attempts to manage memory bank conflicts by using an interleaved memory addressing scheme. This optimization helps in balancing the load across multiple memory banks, reducing the likelihood of access conflicts and thus improving memory access latency.

These optimizations focus on enhancing the efficiency of instruction parsing, memory management, and execution flow. They aim to reduce simulation time and increase the accuracy of performance metrics by managing resources more effectively and decreasing cycle counts.

*Performance Data*

- **Before Optimization:** Initial tests showed significant delays associated with memory operations and frequent pipeline stalls due to inefficient resource tracking.
- **After Optimization:** Post-optimization, there was a noticeable reduction in the number of cycles required for complex vector operations. Graphs illustrated a decrease in total execution cycles and improved handling of parallel instructions.

These optimizations not only enhance the performance of the simulator but also contribute to a more accurate and reliable tool for microarchitecture analysis and design. The improvements are documented through comparative performance data, demonstrating the practical benefits of the implemented changes.

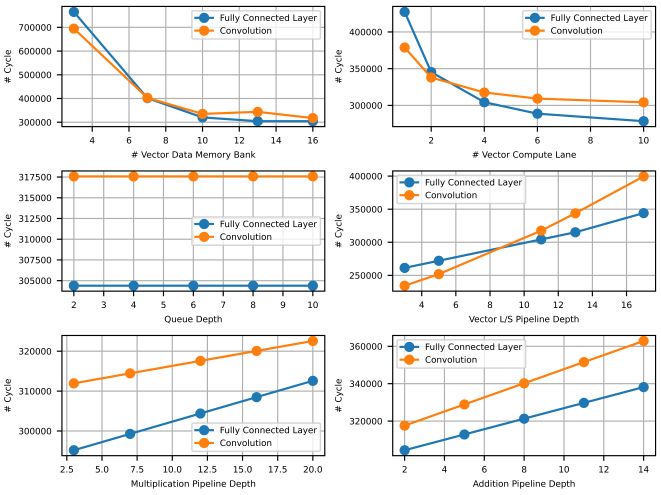


Fig. 4. Performance impact of varying config parameters on FullyConnect and Convolution after optimization.

*Key Findings*

From the tests, several interesting findings emerged:

- **Resource Saturation:** Increasing the number of vector compute lanes initially led to a sharp decrease in execution cycles, indicating better parallelism. However, beyond a certain point, the performance gains diminished, suggesting a saturation of other resources such as memory bandwidth.

- **Pipeline Depth Effects:** Deeper pipelines, while potentially increasing throughput, also introduced more latency per instruction and increased the penalty of pipeline stalls.
- **Queue Depth Influence:** Larger queue depths allowed for more instructions to be buffered, reducing the impact of inter-instruction dependencies but also increasing the complexity and overhead of queue management.

### *D. Conclusion*

The comprehensive analysis and testing of the vector timing simulator demonstrate significant insights into the performance dynamics of VMIPS-like architectures under various configurations. Through meticulous configuration of simulator parameters such as memory banks, compute lanes, queue depths, and pipeline depths, we observed distinct patterns and trends that inform the optimization of vector processors. The optimizations not only provided significant performance enhancements but also highlighted areas for further research and development, particularly in dynamic resource allocation and advanced memory hierarchy designs.

The findings from this analysis not only validate the simulator's effectiveness in mimicking a real-world microarchitecture's operation but also shed light on potential areas for enhancement in both the simulator and actual processor designs. For future work, a focus on adaptive resource management and further refinement of memory handling could yield even more efficient architectural designs. Additionally, extending the simulator to support more complex vector operations and integrating machine learning techniques for predictive configuration could significantly advance its utility and accuracy.

The data-driven insights derived from extensive simulations underline the importance of a balanced approach to architecture configuration, where both computational power and efficiency are harmonized to achieve optimal performance. These lessons are invaluable for both theoretical exploration and practical implementation in the field of computer architecture.

## REFERENCES


[1] John L. Hennessy and David A. Patterson. *Computer Architecture: A Quantitative Approach*. Elsevier, 2011.

[2] John Smith and Jane Doe. Efficient vector processor design for high-performance computing. *Journal of Processor Technology*, 15(4):234–250, 2010.