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MicroProcessor: General Purpose Processor contains no RAM, no RoM & no I/o ports & can't operate without adding them to it externally

Micro-controller: A single specific purpose chip contains CPU, Fixed amount of RAM, RoM & I/o ports used to control embedded systems

Embedded systems: systems (electrical or electroMechanical devices) controlled by special purpose computer encapsulated inside it

MechaTronic systems: systems in which Mechanical hardware are integrated with information-driven systems (Micro-controllers)

n-bit Processor: 1-) Processor work only on n-bit of data at a time

2-) Data larger than n-bit has to be broken into n-bit pieces to be Processed

Micro-Processor :

→ We need To connect Peripheral externally so it makes circuit large

→ Due To The external component The Total Power consumption is high So it's not ideal For The devices running on Stored Power like batteries

→ MoST of MP don't have Power saving Feature

→ based on The von-neumann model where program & data are stored in The same memory Module

→ MP-based system can run at a very high speed because of The Technology involved

→ it's useful For general purpose Application That allow you To handle loads of data

→ Watch dog Timer don't exist in MPU system

OSCAR
→ MP is a core of computer system

Micro - controller

→ The Peripherals such as RAM, RoM, I/o & Timers are Built in So it's available in one single chip

→ as external component are low Total Power consumption is less so it can be used With devices running on Stored Power like batteries

→ MoST of Mc offer Power saving Mode

→ based on harvard architecture where Program & data are stored in separate memory Module

→ Mc Based system run-up To 200 MHz or more depending on The architecture

→ it's useful For Application Specific system

→ MCU have WDT To ensure That The Program is executed correctly

→ Mc embedded inside some other devices

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→ Von-neumann: → Single common memory spaces where program instruction & data are stored

↳ There is a single data bus fetches both instruction & data

→ Harvard: → separate memory area for instruction & another are for data

↳ one bus connects the CPU to the RAM & another connect the CPU to ROM

PRoM: Programed RoM

↳ can be Programed

↳ For every bit There is a Fuse

↳ Programed by blowing The Fuse

↳ Programed only burned 1 Time

↳ MasKed RoM: NoT user Programed RoM

↳ are Programed by IC Manufacture

↳ OTP one Time programes

Like BioS – BooTloader

↳ EPRoM Erasable Programed RoM

↳ We can Program & erase Much Time

↳ Need burner To but your code

↳ IT canbe eqrsed while it in The System board

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RaM → RanJoM access MeMory ⟶ Based on MosFeT

↳ Read WriTe memory

↳ VolaTile MeMory

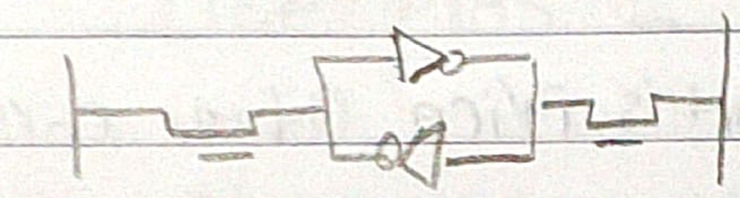
↳ DaTa access MeMory is very FaST

① SRAM. STaTic RandoM access MeMory

↳ تتكون من 6 ترانزستور

↳ Form FroM BiT liNe TRue & BiT liNe complement

↳ 2 iNVerse & Feedback on each oTher



↳ cell are Made of FliPFloP & TheVeFore don'T Require refreshing in order To keeP TheiR DaTa

↳ iT'S AdVanTage: ⟶ SRAM PerForMance beTTer Than dRaM iN Spe

↳ iT used To creaTe speed sensiTive cache

↳ iT has MediuM PoWer consuMPTion

↳ iT'S diSAdVanTages: → expensive coMPare To DRAM

↳ has coMPleX desi'gn

↳ PrOPleM of FliP FloP each BiT requiVe aT leaST 6 TRansiSTor

↳ loW capaciTy Than DraM

↳ When PoWer lOST daTa lOST

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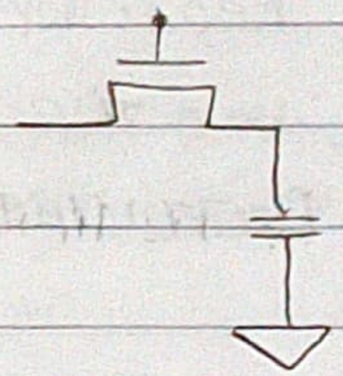
→ DRAM. Dynamic Random access memory

↳ consist of 1 capacitor & 1 transistor

↳ Is volatile

↳ Fast compare to Flash



→ There small leakage path from the drain into the substrate when the gate is off

↳ Through the reverse current junction here the capacitor will discharge

↳ ① it's lower than SRAM is price Power consumption

② using capacitor to store Data cut down the number of transistor to Build the cell

③ capacitor is require constant refreshing due to charge leakage

④ While refreshing the Data can't be accessed

Why RoM is Read only Memory although i can write on it ?

↳ It's Refered To as RoM since in The normal operation, The CPU doesn't have

The capability To write To it

↳ it may be written To by an external device or They may be a special configuration

within The system wherein The CPU is granted access To write To it

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Type	Volatile	Rewriteable	Erase size	Max erase cycle	Cost per Byte	Speed
SRAM	yes	yes	Byte	unlimited	expensive	Fast
DRAM	yes	yes	Byte	unlimited	Moderate	Moderate
Masked ROM	No	No	—	—	Inexpensive	Fast
PROM	No	once	—	—	Moderate	Fast
EPROM	No	yes	Entire	limited	Moderate	Fast
EEPROM	No	yes	Byte	limited	expensive	Fast / slow
Flash	No	yes	Sector	limited	Moderate	Fast / slow
NVRAM	No	yes	Byte	unlimited	expensive	Fast