

CPEEEE64

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Lab Six: Special Projects

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Abstract

Two input logic gates are synthesized for the Altera Cyclone IV FPGA using the Quartus IDE. The logic gates are verified using a System Verilog testbench and Mentor's Modelsim HDL simulator

CONTENTS

I	Introduction	1
II	Lab Procedure	1
III	Lab Report	1
IV	Conclusion	1

LIST OF FIGURES

I. INTRODUCTION

THIS Lab allows the student to exercise some design liberty. A number of example projects will be provided but you are free to choose something of your own. The student could implement a communication protocol to one of the on board devices.

II. LAB PROCEDURE

III. LAB REPORT

IV. CONCLUSION