Lab Four: Shift registers, Counters

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***Abstract*—Two input logic gates are synthesized for the Altera Cyclone IV FPGA using the Quartus IDE. The logic gates are verified using a System Verilog testbench and Mentor's Modelsim HDL simulator**

I. Introduction

THIS lab will reinforce the idea of modularity as we design modules which depend on a clock. Clocking circuits allows the synchronization of large blocks of logic.

A. What a Register really is

B. Posedge and Negedge in the sensitivity list

C. Blocking and non blocking operators

II. Lab Procedure

THIS lab focuses on applications of the shift register. It can be found in a number of uses like the serialization and de-serialization of data streams. A common trick to expand IO on a device is to use the venerable HC595 shift register. The data for the output pins can be output serially to the shift register instead of directly parallel. This trades update speed and code complexity for IO pin usage. Let's take some indicator LED's for example. They do not need to be updated frequently and we can save the complex IO pins on the FPGA for other purposes.

A. Timers

1) LED Brightness modulation:

B. Shift Registers

1) Interaction with External Shift register:

III. **Lab Report**

IV. **Conclusion**