Lab Six: Special Projects

Ben Smith

***Abstract*—Two input logic gates are synthesized for the Altera Cyclone IV FPGA using the Quartus IDE. The logic gates are verified using a System Verilog testbench and Mentor's Modelsim HDL simulator**

I. Introduction

THIS Lab allows the student to exercise some design liberty. A number of example projects will be provided but you are free to choose something of your own. The student could implement a communication protocol to one of the on board devices like the accelerometer.

II. Lab Procedure

A. Using the on board ADC

B. Using the on board Accelerometer

C. Implement a Bit coin miner

III. Lab Report

IV. Conclusion