Lab Four: Shift registers, Counters

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***Abstract*—Two input logic gates are synthesized for the Altera Cyclone IV FPGA using the Quartus IDE. The logic gates are verified using a System Verilog testbench and Mentor's Modelsim HDL simulator**

I. Introduction

THIS lab will reinforce the idea of modularity as we design modules which depend on a clock. Clocking circuits allows the synchronization of large blocks of logic.

A. What a Register really is

B. Posedge and Negedge in the sensitivity list

C. Blocking and non blocking operators

II. Lab Procedure

A. Shift register

B. SPI Bus communication

III. Lab Report

IV. Conclusion