CPEEEE64

DECEMBER 23, 2013

Lab Four: Sequential Logic

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Abstract

Two input logic gates are synthesized for the Altera Cyclone IV FPGA using the Quartus IDE. The logic gates are verified using a System Verilog testbench and Mentor's Modelsim HDL simulator

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DERP

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References

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[2] W. Foundation. (2013) Verilog. [Online]. Available: https://en.wikipedia.org/wiki/Verilog