CSU22022 Computer Architecture

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Project A - Register-file

4th October 2021

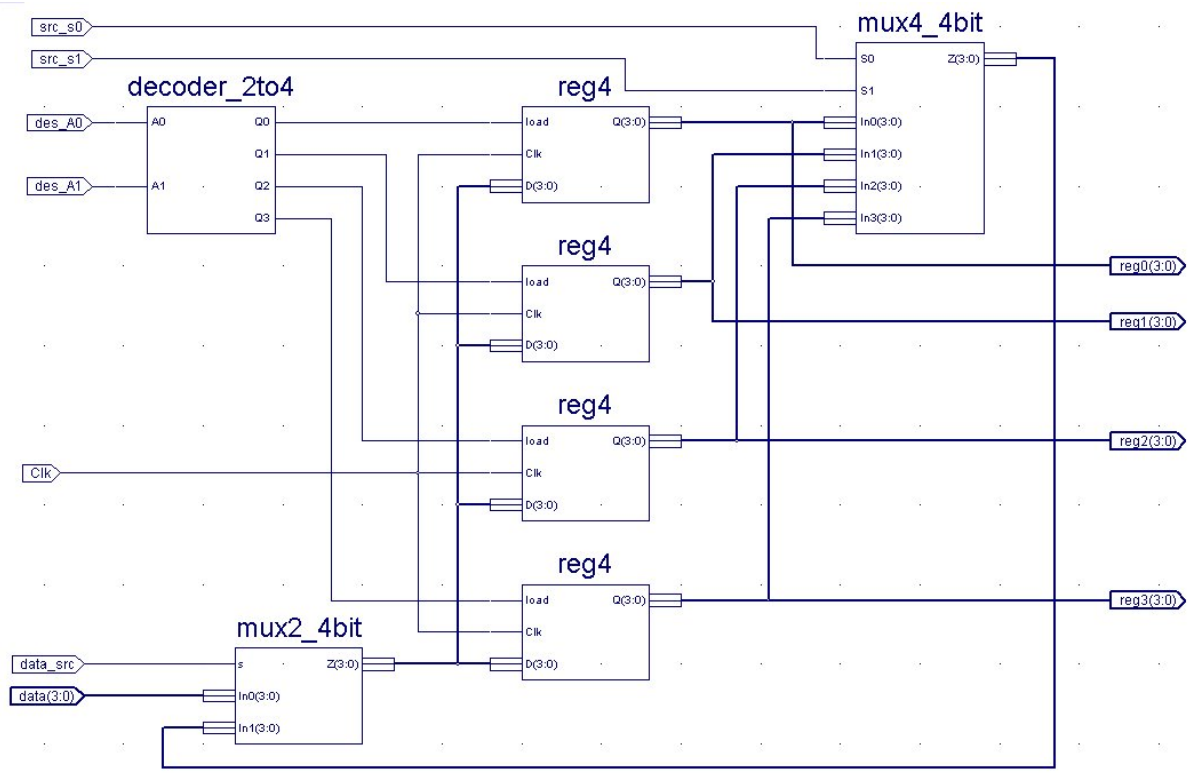
Description:

The circuit overleaf implements a 4-bit version of the Register-file section of the datapath shown in Mano and Kime figure 7-9 (or 4th lecture, page 12), by using components designed in VHDL.

1. Design the VHDL components (Register, Decoder, and two Multiplexer 32 bit) and interconnect them to build a register-file. The schematic shows only four registers. Your solution should implement 32 registers.
2. You should provide test benches and simulations that prove the correctness of the following operations:
    a. Load your StudentID (HEX value) into the first of the 32 registers. Then load your StudentID - 1 (HEX value) into the 2nd register, your StudentID - 2 (HEX value) into the 3rd register... Please continue until all 32 registers have a value.
    b. Transfer the contents of any register to any other register, i.e. that it can execute the transfers R_i <- R_j, I,j=O,31 (show 10 examples)

DUE: Friday, 15th October 2021

Please submit a copy of your VHDL-code and test-benches including all simulation results (screen-shots) to Blackboard. You need VHDL-code and test-benches including all simulation results (screen-shots) for the Register, the Decoder, the two Multiplexer, and the register-file. Please no zip-file or other documents. File naming convention: EntityNameStudentID, EntityNameStudentID_TB, and EntityNameStudentID_SIM01 ...


src_s0
src_s1
mux4_4bit
S0
S1
Z(3:0)
decoder_2to4
reg4
des_A0
des_A1
A0
A1
Q0
Q1
Q2
Q3
load
Clk
D(3:0)
Q(3:0)
In0(3:0)
In1(3:0)
In2(3:0)
In3(3:0)
reg0(3:0)
reg1(3:0)
reg2(3:0)
reg3(3:0)
Clk
mux2_4bit
data_src
data(3:0)
s