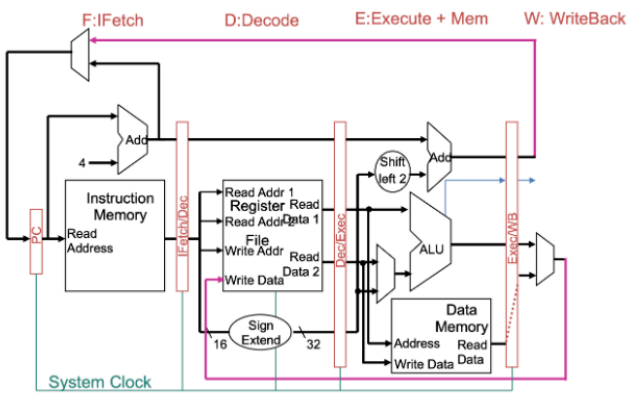
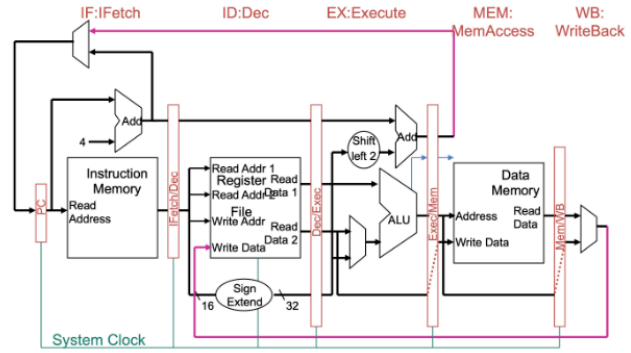
Problem 4:
I didn't read properly and didn't recognize that lw and sw didn't wasn't using immediate values.

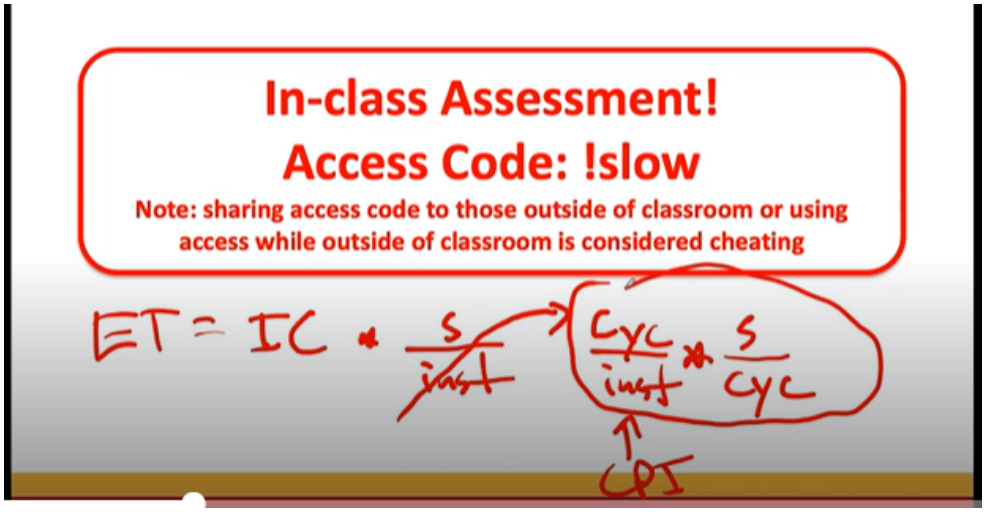
4-stage pipeline design:



Original 5-stage pipeline design:



This means that pushing the mem unit back to the execute stage does not increase the critical path because the alu will never be used prior to the mem unit. This is because they work in parallel. Because the critical path does not change, the frequency should stay the same. This would likely increase the number of instructions as any immediate lw or sw instruction would turn into a pseudo instruction and increase the number of instructions.



CPI = s / inst, this is broken down into cyc / inst and s/cyc

Cyc / inst the cycles per instruction for the 5 cycle would be 5 cycles and it would be 4 for the new 4 cycle pipeline.

s/cyc would stay the same as the critical path would not increase. This is because the mem unit and the alu are in parallel because there are no immediate value mem instructions.

ET = IC * cyc/inst * s/cyc

Et1 = Et2

IC1 * cyc/inst1 * s/cyc1 = IC2 * cyc/inst2 * s/cyc2 --cyc/inst are the same and cancel out
IC1 * cyc/inst1 = IC2 * cyc/inst2 --cyc/inst1 = 5, cyc/inst2 = 4
IC1 * 5 = IC2 * 4
IC1/IC2 = 4/5