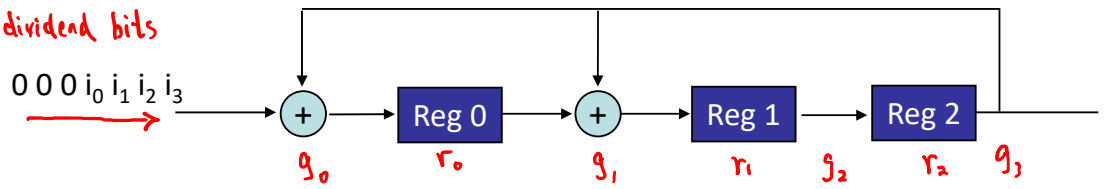
Shift-Register Circuit Implementation

info bits : (1100)

$g(x) = x^3 + x + 1$

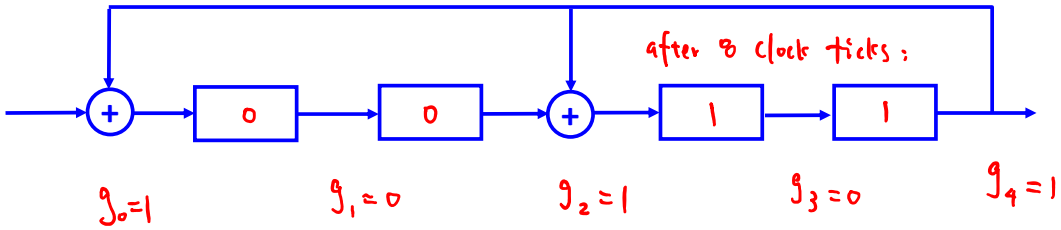
dividend bits



	Clock	Input	Reg 0	Reg 1	Reg 2	
	0	-	0	0	0	← initial
	1	$1 = i_3$	1+0 = 1	0+0 = 0	0	
	2	$1 = i_2$	1	1	0	
	3	$0 = i_1$	0	1	1	
	4	$0 = i_0$	1	1	1	
*	5	0	0+1 = 1	1+1 = 0	1	
	6	0	1	0	0	
	7	0	0	1	0	

Check bits: $r_0 = 0$ $r_1 = 1$ $r_2 = 0$

$\Longrightarrow$ $r(x) = x$



$g(x) = x^4 + x^2 + 1$

E.g. info bits (1111)

$$
\begin{array}{r}
10101 \;\big)\; 11110000 \\
\underline{10101} \\
10110 \\
\underline{10101} \\
1100
\end{array}
$$

⇒ codeword : (1111 | 1100)

$L = 8$

* Example undetectable error burst of length 8 ?

$e = [\,1\ ?\ ?\ ?\ ?\ ?\ ?\ 1\,]_{1\times 8}$

$e(x) = x^7 + ??? + 1$

$= g(x)\cdot c(x) = (x^4 + x^2 + 1)\,c(x)$

$c(x) = x^3 + ?? + 1$

let's pick $c(x) = x^3 + 1 \Rightarrow e(x) = g(x)\,c(x)$

$= x^7 + x^5 + x^4 + x^3 + x^2 + 1$

$\Rightarrow e = [\,1\ 0\ 1\ 1\ 1\ 1\ 0\ 1\,]_{1\times 8}$

$g(x) \rightarrow$ 1 0 1 0 1

$g(x)x^3 \rightarrow$ 1 0 1 0 1

1 0 1 1 1 1 0 1

* Example undetectable $M = 3$ 3-bit error

$g(x) = x^4 + x^2 + 1$

1 0 1 0 1

$e = [\,0\ 0\ 0\ 1\ 0\ 1\ 0\ 1\,]$

* Example undetectable $M = 2$ 2-bit error

1 0 1 0 1 ← $g(x)\cdot 1$

1 0 1 0 1 ← $g(x)\cdot x^2$

$e = [\,0\ 1\ 0\ 0\ 0\ 0\ 0\ 1\,]_{1\times 8}$

$e(x) = x^6 + 1 = g(x)(x^2 + 1)$

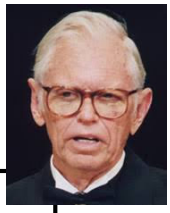
1 0 1 0 1

1 0 1 0 1

1 0 1 0 1

$e = [\,0\ 1\ 1\ 0\ 1\ 0\ 1\ 1\,] = g(x)(x^2 + x + 1)$

Standard Generator Polynomials

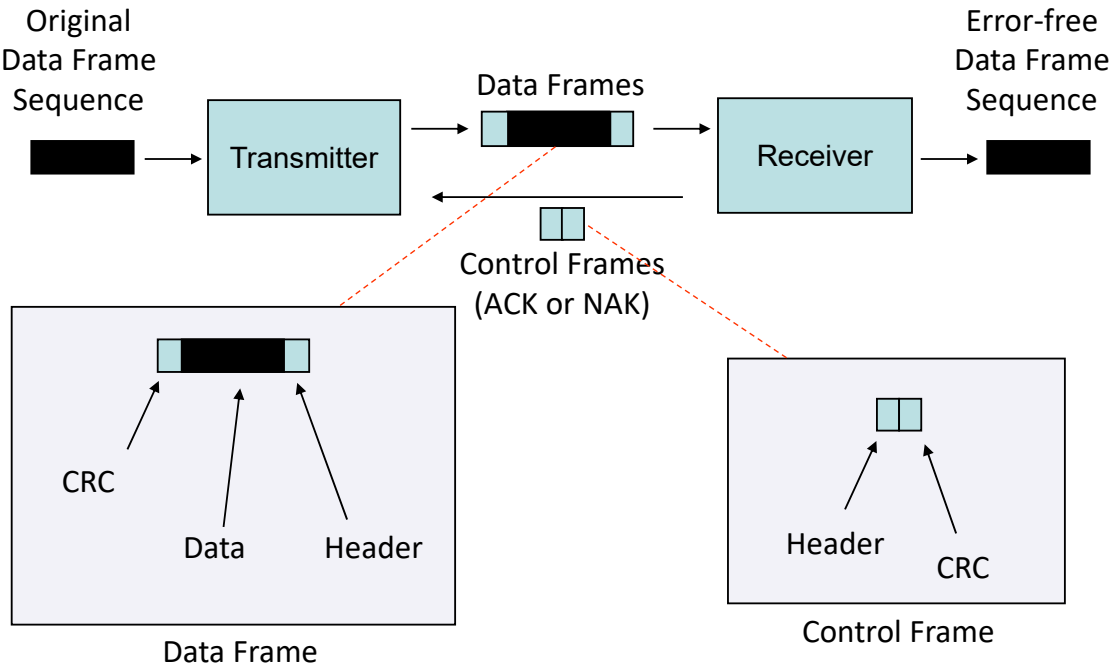


Name	Polynomial	Used in
CRC-8	$x^8 + x^2 + x + 1$	ATM header
CRC-10	$x^{10} + x^9 + x^5 + x^4 + x + 1$	ATM AAL CRC
CRC-12	$x^{12} + x^{11} + x^3 + x^2 + x + 1$ $= (x + 1)(x^{11} + x^2 + 1)$	Bisync
CRC-16	$x^{16} + x^{15} + x^2 + 1$ $= (x + 1)(x^{15} + x + 1)$	Bisync
CCITT-16	$x^{16} + x^{12} + x^5 + 1$	HDLC, XMODEM, V.41
CCITT-32	$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$	IEEE 802, DoD, V.42, AAL5

ARQ (Automatic Repeat reQuest)

- Three Design Goals of ARQ Protocols
  - **Goal #1:** to ensure that each data frame is delivered error-free
  - **Goal #2:** to ensure that each data frame is delivered exactly once without duplication
  - **Goal #3:** to ensure that data frames are delivered in order

ARQ Basics



5 basic elements

① error detection (e.g. CRC)

② control frame : ACK, NAK

required optional

③ sequence number : (SN)

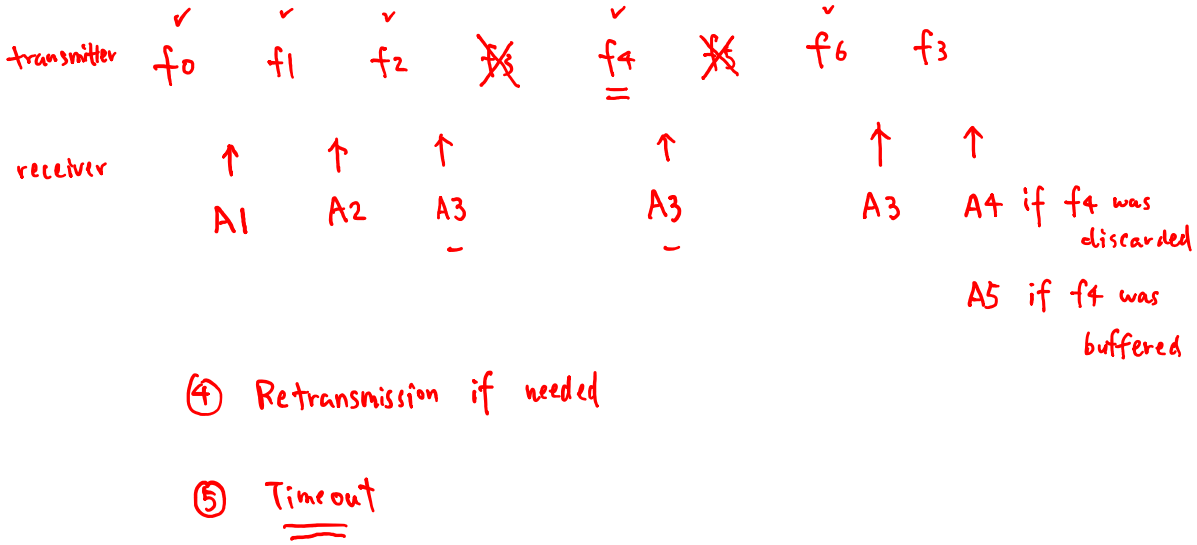
- data frame SN : position in the seq.
- control frame : carries SN

cumulative Acknowledgment

ACK(20)

↑

all data frames with seq. < 20 have already been received correctly



④ Retransmission if needed

⑤ Timeout