
Cpr E 489 Spring 2024

Midterm Exam

Exam Time: 11:00 AM ~ 12:15 PM, March 7, 2024 (Thursday)

Print your name here:

Joseph Schmidt

Honor Code Pledge: *"I have neither given nor received aid in this exam, nor have I concealed any violations of the honor code."*

Sign your name here:

Joseph Schmidt

- There are three (3) big questions for a total of 100 points.
- This is an open-books, open-references, open-notes, and open-assignments examination.
- Is calculator allowed: Yes.
- Is laptop allowed: Yes, to check notes (but cannot be used to browse the Internet).
- Write your answers and all your work in the space provided.

Question 1	46
Question 2	30
Question 3	24
Total	100

+46

1. (46 points) Give a short answer to each of the following questions:

a. (6 points) Briefly explain the key differences between message switching and packet switching transfer modes.

Message switching sends the entire ^{with max size} message while packet switching breaks the message down into packets. Packet switching is more fair as a small message doesn't have to wait for an entire huge message to be sent as it's broken into packets so the long message can send a packet then the small message can send its packet.

b. (6 points) Briefly explain the key differences between mBnB and mBnT line coding schemes.

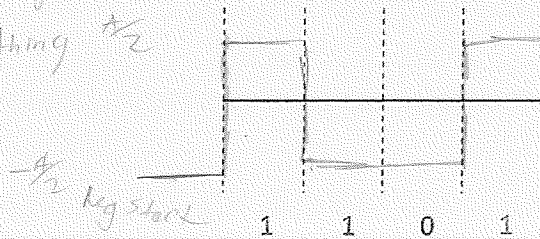
mBnB maps block of m information bits into n pulses. mBnT is the ternary version so instead of the pulses having 2 values like in mBnB binary, pulses will have 3 values.

c. (6 points) Briefly explain the key differences between 1-persistent and non-persistent options of the CSMA MAC protocol.

1-persistent is more greedy, has more collisions, but has a lower delay. non-persistent is less greedy, fewer collisions, but has a higher delay. This comes from the fact that if the non-persistent protocol sees the channel is not busy it will do a random backoff before trying to send. This is why it's a longer delay, less greedy and why there it's less collisions.

d. (7 points) For a stream of four bits: 1101, sketch the waveform for NRZ-Inverted line coding scheme in the figure below. Suppose the waveform in the bit interval prior to 1101 ends at a negative voltage level.

* 1 is flip signal
* 0 do nothing



e. (7 points) Consider a noisy AWGN communication channel with a channel bandwidth of 100 KHz. The goal is to transmit reliably over this channel at a bit rate of 1 Mbps. Which of the following SNR (Signal to Noise Ratio) is able to accomplish this?

- i. 1100 (absolute value; no unit)
- ii. 30 dB
- iii. Both (i) and (ii)
- iv. None of the above

very close but should be .1 higher for Markov inequality

30db is not greater than 30.1db

$$C = W \log_2(1 + \text{SNR})$$

$$R = 1 \text{ Mbps}$$

$$W = 100 \text{ kHz}$$

$$C \geq R = 1 \text{ Mbps}$$

$$W \log_2(1 + \text{SNR}) \geq R = 1 \text{ Mbps}$$

$$100 \text{ kHz} \log_2(1 + \text{SNR}) \geq 1 \text{ M}$$

$$\log_2(1 + \text{SNR}) \geq 10$$

$$1 + \text{SNR} \geq 2^{10}$$

$$\text{SNR} \geq 1023$$

In dB

$$10 \log_{10}(1023) \approx 30.0987 \text{ dB}$$

$$\text{SNR} \geq 30.1$$

- f. (7 points) An (n, 1) repetition error detection code is defined as follows: each codeword is n-bit long; the first bit of a codeword is a single information bit and the following (n - 1) check bits are repetitions of the information bit. What is the FUE (Fraction of Undetectable Errors) of a (5, 1) repetition code?

- i. 1/3
ii. 1/7
iii. 1/15
iv. None of the above

$FUE = \frac{2^K - 1}{2^n - 1}$ $K = \text{info bits}$

$i_0 \quad c_3 \quad c_2 \quad c_1 \quad c_0$

only 1 info bit

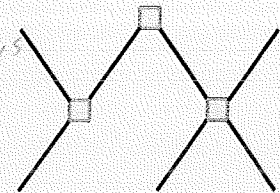
$\frac{2^1 - 1}{2^5 - 1} = \frac{1}{31}$

- g. (7 points) A CSMA/CD-based half-duplex LAN consists of 7 segments connected by 3 repeaters, as shown in the figure. The maximum length of each segment is 80 meters and the processing delay at each repeater is 1 μ s. It transmits at 100 Mbps and signal propagates at 2×10^8 m/s. What is the minimum frame size required for this CSMA/CD-based half-duplex LAN to operate properly?

- i. 460 bits
ii. 920 bits
iii. 1160 bits
iv. None of the above

$t_{prop} = \frac{80 \text{ m} \times 4}{2 \times 10^8 \text{ m/s}} + 1 \mu\text{s} \times 3 = 4.6 \mu\text{s}$

$2 \times t_{prop} \times R = 9.2 \mu\text{s} \times 100 \text{ Mbps} = 920 \text{ bits}$



+30

2. (30 points) Consider a CRC code with a generator polynomial of $g(x) = x^5 + x^3 + 1$.

- a. (10 points) Show step-by-step (using long division) how to find the codeword that corresponds to five information bits of 10110.

$S(x) = 10110$

$g(x) = x^5 + x^3 + 1$

Long division:

```

      x^4 + x
    1011001
  1011001
  -----
    000101000
    1011001
    -----
    0000010
  
```

Therefore, $r(x) = x$

$i(x) = x^4 + 0x^3 + x^2 + x + 0$

$i(x) * (g(x) \text{ mod } x^5) = x^9 + x^7 + x^6$

$\Rightarrow k(x) = x^5 * i(x) + r(x)$

$k(x) \text{ mod } x^5 = x^4 + x^3 + x^2 + x$

$\Rightarrow \text{codeword} = [1011000010]$

- b. (10 points) Suppose the codeword length is 10. Give an example error vector of an undetectable error burst of length 8 (L = 8). Justify your answer.

undetectable

$e(x) = c(x) \cdot g(x)$

1010011

101001

x^2

10001101

$e(x) = (x^2 + 1)(x^5 + x^3 + 1)$ 8 error burst

$e(x) = [0010001101]$

9 8 7 6 5 4 3 2 1 0

- (M = 4). Justify your answer.
- Undetectable
- $$e(x) = e(x) \cdot g(x)$$
- $$= (x^2 + 1)(x^3 + x + 1)$$
- $$e(x) = [00 \underbrace{10001101}_{10}]$$
- 4 error bits
- ✓

- + 24

- exchange sequence until all five data frames are delivered successfully.
- a. (12 points) Go-Back-N ARQ protocol with $N = 3$.
-
- Handwritten notes on the diagram:
- seq 0,1,2,3
 - seq 1,2,3,3
 - Timeout based on f_3
 - seq 2,3,4,5
 - seq 3,4,5,6
 - Only has f_4 to send, f_5 & f_6 don't exist
 - f_0, f_1, f_2
 - f_3, f_4, f_5
 - f_1, f_2, f_3
 - f_4, f_5
 - $A_1 = A_4$
 - $A_2 = A_3$

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- The diagram illustrates the execution of a program on a multi-processor system with a shared cache. The diagram shows two processors, A and B, and a timeline of events. Processor A starts at time 0 and executes instructions $f_0, f_1, f_2, f_3, f_4, f_5, f_6, f_7$. Processor B starts at time 0 and executes instructions A_1, A_2, A_3, A_4, A_5 . The diagram shows that Processor A's execution is interrupted by Processor B's execution, and the cache state is updated accordingly. The final state of the cache is "complete".