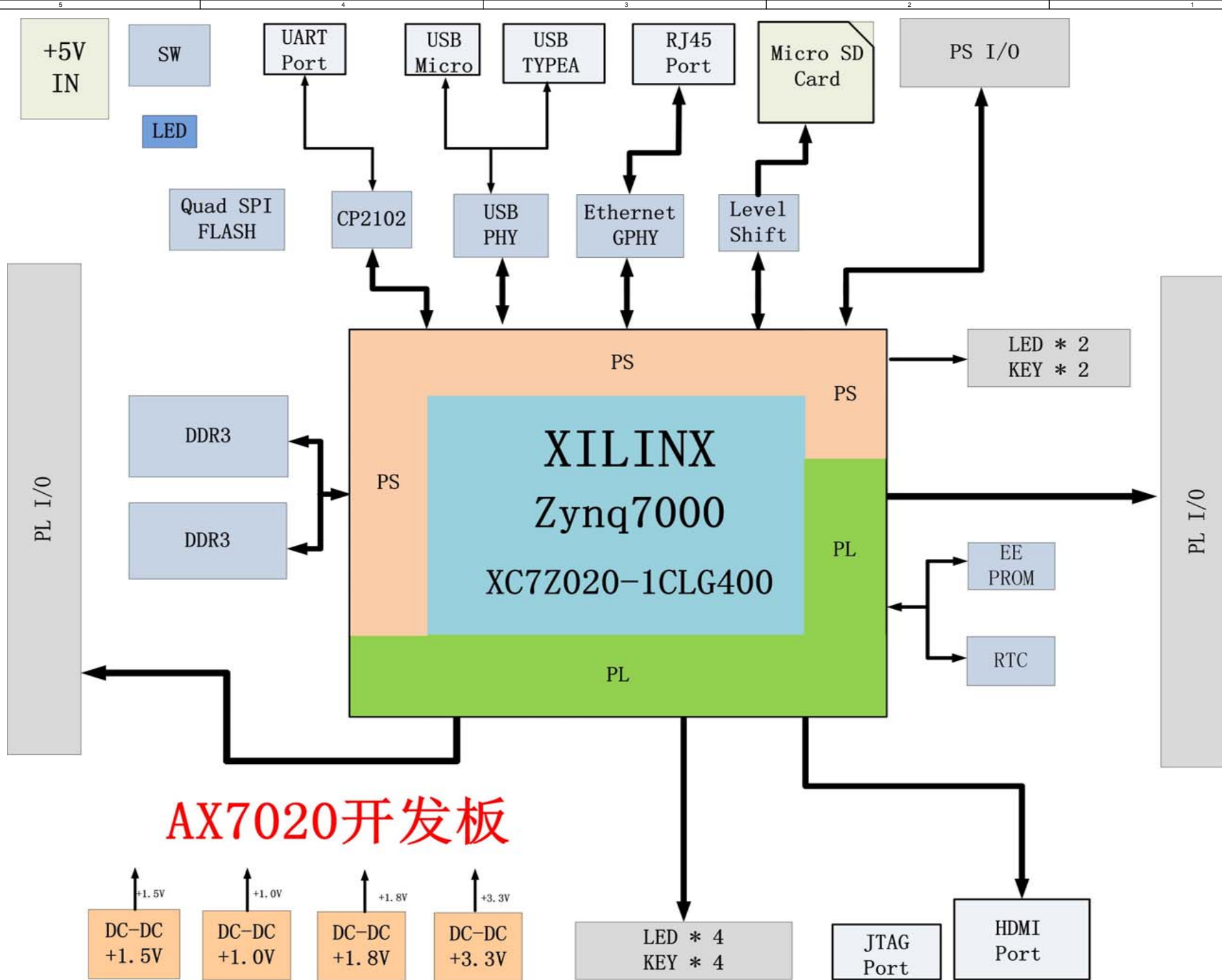


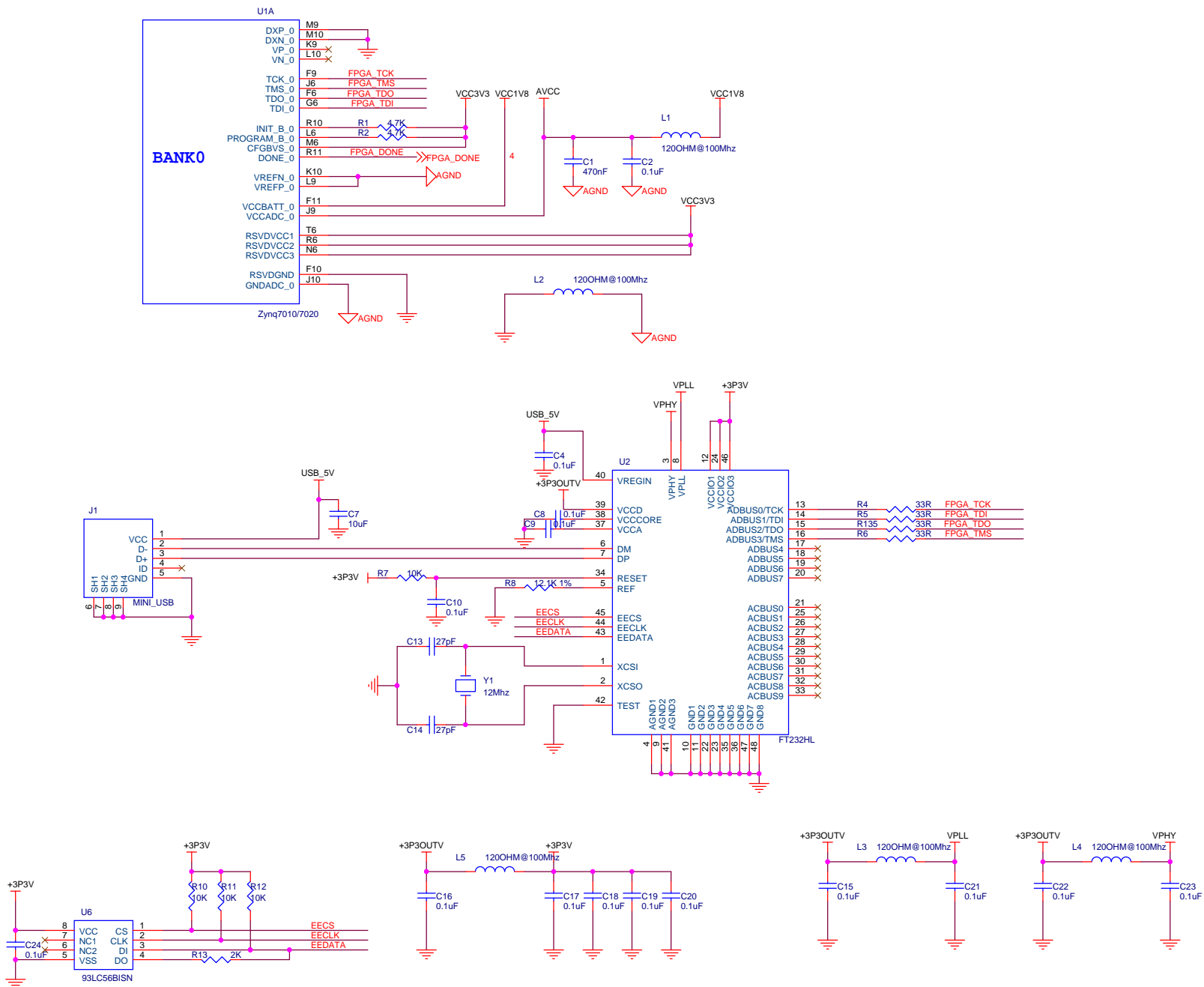
REV	Description	Date
V1.0	First Release	2016-7-12

AX7010/AX7020 Schematics

黑金ZYNQ硬件平台

Page Number	Description
Page01	Cover Page
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Page05	Zynq-7000 Bank13-34-35
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Page07	Zynq-7000 Power
Page08	DDR3
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BOOT OPTION

The diagram illustrates the boot options for the device, showing connections for JTAG, QSPI, and SD. The 4-pin header (J13) is connected to VCC3V3 and ground. The connections are as follows:

- JTAG:** JTAG is connected to VCC3V3 via R15 (20K).
- QSPI:** QSPI D0 is connected to VCC3V3 via R16 (20K). QSPI D1 is connected to VCC3V3 via R17 (20K). QSPI SCK is connected to VCC3V3 via R18 (20K). QSPI D2 is connected to VCC3V3 via R19 (20K).
- PS MIO:** PS MIO8 is connected to VCC3V3 via R20 (20K). PS MIO7 is connected to VCC3V3 via R21 (20K).

The boot mode is determined by the configuration of MIO[5] (QSPI_D3) and MIO[4] (QSPI_D2). The table below shows the boot mode and the corresponding MIO pin configurations.

Boot Mode	MIO[5] (QSPI_D3)	MIO[4] (QSPI_D2)
JTAG	0	0
NAND	0	1
QSPI-FLASH	1	0
SD Card	1	1

POWER ON RESET

The diagram illustrates a Power On Reset (POR) circuit. A push button, labeled KEY1, is connected to the #MR pin (pin 3) of the TCM811T ERTCTR chip (U7). The other side of the button is connected to ground. The VDD pin (pin 4) of the chip is connected to a 3.3V supply (VCC3V3) through a 0.1μF capacitor (C27). The #RESET pin (pin 2) of the chip is connected to the PS POR.B output. The chip is also connected to ground at pins 1 and 2.

U1B

VCC3V3

BANK500

PS_MIO0_500

PS_MIO1_500

PS_MIO2_500

PS_MIO3_500

PS_MIO4_500

PS_MIO5_500

PS_MIO6_500

PS_MIO7_500

PS_MIO8_500

PS_MIO9_500

PS_MIO10_500

PS_MIO11_500

PS_MIO12_500

PS_MIO13_500

PS_MIO14_500

PS_MIO15_500

PS_POR_B_500

PS_CLK_500

E6

A7

B8

D6

B7

A6

A5

D8

D5

B5

E9

C6

D9

E8

C5

C8

C7

E7

MIO0_LED

QSPI_CS

QSPI_D0

QSPI_D1

QSPI_D2

QSPI_D3

QSPI_SCK

PS_MIO7

PS_MIO8

PS_MIO9

PS_MIO10

PS_MIO11

PS_MIO12

MIO13_LED

PS_MIO14

PS_MIO15

PS_POR_B

33R

R20

33R

X1

OUT

VDD

GND

OE

33.333333Mhz

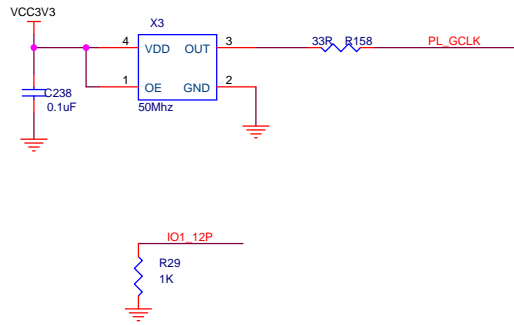
C25

0.1uF

VCC3V3

Zynq7010/7020

[illegible]



11 RTC_SCLK
11 EEPROM_I2C_SCL
15 IO1_15P
15 IO1_15N
15 IO1_14N
15 IO1_12P
15 IO1_12N
15 IO1_13P
15 IO1_13N
15 IO1_11N
15 IO1_2P
15 IO1_2N
15 IO1_3P
15 IO1_3N
15 IO1_5P
15 IO1_5N
15 IO1_9P
15 IO1_9N
15 IO1_4P
15 IO1_4N

VCC3V3 BANK34

IO_0_34
IO_25_34
IO_L11P_T1_SRCC_34
IO_L12P_T1_MRCC_34
IO_L12N_T1_MRCC_34
IO_L13P_T2_MRCC_34
IO_L13N_T2_MRCC_34
IO_L14P_T2_SRCC_34
IO_L14N_T2_SRCC_34
IO_L15P_T2_DQS_34
IO_L15N_T2_DQS_34
IO_L16P_T2_34
IO_L16N_T2_34
IO_L17P_T2_34
IO_L17N_T2_34
IO_L18P_T2_34
IO_L18N_T2_34
IO_L19P_T2_34
IO_L19N_T3_VREF_34
IO_L20P_T3_34
IO_L20N_T3_34
IO_L21P_T3_DQS_34
IO_L21N_T3_DQS_34
IO_L22P_T3_34
IO_L22N_T3_34
IO_L23P_T3_34
IO_L23N_T3_34
IO_L24P_T3_34
IO_L24N_T3_34

IO1_7P
IO1_7N
EEPROM_I2C_SDA
HDMI_CLK_P
HDMI_CLK_N
HDMI_D2_P
HDMI_D2_N
HDMI_D1_P
HDMI_D1_N
HDMI_D0_P
HDMI_D0_N
HDMI_CEC
HDMI_HPD
HDMI_OUT_EN
HDMI_SDA
KEY4
KEY3
HDMI_SCL
IO1_10P
IO1_10N
IO1_1P
IO1_1N
IO1_6P
IO1_6N
IO1_8P
IO1_8N

Zynq7010/7020

VCC3V3 BANK13 (Z7020 Only)

IO_L6N_T0_VREF_13
IO_L11P_T1_SRCC_13
IO_L11N_T1_SRCC_13
IO_L12P_T1_MRCC_13
IO_L12N_T1_MRCC_13
IO_L13P_T2_MRCC_13
IO_L13N_T2_MRCC_13
IO_L14P_T2_SRCC_13
IO_L14N_T2_SRCC_13
IO_L15P_T2_DQS_13
IO_L15N_T2_DQS_13
IO_L16P_T2_13
IO_L16N_T2_13
IO_L17P_T2_13
IO_L17N_T2_13
IO_L18P_T2_13
IO_L18N_T2_13
IO_L19P_T3_13
IO_L19N_T3_VREF_13
IO_L20P_T3_13
IO_L20N_T3_13
IO_L21P_T3_DQS_13
IO_L21N_T3_DQS_13
IO_L22P_T3_13
IO_L22N_T3_13

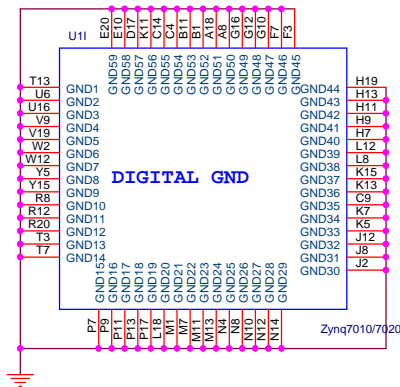
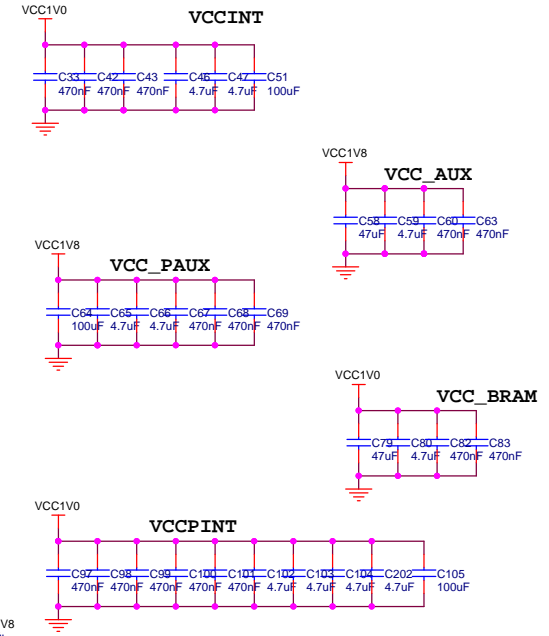
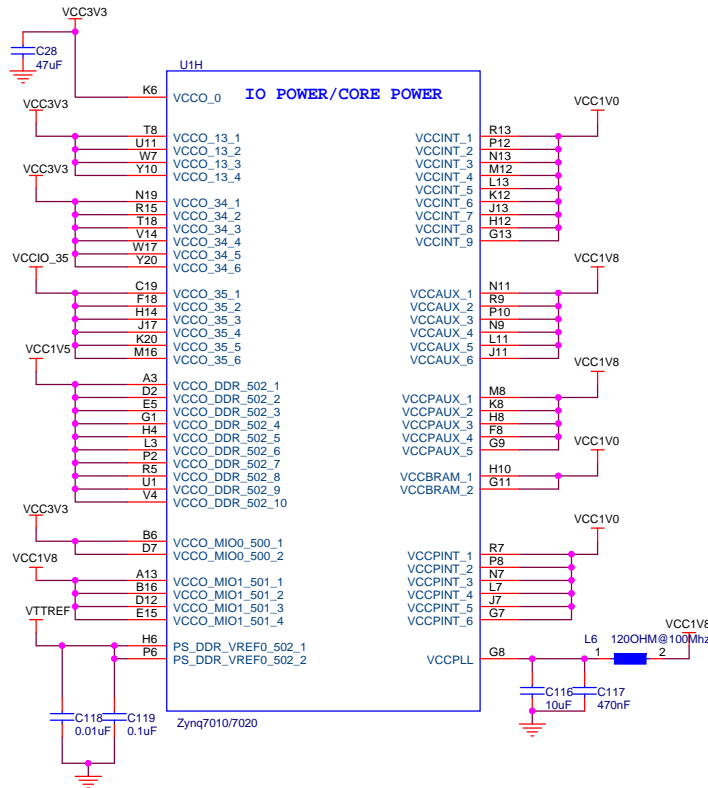
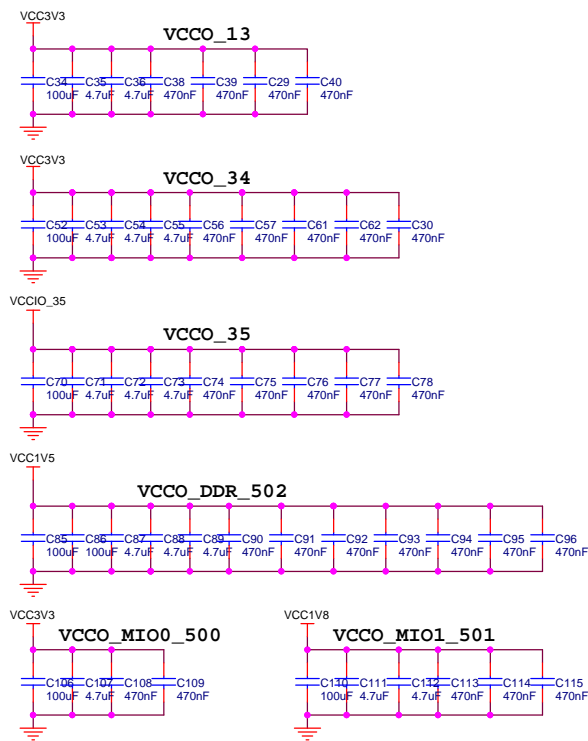
Zynq7010/7020

VCCIO BANK35

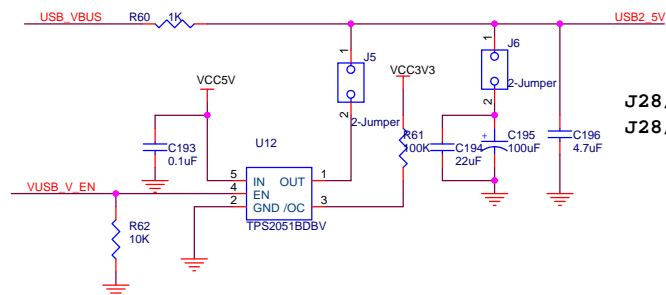
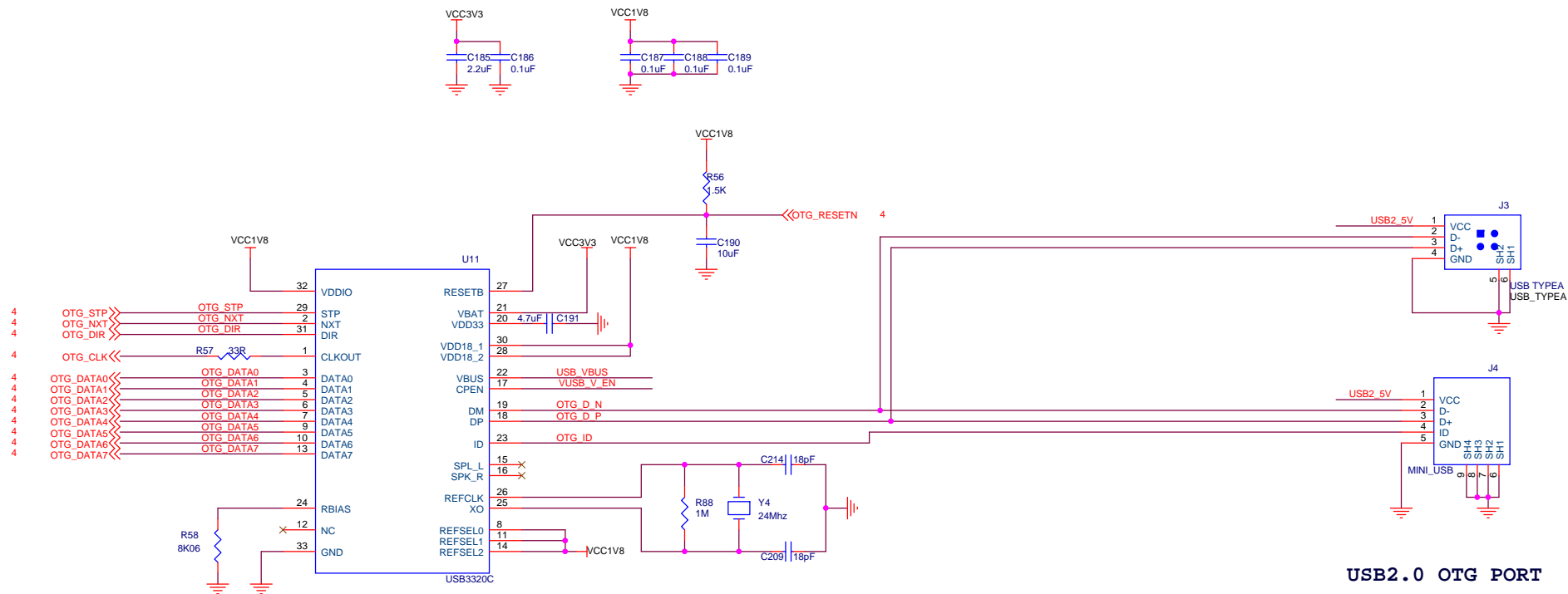
IO_0_35
IO_25_35
IO_L11P_T0_AD0P_35
IO_L11N_T0_AD0N_35
IO_L12P_T0_AD0P_35
IO_L12N_T0_AD0N_35
IO_L13P_T2_MRCC_35
IO_L13N_T2_MRCC_35
IO_L14P_T2_AD4P_SRCC_35
IO_L14N_T2_AD4N_SRCC_35
IO_L15P_T2_DQS_AD12P_35
IO_L15N_T2_DQS_AD12N_35
IO_L16P_T2_35
IO_L16N_T2_35
IO_L17P_T2_AD5P_35
IO_L17N_T2_AD5N_35
IO_L18P_T2_AD13P_35
IO_L18N_T2_AD13N_35
IO_L19P_T3_35
IO_L19N_T3_VREF_35
IO_L20P_T3_AD6P_35
IO_L20N_T3_AD6N_35
IO_L21P_T3_DQS_AD14P_35
IO_L21N_T3_DQS_AD14N_35
IO_L22P_T3_AD7P_35
IO_L22N_T3_AD7N_35
IO_L23P_T3_35
IO_L23N_T3_35
IO_L24P_T3_AD15P_35
IO_L24N_T3_AD15N_35

IO2_10P
IO2_10N
IO2_7P
IO2_7N
IO2_15P
IO2_15N
IO2_4P
IO2_4N
IO2_2P
IO2_2N
IO2_14P
IO2_14N
IO2_9P
IO2_9N
IO2_3P
IO2_3N
IO2_16P
IO2_16N
IO2_17P
IO2_17N
KEY1
KEY2
RTC_DATA
RTC_RESET
LED1
LED2
LED3
LED4

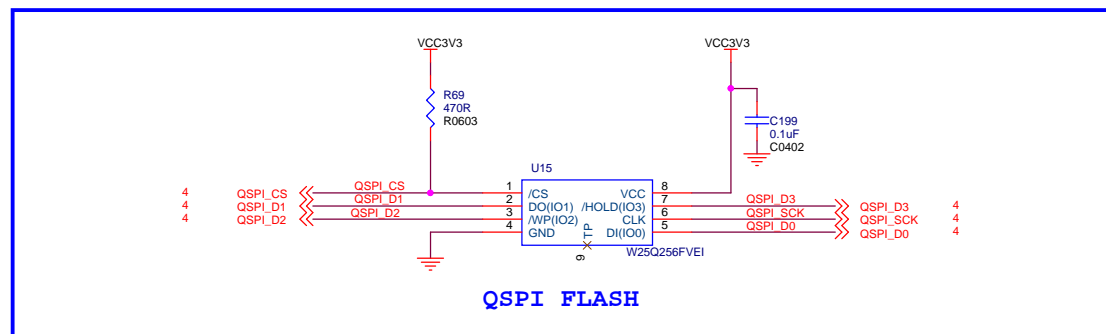
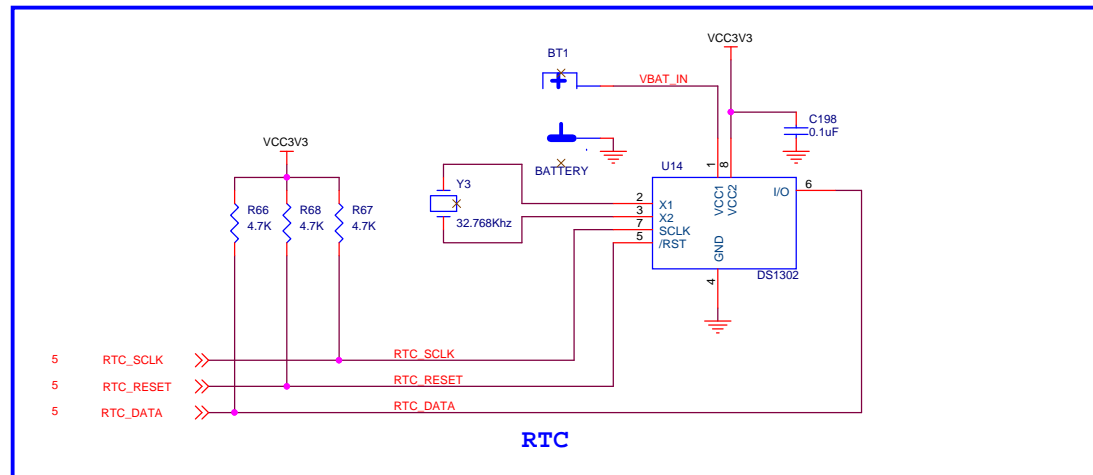
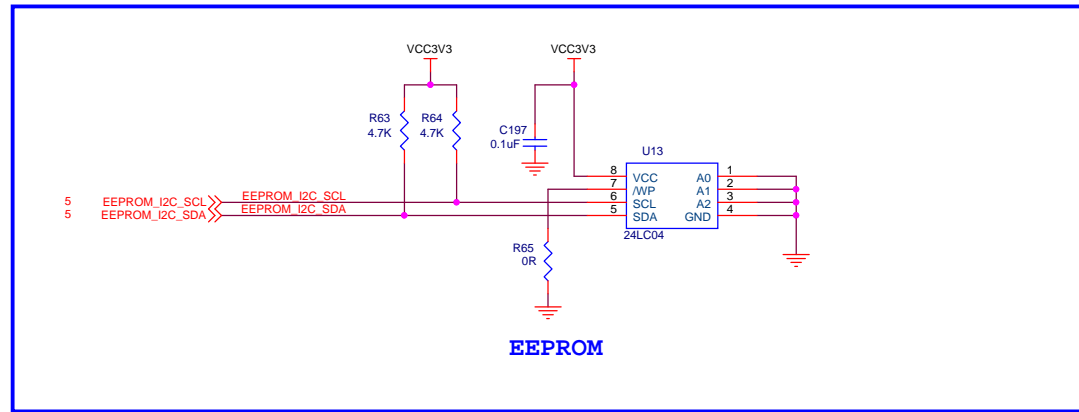
Zynq7010/7020

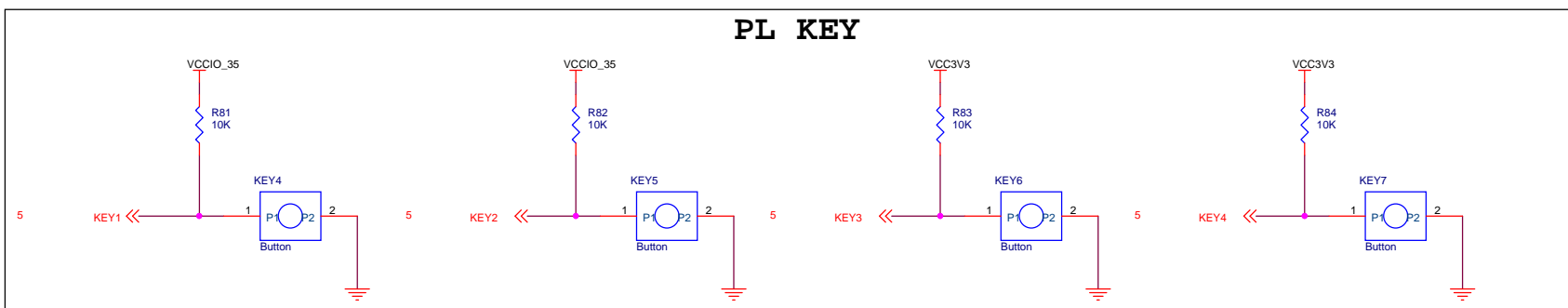
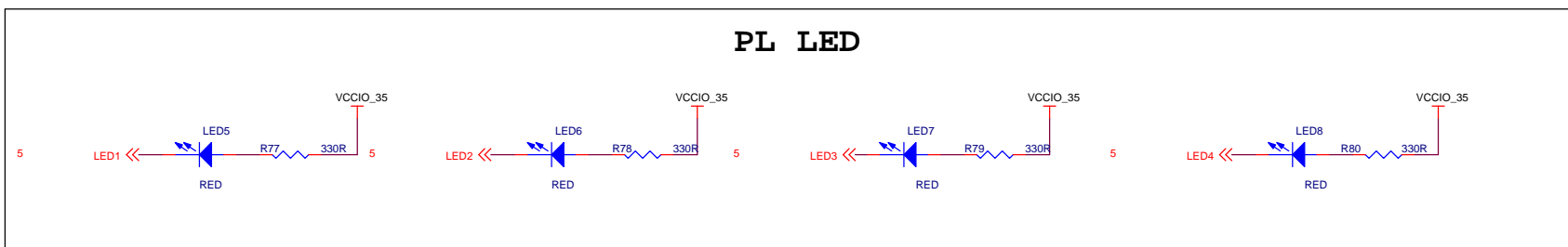
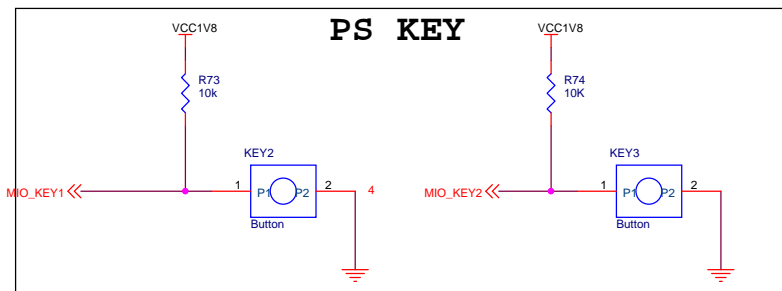
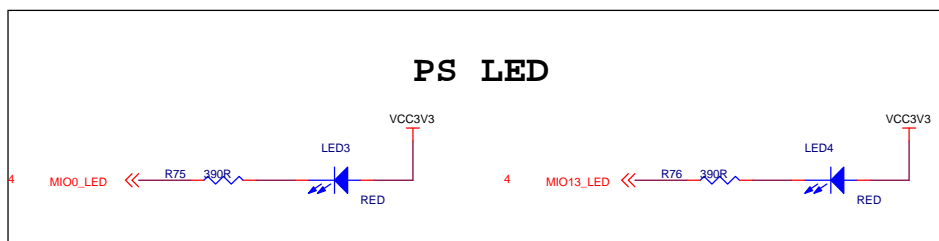
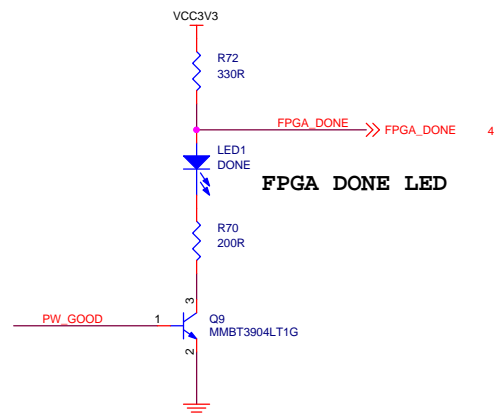
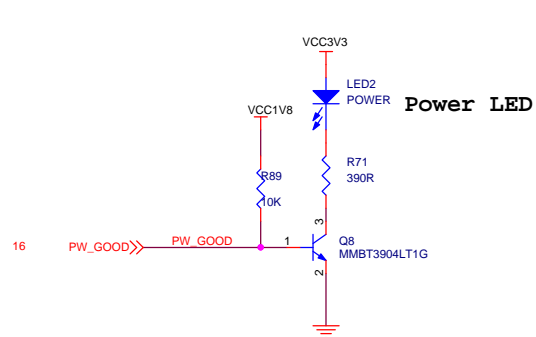




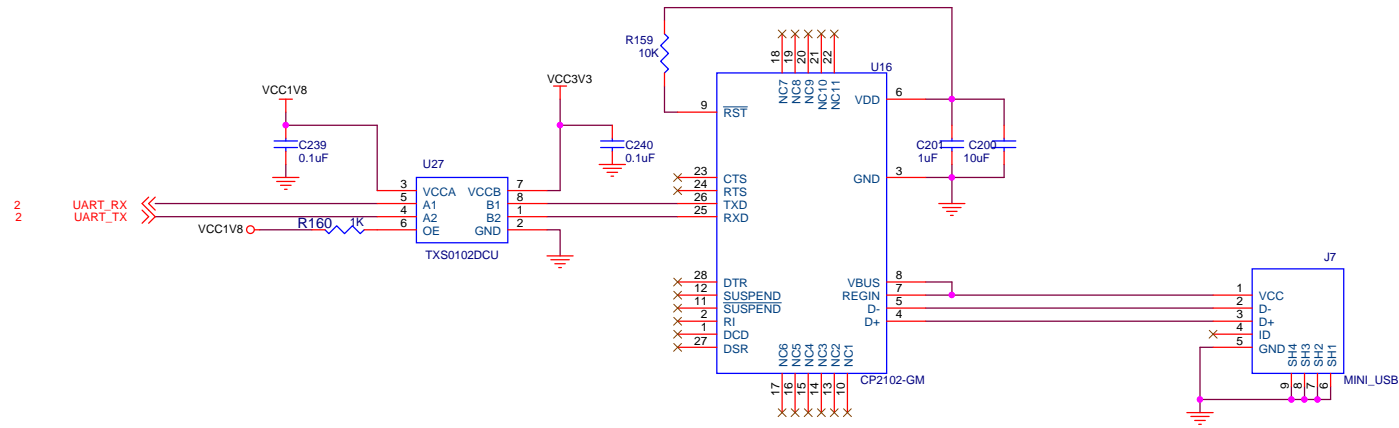


J28/J29 Connect: Host Mode
J28/J29 Not Connect: Slave/OTG Mode

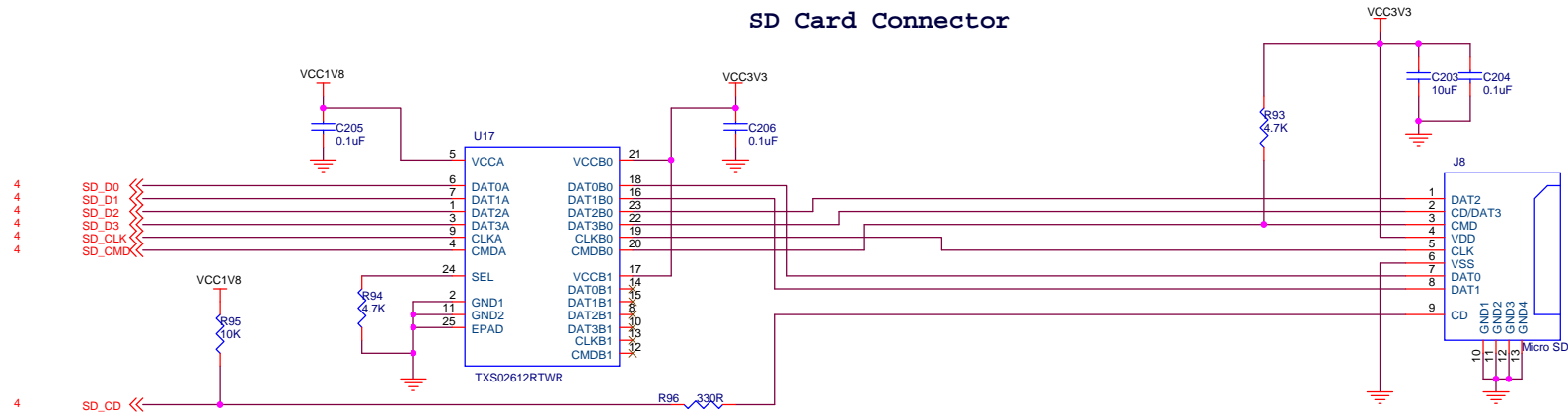




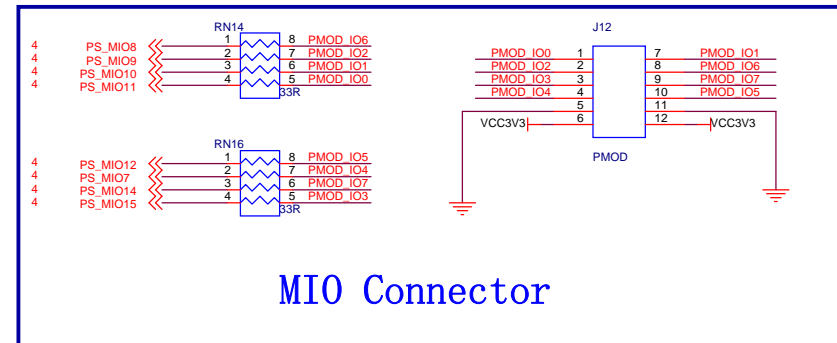
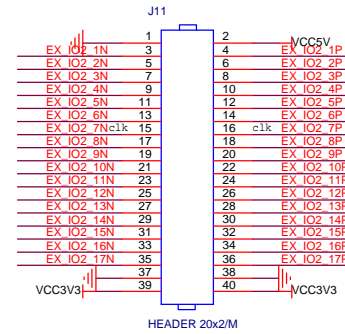
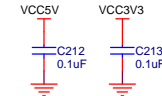
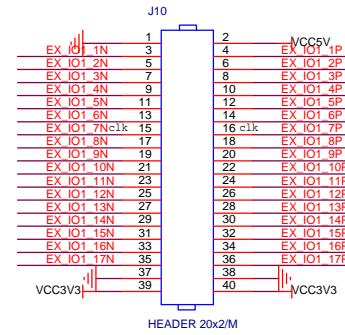
USB Uart



SD Card Connector

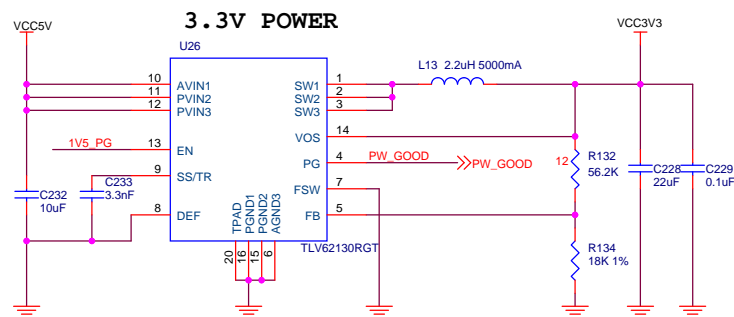
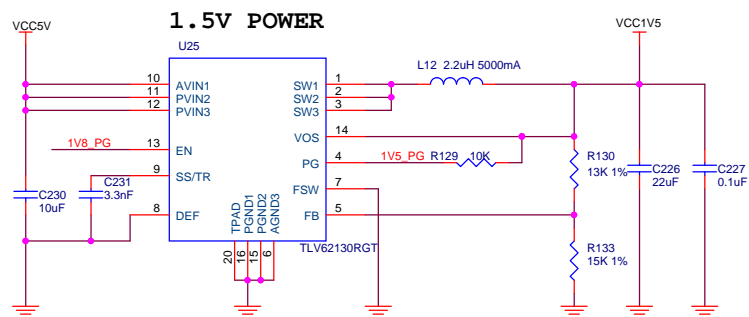
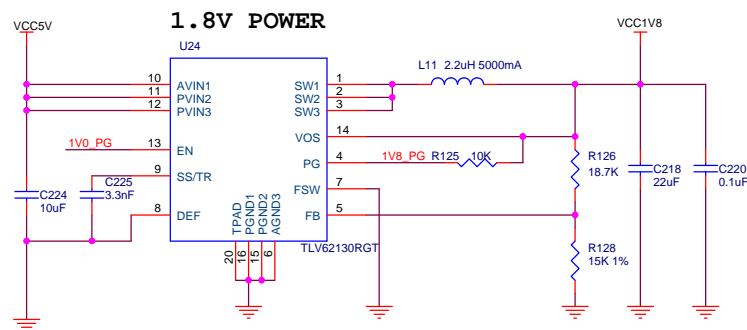
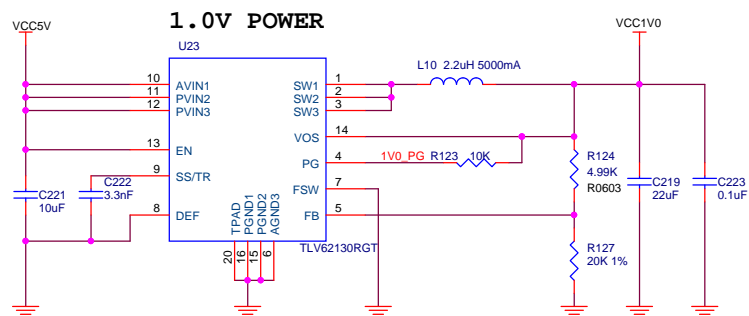
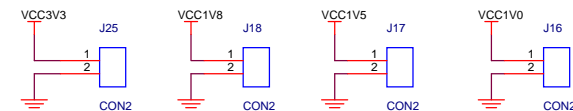
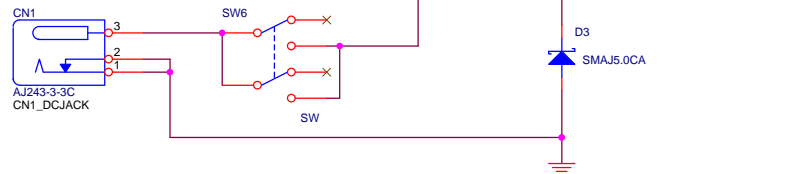


FPGA 40 PIN External IO



MIO Connector

5V/2A AC Adapter



Power On Sequence:

1.0V -> 1.8V -> 1.5 V -> 3.3V -> VCCIO

