CS223 : Assignment 5, Date of Demonstration 16th March 2018, Lab Timing (2PM-5PM), 10% (7%+3%) weight

(Part I is subset of Part II, showing Part II successfully do not require to show part I.)

Part I (VHDL and FPGA: 70%) : MFU on stand alone FPGA

Design and implement a 8 bit eight functions multi-functional unit (MFU) using HDL (either VHDL or Verilog, preferred VHDL), synthesize and simulate your design entry. After that download bit file of your design to FPGA board and demonstrate the working of your design on FPGA. ***Assume all the inputs are unsigned and all the computations are to be done in integer domain.***

Your MFU required to interface with a memory of 16 location each 16 bits. You should store input numbers in first 8 locations and computed results in next 8 locations. Inputs are 8 bits and result may be of 16 bit. MFU should be able to compute (1) sum, (2) mean, (3) median, (4) max, (5) min, (6) mode, (7) range (max-min) and (8) mid range ((max+min)/2). Your multi-functional unit should support 4 modes: INPUT mode, DISPLAY mode, COMPUTE mode and RESET mode.

- In INPUT mode, you should be able to input 8 bit number from switches of FPGA board (one after another) and store to particular location of memory (pointed by some switches to memory location/address).
- In COMPUTE mode, the designed MFU should compute all the required function and put the result in respective locations. (***You should not compute at the time of taking inputs***)
- In DISPLAY mode, you should be able to display the contents of a memory location. Memory address should be specified using some switches of FPGA in DISPLAY mode.
- In RESET mode, it should initialize contents of all the memory locations of MFU to 0s.

You should be able to demonstrate sequence of RESET, DISPLAY, INPUT, DISPLAY, COMPUTE DISPLAY. RESET, DISPLAY, INPUT, COMPUTE, DISPLAY.

Grade will be based on Functionality, quality (less resources (LUTs, SR, DSP Slices), low delay/high frequency) of design.

Part II (Demonstrate MFU with FPGA and PC Communication: 30%)

Interface UART of FPGA with PC USB port to send and receive data. In UART 8 bit data can be send at time and similarly 8 bit data can be received. Do operation in two phases

- From PC, send mode (2bit) and memory address (4 bit) in first 8 bit.
- Based on mode: If mode is INPUT then send another 8 bit data. If the mode is RESET mode then simply clear the MFU. If the mode is COMPUTE then compute the results. And the mode is DISPLAY, get the result data from the memory to output register and read 8 bit data to PC from FPGA using UART port.

  Hint: Use the Basys 3, general IO demo for help in communications between FPGA and PC. https://reference.digilentinc.com/learn/programmable-logic/tutorials/basys-3-general-io/start
  Hint: Use the ATLYS Board, general IO demo for help in communications between FPGA and PC. https://reference.digilentinc.com/_media/atlys/atlys/atlys_ise_gpio_uart.zip

Other options are : Send 8 eight bit data to FPGA, compute MFU functions in FPGA, get 16 eight bit 16 bit data (or 32 eight bit data) from FPGA to PC and display them. Also display some part of result in LEDS of FPGA.

This PC to USB communication will be used in the next two assignments.

Evaluation Procedure

All the member of the group need to be present at the time of Demonstration of the assignment. All the absent members will be awarded 0 marks for the assignment. Please **show your ID card** at the time of demonstration (as it is difficult to remember faces of all the 90 students of your batch).

For HDL codes the quality will be based on FPGA minimum resource utilization (Synthesis Report: optimized number of LUTs, register, Minimum Clock), coding style (Use of proper Comment/Naming/Labeling of the wires), performance, comments, and questionnaire and explanation.