# Linux generic IRQ handling

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```

#### 10. Credits

#### **Chapter 1. Introduction**

The generic interrupt handling layer is designed to provide a complete abstraction of interrupt handling for device drivers. It is able to handle all the different types of interrupt controller hardware. Device drivers use generic API functions to request, enable, disable and free interrupts. The drivers do not have to know anything about interrupt hardware details, so they can be used on different platforms without code changes.

This documentation is provided to developers who want to implement an interrupt subsystem based for their architecture, with the help of the generic IRQ handling layer.

#### **Chapter 2. Rationale**

The original implementation of interrupt handling in Linux is using the \_\_do\_IRQ() super-handler, which is able to deal with every type of interrupt logic.

Originally, Russell King identified different types of handlers to build a quite universal set for the ARM interrupt handler implementation in Linux 2.5/2.6. He distinguished between:

- Level type
- Edge type
- Simple type

In the SMP world of the \_\_do\_IRQ() super-handler another type was identified:

• Per CPU type

This split implementation of highlevel IRQ handlers allows us to optimize the flow of the interrupt handling for each specific interrupt type. This reduces complexity in that particular codepath and allows the optimized handling of a given type.

The original general IRQ implementation used hw\_interrupt\_type structures and their ->ack(), ->end() [etc.] callbacks to differentiate the flow control in the super-handler. This leads to a mix of flow logic and lowlevel hardware logic, and it also leads to unnecessary code duplication: for example in i386, there is a ioapic\_level\_irq and a ioapic\_edge\_irq irq-type which share many of the lowlevel details but have different flow handling.

A more natural abstraction is the clean separation of the 'irq flow' and the 'chip details'.

Analysing a couple of architecture's IRQ subsystem implementations reveals that most of them can use a generic set of 'irq flow' methods and only need to add the chip level specific code. The separation is also valuable for (sub)architectures which need specific quirks in the irq flow itself but not in the chip-details - and thus provides a more transparent IRQ subsystem design.

Each interrupt descriptor is assigned its own highlevel flow handler, which is normally one of the generic implementations. (This highlevel flow handler implementation also makes it simple to provide demultiplexing handlers which can be found in embedded platforms on various architectures.)

The separation makes the generic interrupt handling layer more flexible and extensible. For example, an (sub)architecture can use a generic irq-flow implementation for 'level type' interrupts and add a (sub)architecture specific 'edge type' implementation.

To make the transition to the new model easier and prevent the breakage of existing implementations, the \_\_do\_IRQ() super-handler is still available. This leads to a kind of duality for the time being. Over time the new model should be used in more and more architectures, as it enables smaller and cleaner IRQ subsystems.

# **Chapter 3. Known Bugs And Assumptions**

None (knock on wood).

# **Chapter 4. Abstraction layers**

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Default flow implementations
Default flow handler implementations
Quirks and optimizations
Delayed interrupt disable

#### Chiplevel hardware encapsulation

There are three main levels of abstraction in the interrupt code:

- 1. Highlevel driver API
- 2. Highlevel IRQ flow handlers
- 3. Chiplevel hardware encapsulation

#### **Interrupt control flow**

Each interrupt is described by an interrupt descriptor structure irq\_desc. The interrupt is referenced by an 'unsigned int' numeric value which selects the corresponding interrupt decription structure in the descriptor structures array. The descriptor structure contains status information and pointers to the interrupt flow method and the interrupt chip structure which are assigned to this interrupt.

Whenever an interrupt triggers, the lowlevel arch code calls into the generic interrupt code by calling desc->handle\_irq(). This highlevel IRQ handling function only uses desc->chip primitives referenced by the assigned chip descriptor structure.

### **Highlevel Driver API**

The highlevel Driver API consists of following functions:

- request\_irq()
- free\_irq()
- disable\_irq()
- enable\_irq()

- disable\_irq\_nosync() (SMP only)
- synchronize\_irq() (SMP only)
- set\_irq\_type()
- set\_irq\_wake()
- set\_irq\_data()
- set\_irq\_chip()
- set\_irq\_chip\_data()

See the autogenerated function documentation for details.

### **Highlevel IRQ flow handlers**

The generic layer provides a set of pre-defined irq-flow methods:

- handle\_level\_irq
- handle\_edge\_irq
- handle\_simple\_irq
- handle\_percpu\_irq

The interrupt flow handlers (either predefined or architecture specific) are assigned to specific interrupts by the architecture either during bootup or during device initialization.

#### **Default flow implementations**

#### **Helper functions**

The helper functions call the chip primitives and are used by the default flow implementations. The following helper functions are implemented (simplified excerpt):

#### **Default flow handler implementations**

#### Default Level IRQ flow handler

handle\_level\_irq provides a generic implementation for level-triggered interrupts.

The following control flow is implemented (simplified excerpt):

```
desc->chip->start();
handle_IRQ_event(desc->action);
desc->chip->end();
```

#### Default Edge IRQ flow handler

handle\_edge\_irq provides a generic implementation for edge-triggered interrupts.

The following control flow is implemented (simplified excerpt):

#### **Default simple IRQ flow handler**

handle\_simple\_irq provides a generic implementation for simple interrupts.

Note: The simple flow handler does not call any handler/chip primitives.

The following control flow is implemented (simplified excerpt):

```
handle_IRQ_event(desc->action);
```

#### Default per CPU flow handler

handle\_percpu\_irq provides a generic implementation for per CPU interrupts.

Per CPU interrupts are only available on SMP and the handler provides a simplified version without locking.

The following control flow is implemented (simplified excerpt):

```
desc->chip->start();
handle_IRQ_event(desc->action);
desc->chip->end();
```

#### **Quirks and optimizations**

The generic functions are intended for 'clean' architectures and chips, which have no platform-specific IRQ handling quirks. If an architecture needs to implement quirks on the 'flow' level then it can do so by overriding the highlevel irq-flow handler.

#### **Delayed interrupt disable**

This per interrupt selectable feature, which was introduced by Russell King in the ARM interrupt implementation, does not mask an interrupt at the hardware level when disable\_irq() is called. The interrupt is kept enabled and is masked in the flow handler when an interrupt event happens. This prevents losing edge interrupts on hardware which does not store an edge interrupt event while the interrupt is disabled at the hardware level. When an interrupt arrives while the IRQ\_DISABLED flag is set, then the interrupt is masked at the hardware level and the IRQ\_PENDING bit is set. When the interrupt is re-enabled by enable\_irq() the pending bit is checked and if it is set, the interrupt is resent either via hardware or by a software resend mechanism. (It's necessary to enable CONFIG\_HARDIRQS\_SW\_RESEND when you want to use the delayed interrupt disable feature and your hardware is not capable of retriggering an interrupt.) The delayed interrupt disable can be runtime enabled, per interrupt, by setting the IRQ\_DELAYED\_DISABLE flag in the irq\_desc status field.

#### Chiplevel hardware encapsulation

The chip level hardware descriptor structure irq\_chip contains all the direct chip relevant functions, which can be utilized by the irq flow implementations.

- ack()
- mask\_ack() Optional, recommended for performance

- mask()
- unmask()
- retrigger() Optional
- set\_type() Optional
- set\_wake() Optional

These primitives are strictly intended to mean what they say: ack means ACK, masking means masking of an IRQ line, etc. It is up to the flow handler(s) to use these basic units of lowlevel functionality.

#### Chapter 5. \_\_do\_IRQ entry point

The original implementation \_\_do\_IRQ() is an alternative entry point for all types of interrupts.

This handler turned out to be not suitable for all interrupt hardware and was therefore reimplemented with split functionality for egde/level/simple/percpu interrupts. This is not only a functional optimization. It also shortens code paths for interrupts.

To make use of the split implementation, replace the call to \_\_do\_IRQ by a call to desc->chip->handle\_irq() and associate the appropriate handler function to desc->chip->handle\_irq(). In most cases the generic handler implementations should be sufficient.

### **Chapter 6. Locking on SMP**

The locking of chip registers is up to the architecture that defines the chip primitives. There is a chiplock field that can be used for serialization, but the generic layer does not touch it. The per-irq structure is protected via desc->lock, by the generic layer.

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    struct irq desc — interrupt descriptor
    alloc desc masks — allocate cpumasks for irq_desc
    init copy desc masks — copy cpumasks for irq_desc
    struct irqaction — per interrupt action descriptor
```

This chapter contains the autogenerated documentation of the structures which are used in the generic IRQ layer.

#### Name

struct irq\_chip — hardware interrupt chip descriptor

#### **Synopsis**

```
struct irq chip {
 const char * name;
 unsigned int (* startup) (unsigned int irq);
 void (* shutdown) (unsigned int irq);
 void (* enable) (unsigned int irq);
 void (* disable) (unsigned int irq);
 void (* ack) (unsigned int irq);
 void (* mask) (unsigned int irq);
 void (* mask ack) (unsigned int irg);
 void (* unmask) (unsigned int irg);
 void (* eoi) (unsigned int irq);
 void (* end) (unsigned int irq);
  int (* set_affinity) (unsigned int irq,const struct cpumask *dest);
  int (* retrigger) (unsigned int irq);
  int (* set_type) (unsigned int irq, unsigned int flow_type);
  int (* set wake) (unsigned int irq, unsigned int on);
 void (* bus lock) (unsigned int irq);
 void (* bus sync unlock) (unsigned int irq);
#ifdef CONFIG IRQ RELEASE METHOD
  void (* release) (unsigned int irg, void *dev id);
 const char * typename;
Members
name
     name for /proc/interrupts
```

```
startup
      start up the interrupt (defaults to ->enable if NULL)
shutdown
      shut down the interrupt (defaults to ->disable if NULL)
enable
      enable the interrupt (defaults to chip->unmask if NULL)
disable
      disable the interrupt (defaults to chip->mask if NULL)
ack
      start of a new interrupt
mask
      mask an interrupt source
```

```
mask ack
      ack and mask an interrupt source
unmask
      unmask an interrupt source
eoi
      end of interrupt - chip level
end
     end of interrupt - flow level
set_affinity
      set the CPU affinity on SMP machines
retrigger
      resend an IRQ to the CPU
set_type
      set the flow type (IRQ_TYPE_LEVEL/etc.) of an IRQ
set_wake
      enable/disable power-management wake-on of an IRQ
bus_lock
      function to lock access to slow bus (i2c) chips
bus_sync_unlock
      function to sync and unlock slow bus (i2c) chips
release
      release function solely used by UML
typename
     obsoleted by name, kept as migration helper
```

#### Name

struct irq\_desc — interrupt descriptor

#### **Synopsis**

```
struct irq_desc {
 unsigned int irq;
  struct timer_rand_state * timer_rand_state;
 unsigned int * kstat_irqs;
#ifdef CONFIG_INTR_REMAP
 struct irq 2_iommu * irq_2_iommu;
 irq flow handler t handle irq;
 struct irq chip * chip;
 struct msi desc * msi desc;
 void * handler_data;
 void * chip_data;
 struct irgaction * action;
 unsigned int status;
 unsigned int depth;
 unsigned int wake depth;
 unsigned int irq count;
 unsigned long last_unhandled;
 unsigned int irqs unhandled;
 spinlock t lock;
#ifdef CONFIG SMP
 cpumask_var_t affinity;
 unsigned int node;
#ifdef CONFIG_GENERIC_PENDING_IRQ
  cpumask_var_t pending_mask;
#endif
#endif
 atomic t threads active;
 wait queue head t wait for threads;
#ifdef CONFIG PROC FS
  struct proc dir entry * dir;
#endif
 const char * name;
```

#### **Members**

```
interrupt number for this descriptor

timer_rand_state

pointer to timer rand state struct

kstat_irqs

irq stats per cpu

irq_2_iommu

iommu with this irq
```

```
handle_irq
      highlevel irq-events handler [if NULL, __do_IRQ]
chip
      low level interrupt hardware access
msi_desc
      MSI descriptor
handler_data
      per-IRQ data for the irq_chip methods
chip_data
      platform-specific per-chip private data for the chip methods, to allow shared chip implementations
action
      the irq action chain
status
      status information
depth
      disable-depth, for nested irg disable calls
wake_depth
      enable depth, for multiple set_irq_wake callers
irq_count
      stats field to detect stalled irqs
last_unhandled
      aging timer for unhandled count
irqs_unhandled
      stats field for spurious unhandled interrupts
lock
      locking for SMP
affinity
```

```
IRQ affinity on SMP
```

node

node index useful for balancing

pending\_mask

pending rebalanced interrupts

threads\_active

number of irqaction threads currently running

wait\_for\_threads

wait queue for sync\_irq to wait for threaded handlers

dir

/proc/irq/ procfs entry

name

flow handler name for /proc/interrupts output

#### Name

alloc\_desc\_masks — allocate cpumasks for irq\_desc

# **Synopsis**

# **Arguments**

desc

pointer to irq\_desc struct

node

node which will be handling the cpumasks

boot

true if need bootmem

# **Description**

Allocates affinity and pending\_mask cpumask if required. Returns true if successful (or not required).

#### Name

```
init_copy_desc_masks — copy cpumasks for irq_desc
```

# **Synopsis**

#### **Arguments**

```
pointer to old irq_desc struct

new_desc

pointer to new irq_desc struct
```

### **Description**

Insures affinity and pending\_masks are copied to new irq\_desc. If !CONFIG\_CPUMASKS\_OFFSTACK the cpumasks are embedded in the irq\_desc struct so the copy is redundant.

#### Name

struct irqaction — per interrupt action descriptor

# **Synopsis**

```
struct irqaction {
  irq_handler_t handler;
  unsigned long flags;
  const char * name;
  void * dev_id;
```

```
struct irqaction * next;
int irq;
struct proc_dir_entry * dir;
irq_handler_t thread_fn;
struct task_struct * thread;
unsigned long thread_flags;
};
```

#### **Members**

```
handler
      interrupt handler function
flags
      flags (see IRQF_* above)
name
      name of the device
dev_id
      cookie to identify the device
next
      pointer to the next irqaction for shared interrupts
irq
      interrupt number
dir
      pointer to the proc/irq/NN/name entry
thread_fn
      interupt handler function for threaded interrupts
thread
      thread pointer for threaded interrupts
thread_flags
      flags related to thread
```

# **Chapter 8. Public Functions Provided**

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disable irq nosync — disable an irq without waiting

disable irq — disable an irq and wait for completion

enable irq — enable handling of an irq

set irq wake — control irq power management wakeup

setup irq — setup an interrupt

remove irq — free an interrupt

free irq — free an interrupt allocated with request_irq

request threaded irq — allocate an interrupt line

set irq chip — set the irq chip for an irq

set irq type — set the irq trigger type for an irq

set irq data — set irq type data for an irq

set irq chip data — set irq chip data for an irq

set irq nested thread — Set/Reset the IRQ_NESTED_THREAD flag of an irq

handle level irq — Level type irq handler
```

This chapter contains the autogenerated documentation of the kernel API functions which are exported.

#### Name

synchronize\_irq — wait for pending IRQ handlers (on other CPUs)

# **Synopsis**

```
void synchronize_irq (irq);
unsigned int irq;
```

#### **Arguments**

irq

interrupt number to wait for

# **Description**

This function waits for any pending IRQ handlers for this interrupt to complete before returning. If you use this function while holding a resource the IRQ handler may need you will deadlock.

This function may be called - with care - from IRQ context.

#### Name

disable\_irq\_nosync — disable an irq without waiting

#### **Synopsis**

```
void disable_irq_nosync (irq);
unsigned int irq;
```

#### **Arguments**

irq

Interrupt to disable

# **Description**

Disable the selected interrupt line. Disables and Enables are nested. Unlike disable\_irq, this function does not ensure existing instances of the IRQ handler have completed before returning.

This function may be called from IRQ context.

#### Name

disable\_irq — disable an irq and wait for completion

# **Synopsis**

```
void disable_irq (irq);
unsigned int irq;
```

#### **Arguments**

irq

Interrupt to disable

# **Description**

Disable the selected interrupt line. Enables and Disables are nested. This function waits for any pending IRQ handlers for this interrupt to complete before returning. If you use this function while holding a resource the IRQ handler may need you will deadlock.

This function may be called - with care - from IRQ context.

#### Name

enable\_irq — enable handling of an irq

# **Synopsis**

```
void enable_irq (irq);
unsigned int irq;
```

#### **Arguments**

irq

Interrupt to enable

# **Description**

Undoes the effect of one call to disable\_irq. If this matches the last disable, processing of interrupts on this IRQ line is re-enabled.

This function may be called from IRQ context only when desc->chip->bus\_lock and desc->chip->bus\_sync\_unlock are NULL!

#### Name

set\_irq\_wake — control irq power management wakeup

#### **Synopsis**

# **Arguments**

```
irq interrupt to control
```

enable/disable power management wakeup

# **Description**

Enable/disable power management wakeup mode, which is disabled by default. Enables and disables must match, just as they match for non-wakeup mode support.

Wakeup mode lets this IRQ wake the system from sleep states like "suspend to RAM".

#### Name

setup\_irq — setup an interrupt

# **Synopsis**

# **Arguments**

```
irq
    Interrupt line to setup
act
```

irqaction for the interrupt

# **Description**

Used to statically setup interrupts in the early boot process.

### Name

```
remove_irq — free an interrupt
```

# **Synopsis**

### **Arguments**

```
irq
```

Interrupt line to free

act

irqaction for the interrupt

### **Description**

Used to remove interrupts statically setup by the early boot process.

#### Name

free\_irq — free an interrupt allocated with request\_irq

# **Synopsis**

# **Arguments**

```
irq
```

Interrupt line to free

dev\_id

Device identity to free

### **Description**

Remove an interrupt handler. The handler is removed and if the interrupt line is no longer in use by any driver it is disabled. On a shared IRQ the caller must ensure the interrupt is disabled on the card it drives before calling this function. The function does not return until any executing interrupts for this IRQ have completed.

This function must not be called from interrupt context.

#### Name

request\_threaded\_irq — allocate an interrupt line

#### **Synopsis**

#### **Arguments**

irq

Interrupt line to allocate

handler

Function to be called when the IRQ occurs. Primary handler for threaded interrupts If NULL and thread\_fn != NULL the default primary handler is installed

thread fn

Function called from the irq handler thread If NULL, no irq thread is created

irqflags

Interrupt type flags

devname

An ascii name for the claiming device

dev\_id

A cookie passed back to the handler function

### **Description**

This call allocates interrupt resources and enables the interrupt line and IRQ handling. From the point this call is made your handler function may be invoked. Since your handler function must clear any interrupt the board raises, you must take care both to initialise your hardware and to set up the interrupt handler in the right order.

If you want to set up a threaded irq handler for your device then you need to supply handler and

thread\_fn. handler ist still called in hard interrupt context and has to check whether the interrupt originates from the device. If yes it needs to disable the interrupt on the device and return IRQ\_WAKE\_THREAD which will wake up the handler thread and run thread\_fn. This split handler design is necessary to support shared interrupts.

Dev\_id must be globally unique. Normally the address of the device data structure is used as the cookie. Since the handler receives this value it makes sense to use it.

If your interrupt is shared you must pass a non NULL dev\_id as this is required when freeing the interrupt.

### **Flags**

IRQF\_SHARED Interrupt is shared IRQF\_DISABLED Disable local interrupts while processing IRQF\_SAMPLE\_RANDOM The interrupt can be used for entropy IRQF\_TRIGGER\_\* Specify active edge(s) or level

#### Name

set\_irq\_chip — set the irq chip for an irq

# **Synopsis**

#### **Arguments**

```
irq
irq number

chip

pointer to irq chip description structure
```

#### Name

set\_irq\_type — set the irq trigger type for an irq

# **Synopsis**

```
int set_irq_type (irq,
```

```
type);
unsigned int irq;
unsigned int type;
```

#### **Arguments**

```
irq number
type
```

IRQ\_TYPE\_{LEVEL,EDGE}\_\* value - see include/linux/irq.h

#### Name

set\_irq\_data — set irq type data for an irq

# **Synopsis**

#### **Arguments**

irq

Interrupt number

data

Pointer to interrupt specific data

# **Description**

Set the hardware irq controller data for an irq

#### Name

set\_irq\_chip\_data — set irq chip data for an irq

# **Synopsis**

#### **Arguments**

irq

Interrupt number

data

Pointer to chip specific data

#### **Description**

Set the hardware irq chip data for an irq

#### Name

set\_irq\_nested\_thread — Set/Reset the IRQ\_NESTED\_THREAD flag of an irq

# **Synopsis**

# **Arguments**

```
irq
```

Interrupt number

nest

0 to clear / 1 to set the IRQ\_NESTED\_THREAD flag

# **Description**

The IRQ\_NESTED\_THREAD flag indicates that on request\_threaded\_irq no separate interrupt thread should be created for the irq as the handler are called nested in the context of a demultiplexing interrupt

handler thread.

#### Name

handle\_level\_irq — Level type irq handler

### **Synopsis**

#### **Arguments**

```
irq the interrupt number desc
```

the interrupt description structure for this irq

# **Description**

Level type interrupts are active as long as the hardware line has the active level. This may require to mask the interrupt and unmask it after the associated handler has acknowledged the device, so the interrupt line is back to inactive.

# **Chapter 9. Internal Functions Provided**

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    handle simple irq — Simple and software-decoded IRQs.
    handle fasteoi irq — irq handler for transparent controllers
    handle edge irq — edge type IRQ handler
    handle percpu irq — Per CPU local irq handler
```

This chapter contains the autogenerated documentation of the internal functions.

#### Name

handle\_bad\_irq — handle spurious and unhandled irqs

# **Synopsis**

#### **Arguments**

```
trqthe interrupt numberdescdescription of the interrupt
```

# **Description**

Handles spurious and unhandled IRQ's. It also prints a debugmessage.

#### Name

handle\_IRQ\_event — irq action chain handler

# **Synopsis**

### **Arguments**

```
the interrupt number
action
the interrupt action chain for this irq
```

# **Description**

Handles the action chain of an irq event

#### Name

\_\_do\_IRQ — original all in one highlevel IRQ handler

# **Synopsis**

```
unsigned int __do_IRQ (irq);
unsigned int irq;
```

#### **Arguments**

irq

the interrupt number

# **Description**

\_\_do\_IRQ handles all normal device IRQ's (the special SMP cross-CPU interrupts have their own specific handlers).

This is the original x86 implementation which is used for every interrupt type.

#### Name

dynamic\_irq\_init — initialize a dynamically allocated irq

# **Synopsis**

```
void dynamic_irq_init (irq);
unsigned int irq;
```

# **Arguments**

irq

irq number to initialize

#### Name

dynamic\_irq\_cleanup — cleanup a dynamically allocated irq

# **Synopsis**

```
void dynamic_irq_cleanup (irq);
unsigned int irq;
```

# **Arguments**

irq

irq number to initialize

#### Name

set\_irq\_msi — set irq type data for an irq

# **Synopsis**

# **Arguments**

irq

Interrupt number

entry

Pointer to MSI descriptor data

# **Description**

Set the hardware irq controller data for an irq

#### Name

handle\_simple\_irq — Simple and software-decoded IRQs.

### **Synopsis**

### **Arguments**

irq

the interrupt number

desc

the interrupt description structure for this irq

# **Description**

Simple interrupts are either sent from a demultiplexing interrupt handler or come from hardware, where no interrupt hardware control is necessary.

#### **Note**

The caller is expected to handle the ack, clear, mask and unmask issues if necessary.

#### Name

handle\_fasteoi\_irq — irq handler for transparent controllers

# **Synopsis**

#### **Arguments**

irq

the interrupt number

desc

the interrupt description structure for this irq

#### Only a single callback will be issued to the chip

an ->eoi call when the interrupt has been serviced. This enables support for modern forms of interrupt handlers, which handle the flow details in hardware, transparently.

#### Name

handle\_edge\_irq — edge type IRQ handler

# **Synopsis**

#### **Arguments**

irq

the interrupt number

desc

the interrupt description structure for this irq

#### **Description**

Interrupt occures on the falling and/or rising edge of a hardware signal. The occurence is latched into the irq controller hardware and must be acked in order to be reenabled. After the ack another interrupt can happen on the same source even before the first one is handled by the assosiacted event handler. If this happens it might be necessary to disable (mask) the interrupt depending on the controller hardware. This requires to reenable the interrupt inside of the loop which handles the interrupts which have arrived while the handler was running. If all pending interrupts are handled, the loop is left.

#### Name

handle\_percpu\_irq — Per CPU local irq handler

# **Synopsis**

# **Arguments**

irq

the interrupt number

desc

the interrupt description structure for this irq

# **Description**

Per CPU interrupts on SMP machines without locking requirements

# Chapter 10. Credits

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