

RELATÓRIO- PROJETO 6

Questão 1

Arquivo exp6ex1.vhd:

```
2  -- Circuito: flip-flop JK
3  --  gatilhado pela borda de subida
4  --      PR, CLR - Entradas assíncronas
5  --      CLK - Clock
6  --      JK - Entrada síncrona
7  --      Q - Saída
8  -- *****
9  -----
10 library IEEE;
11 use IEEE.std_logic_1164.all;
12 -----
13 entity EXP6EX1 is port (
14     PR, CLR, CLK :in std_logic;
15     JK :in std_logic_vector(1 DOWNTO 0);
16     Q :out std_logic);
17 end EXP6EX1;
18 -----
19
20 architecture flipflopJK of EXP6EX1 is
21 begin
22     process(PR, CLR, CLK)
23         variable Qbuf: std_logic;
24     begin
25         if (PR = '1') then
26             Qbuf := '1';
27         elsif (PR = '0' and CLR = '1') then
28             Qbuf := '0';
29         elsif rising_edge(CLK) then
30             case JK is
31                 when "00" => Qbuf := Qbuf;
32                 when "01" => Qbuf := '0';
33                 when "10" => Qbuf := '1';
34                 when "11" => Qbuf := not(Qbuf);
35                 when others => Qbuf := Qbuf;
36             end case;
37         else
38             Qbuf := Qbuf;
39         end if;
40         Q <= Qbuf;
41     end process;
42 end flipflopJK;
```

Arquivo tb_exp6ex1.vhd:

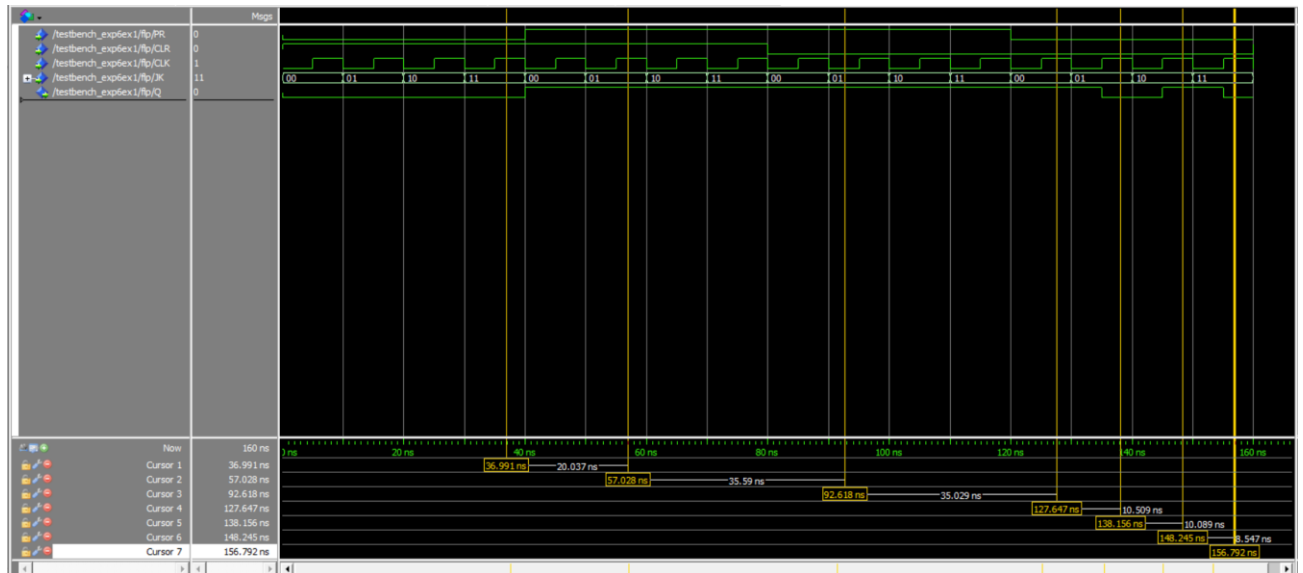
```
1  -- *****  
2  -- Testbench para simulacao Funcional do  
3  -- Circuito: flip-flop JK  
4  -- gatilhado pela borda de subida  
5  -- PR, CLR - Entradas assíncronas  
6  -- CLK - Clock  
7  -- JK - Entrada síncrona  
8  -- Q - Saída  
9  -- *****  
10 -----  
11 library IEEE;  
12 use IEEE.std_logic_1164.all;  
13 use std.textio.all;  
14 use ieee.numeric_std.all;  
15 -----  
16  
17 entity testbench_exp6ex1 IS END;  
18  
19 architecture tb_exp6ex1 of testbench_exp6ex1 is  
20  
21     component EXP6EX1  
22  
23     port (  
24         PR, CLR, CLK :in std_logic;  
25         JK :in std_logic_vector(1 DOWNTO 0);  
26         Q :out std_logic;  
27     end component;  
28 -----  
29     signal pr, clr: std_logic;  
30     signal clk : std_logic := '0';  
31     signal jk : std_logic_vector(1 DOWNTO 0);  
32  
33     Begin  
34  
35     flp: EXP6EX1 PORT MAP (PR => pr, CLR => clr, CLK => clk, JK => jk, Q => open);  
36     clk <= not clk after 5 ns;  
37  
38  
39     estimulo: PROCESS  
40     begin  
41         pr <= '0'; clr <= '1';  
42         for i in 0 to 3 loop  
43             jk <= std_logic_vector(to_unsigned(i, 2));  
44             wait for 10 ns;  
45         end loop;  
46  
47         pr <= '1';  
48         for i in 0 to 3 loop  
49             jk <= std_logic_vector(to_unsigned(i, 2));  
50             wait for 10 ns;  
51         end loop;  
52  
53         clr <= '0';  
54         for i in 0 to 3 loop  
55             jk <= std_logic_vector(to_unsigned(i, 2));  
56             wait for 10 ns;  
57         end loop;  
58  
59         pr <= '0';  
60         for i in 0 to 3 loop  
61             jk <= std_logic_vector(to_unsigned(i, 2));  
62             wait for 10 ns;  
63         end loop;  
64     end PROCESS estimulo;  
65  
66 end tb_exp6ex1;  
67
```

Compilação:

Name	Status	Type	On/Off	Modified
exp6ex1.vhd	✓	VHDL	0	04/08/2021 12:07:41 pm
tb_exp6ex1.vhd	✓	VHDL	1	04/08/2021 12:08:47 pm

```
Project x sim x  
Transcript  
# Compile of exp6ex1.vhd was successful.  
# Compile of tb_exp6ex1.vhd was successful.  
# 2 compiles, 0 failed with no errors.
```

Simulação:



	PR	CLR	CLK	J	K	Q
Cursor 1	0	1	SUBIDA	1	1	0
Cursor 2	1	1	SUBIDA	0	1	1
Cursor 3	1	0	DESCIDA	0	1	1
Cursor 4	0	0	SUBIDA	0	0	1
Cursor 5	0	0	SUBIDA	0	1	0
Cursor 6	0	0	SUBIDA	1	0	1
Cursor 7	0	0	SUBIDA	1	1	0

Questão 2

Arquivo exp6ex1.vhd:

```
1  -- *****
2  -- Circuito: Registrador de deslocamento
3  -- bidirecional de 4 bits
4  --      RST, LOAD - Entradas assíncronas
5  --      CLK - Clock
6  --      D, DIR, L e R - Entradas síncronas
7  --      Q - Saída
8  -- *****
9  -----
10 library IEEE;
11 use IEEE.STD_LOGIC_1164.ALL;
12 -----
13 entity EXP6EX2 is port (
14     CLK, RST, LOAD, DIR, L, R : in std_logic;
15     D : in std_logic_vector(3 DOWNTO 0);
16     Q : out std_logic_vector(3 DOWNTO 0));
17 end EXP6EX2;
18 -----
19 architecture registradorDeslocamento of EXP6EX2 is
20     signal currentState, nextState : std_logic_vector(3 DOWNTO 0);
21
22 begin
23     sync_proc: process(CLK)
24     begin
25         if rising_edge(CLK) then
26             currentState <= nextState;
27         end if;
28     end process sync_proc;
29
30     comb_proc: process(currentState, RST, LOAD, DIR, D, L, R)
31     begin
32         if (RST = '1') then
33             nextState <= "0000";
34         elsif (LOAD = '1') then
35             nextState <= D;
36         elsif (DIR = '0') then
37             nextState <= currentState(2) & currentState(1) & currentState(0) & L;
38         elsif (DIR = '1') then
39             nextState <= R & currentState(3) & currentState(2) & currentState(1);
40         else nextState <= currentState;
41         end if;
42     end process;
43     Q <= currentState;
44 end registradorDeslocamento;
```

Arquivo tb_exp6ex1.vhd:

```
1  -- *****
2  -- Testbench para simulacao Funcional do
3  -- Circuito: Registrador de deslocamento
4  -- bidirecional de 4 bits
5  --         RST, LOAD - Entradas assíncronas
6  --         CLK - Clock
7  --         D, DIR, L e R - Entradas síncronas
8  --         Q - Saída
9  -- *****
10 -----
11 library IEEE;
12 use IEEE.std_logic_1164.all;
13 use std.textio.all;
14 use ieee.numeric_std.all;
15 -----
16 |
17 entity testbench_exp6ex2 IS END;
18
19 architecture tb_exp6ex2 of testbench_exp6ex2 is
20
21     component EXP6EX2
22
23     port (
24         CLK, RST, LOAD, DIR, L, R : in std_logic;
25         D : in std_logic_vector(3 DOWNTO 0);
26         Q : out std_logic_vector(3 DOWNTO 0));
27     end component;
28 -----
29     signal load, rst : std_logic;
30     signal clk : std_logic := '0';
31     signal d : std_logic_vector(3 DOWNTO 0);
32     signal DIR_L_R : std_logic_vector(2 DOWNTO 0);
33
34 Begin
35
36 rgd: EXP6EX2 PORT MAP (LOAD => load, RST => rst, DIR => DIR_L_R(2), L => DIR_L_R(1), R => DIR_L_R(0), CLK => clk, D => d, Q => open);
37 clk <= not clk after 5 ns;
38
39 estimulo: PROCESS
40 begin
41     -- Código com D fixado em um valor qualquer
42
43
44     d <= "1010";
45
46     rst <= '1'; load <= '0';
47     for j in 0 to 7 loop
48         DIR_L_R <= std_logic_vector(to_unsigned(j, 3));
49         wait for 10 ns;
50     end loop;
51
52     load <= '1';
53     for j in 0 to 7 loop
54         DIR_L_R <= std_logic_vector(to_unsigned(j, 3));
55         wait for 10 ns;
56     end loop;
57
58     rst <= '0';
59     for j in 0 to 7 loop
60         DIR_L_R <= std_logic_vector(to_unsigned(j, 3));
61         wait for 10 ns;
62     end loop;
63
64     load <= '0';
65     for j in 0 to 7 loop
66         DIR_L_R <= std_logic_vector(to_unsigned(j, 3));
67         wait for 10 ns;
68     end loop;
69 end PROCESS estimulo;
70 end tb_exp6ex2;
```

Compilação:

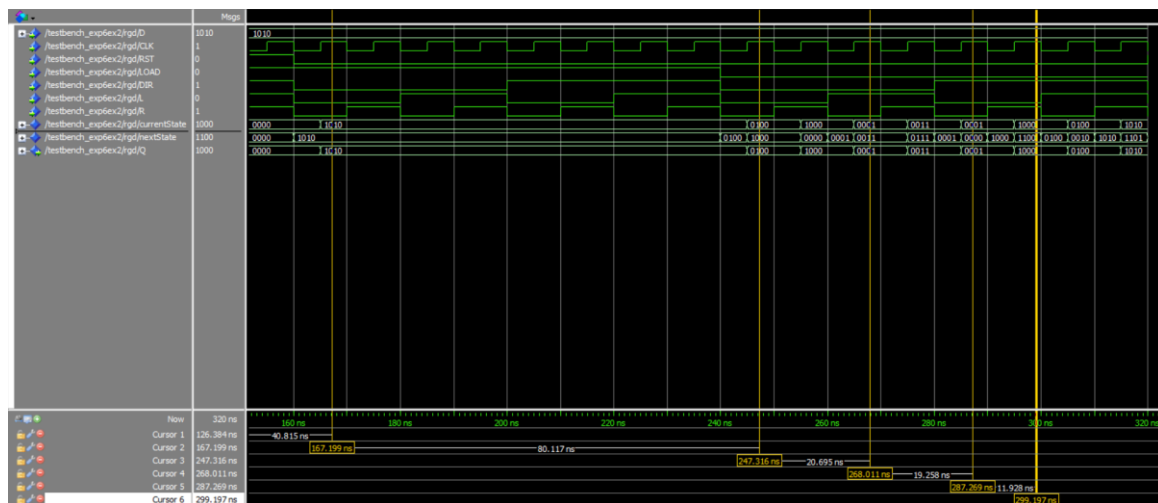
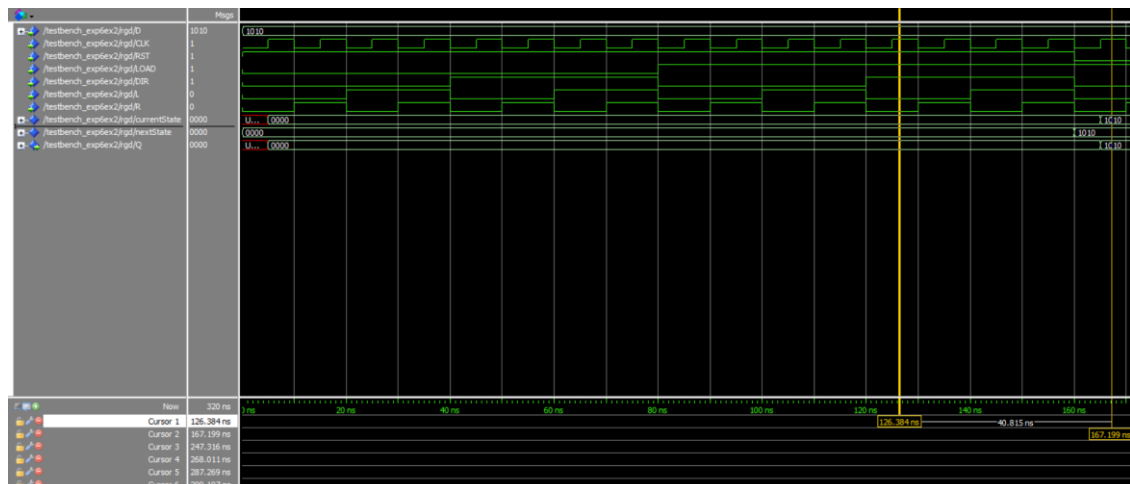
```

Users/david/Documents/UnB/2020.2/LSD/projeto 6/RegistradorDeslocamento :
▼ Name      Status Type On Δ Modified
exp6ex2.vhd  ✓      VHDL  0   04/08/2021 06:16:28 pm
tb_exp6ex2.vhd ✓      VHDL  1   04/08/2021 06:16:29 pm

Library × Project × sim ×

Transcript
# Compile of exp6ex2.vhd was successful.
# Compile of tb_exp6ex2.vhd was successful.
# 2 compiles, 0 failed with no errors.
  
```

Simulação (Feita com D fixo em 1010):



	CLK	RST	LOAD	DIR	L	R	Q	nextState
Cursor 1	SUBIDA	1	1	1	0	0	0000	0000
Cursor 2	SUBIDA	0	1	0	0	0	1010	1010
Cursor 3	SUBIDA	0	0	0	0	0	0100	1000
Cursor 4	SUBIDA	0	0	0	1	0	0001	0011
Cursor 5	SUBIDA	0	0	1	0	0	0001	0000
Cursor 6	SUBIDA	0	0	1	0	1	1000	1100