RELATÓRIO- PROJETO 5

Questão 1

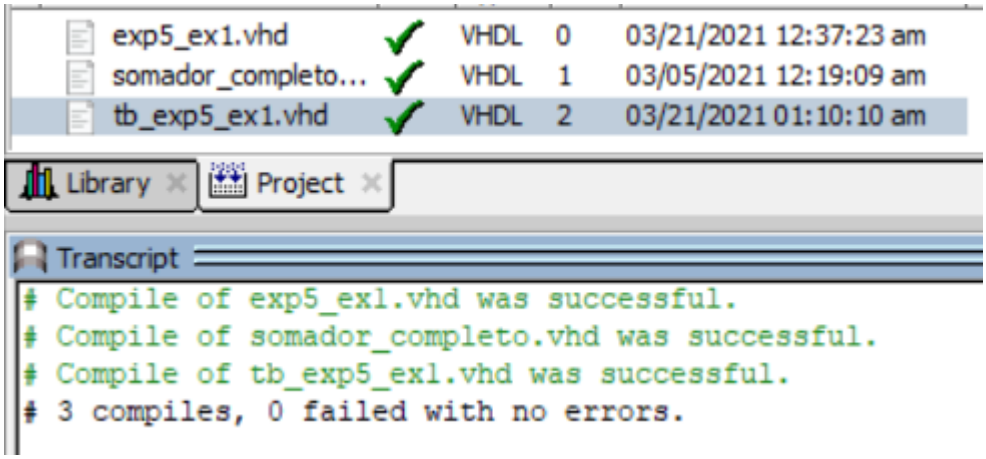
Arquivo exp5_ex1.vhd:

```
-- ***************************************
--    Circuito: Somador de 4 palavras
--    usando 4 somadores completos
--          A,B   Vetores de Entrada
--            S   Vetor de Saída
-- ***************************************
----------------------------------------------------
library IEEE;
use IEEE.std_logic_1164.all;
----------------------------------------------------
entity EXP5_EX1 is port (
    A, B :in  std_logic_vector(3 DOWNTO 0);
    S    :out std_logic_vector(4 DOWNTO 0));
end EXP5_EX1;
----------------------------------------------------

architecture ex1 of EXP5_EX1 is

    component SOMADOR_COMPLETO is
    port (
    A    :in std_logic;
    B    :in std_logic;
    Cin  :in std_logic;
    S    :out std_logic;
    Cout :out std_logic );
end component;

signal Cout_aux : std_logic_vector(2 DOWNTO 0);

begin
    som1: SOMADOR_COMPLETO PORT MAP (Cin =>         '0', A => A(0), B => B(0), S => S(0), Cout => Cout_aux(0));
    som2: SOMADOR_COMPLETO PORT MAP (Cin => Cout_aux(0), A => A(1), B => B(1), S => S(1), Cout => Cout_aux(1));
    som3: SOMADOR_COMPLETO PORT MAP (Cin => Cout_aux(1), A => A(2), B => B(2), S => S(2), Cout => Cout_aux(2));
    som4: SOMADOR_COMPLETO PORT MAP (Cin => Cout_aux(2), A => A(3), B => B(3), S => S(3), Cout => S(4));
end ex1;
```

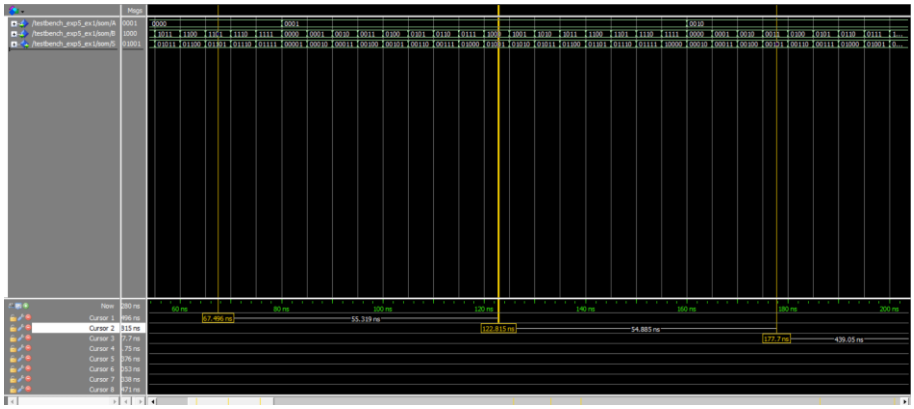
Arquivo tb_exp5_ex1.vhd:

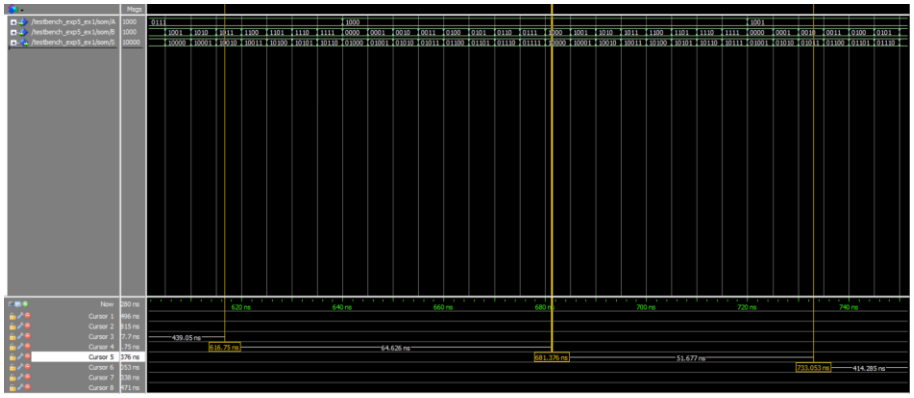
```
9   LIBRARY ieee;
10  USE ieee.std_logic_1164.ALL;
11  USE std.textio.ALL;
12  USE ieee.numeric_std.ALL;
13  ----------------------------------------------------------
14
15  ENTITY testbench_exp5_ex1 IS END;
16
17  ARCHITECTURE tb_exp5_ex1 OF testbench_exp5_ex1 IS
18
19  component EXP5_EX1
20
21  port (
22      A, B :in  std_logic_vector(3 DOWNTO 0);
23      S    :out std_logic_vector(4 DOWNTO 0));
24  end component;
25  ----------------------------------------------------------
26
27  signal aa, bb : std_logic_vector (3 DOWNTO 0);
28
29  Begin
30
31  som: EXP5_EX1 PORT MAP (A => aa, B => bb, S => open);
32
33  estimulo: PROCESS
34
35  begin
36      for i in 0 to 15 loop
37          aa <= std_logic_vector(to_unsigned(i, 4));
38          for j in 0 to 15 loop
39              bb <= std_logic_vector(to_unsigned(j, 4));
40              wait for 5 ns;
41          end loop;
42      end loop;
43  end PROCESS estimulo;
44
45  end tb_exp5_ex1;
```

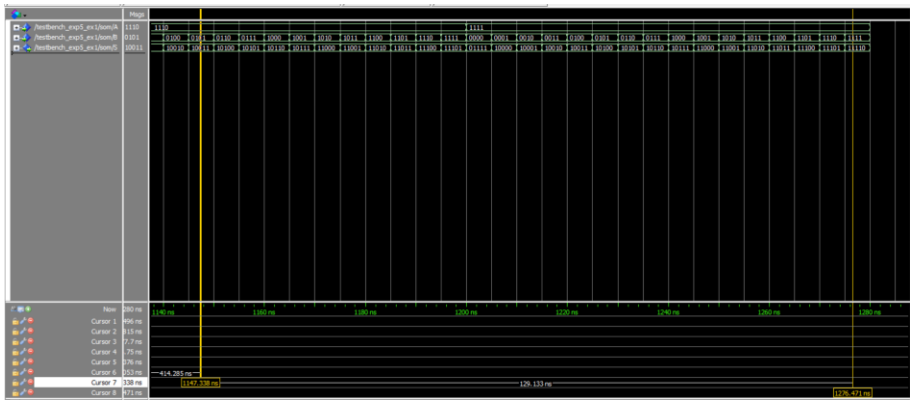
Compilação:



Simulação:







	Entrada A	Entrada B	Saída S
Cursor 1	0000	1101	01101
Cursor 2	0001	1000	01001
Cursor 3	0010	0011	00101
Cursor 4	0111	1011	10010
Cursor 5	1000	1000	10000
Cursor 6	1001	0010	01011
Cursor 7	1110	0101	10011
Cursor 8	1111	1111	11110

Questão 2

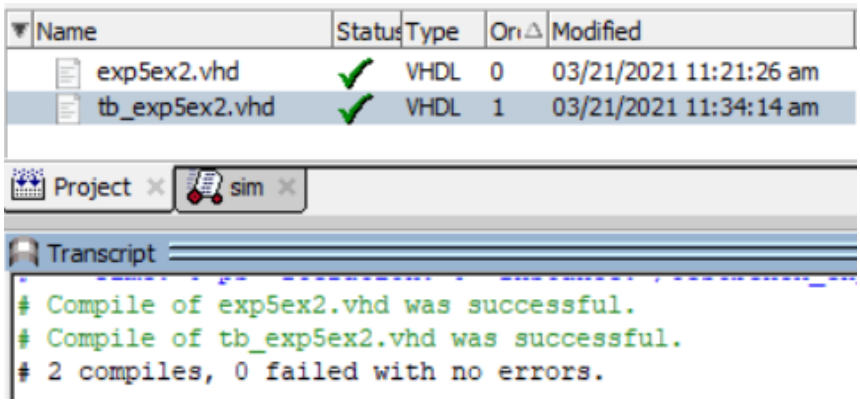
Arquivo exp5ex2.vhd:

```
1   -- ************************************************
2   --  Circuito: Somador de 4 palavras usando o
3   --  operador '+' da biblioteca std_logic_arith
4   --          A,B   Vetores de Entrada
5   --            S   Vetor de Saída
6   -- ************************************************
7   ------------------------------------------------------
8   library IEEE;
9   use IEEE.std_logic_1164.all;
10  use IEEE.std_logic_arith.all;
11  ------------------------------------------------------
12  entity EXP5EX2 is port (
13      A, B :in  std_logic_vector(3 DOWNTO 0);
14      S    :out std_logic_vector(4 DOWNTO 0));
15  end EXP5EX2;
16  ------------------------------------------------------
17
18  architecture ex1 of EXP5EX2 is
19
20  begin
21      S <= ('0' & unsigned(A)) + ('0' &  unsigned(B));
22  end ex1;
23
```

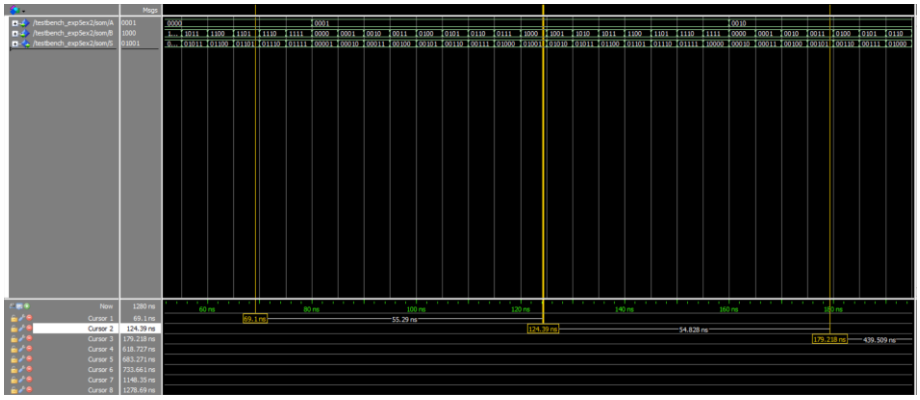
Arquivo tb_exp5ex2.vhd:

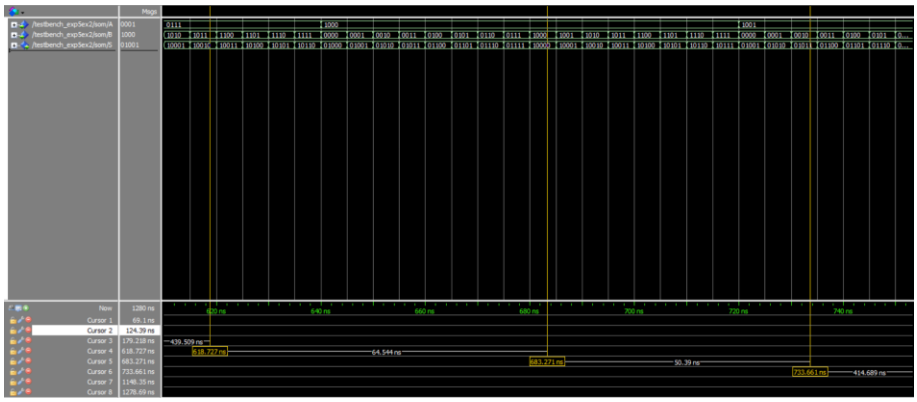
```
8   ----------------------------------------------------------
9   LIBRARY ieee;
10  USE ieee.std_logic_1164.ALL;
11  USE std.textio.ALL;
12  USE ieee.numeric_std.ALL;
13  ----------------------------------------------------------
14
15  ENTITY testbench_exp5ex2 IS END;
16
17  ARCHITECTURE tb_exp5ex2 OF testbench_exp5ex2 IS
18
19  component EXP5EX2
20
21  port (
22      A, B :in  std_logic_vector(3 DOWNTO 0);
23      S    :out std_logic_vector(4 DOWNTO 0));
24  end component;
25  ----------------------------------------------------------
26
27  signal aa, bb : std_logic_vector (3 DOWNTO 0);
28
29  Begin
30
31  som: EXP5EX2 PORT MAP (A => aa, B => bb, S => open);
32
33  estimulo: PROCESS
34
35  begin
36      for i in 0 to 15 loop
37          aa <= std_logic_vector(to_unsigned(i, 4));
38          for j in 0 to 15 loop
39              bb <= std_logic_vector(to_unsigned(j, 4));
40              wait for 5 ns;
41          end loop;
42      end loop;
43  end PROCESS estimulo;
```

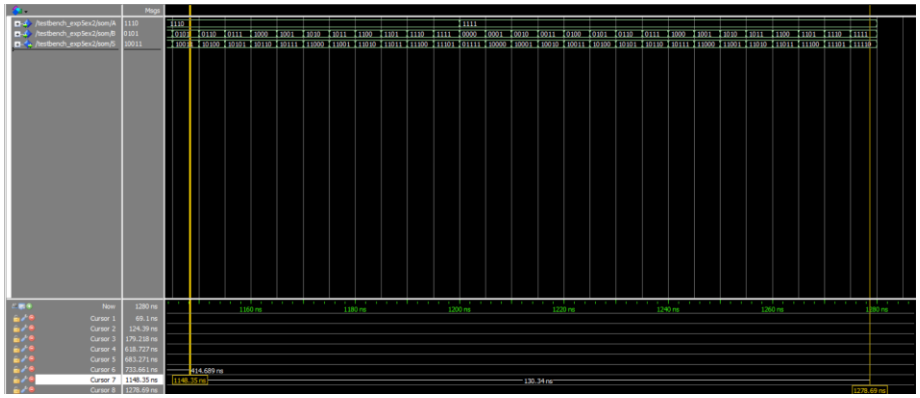
Compilação:



Simulação:







	Entrada A	Entrada B	Saída S
Cursor 1	0000	1101	01101
Cursor 2	0001	1000	01001
Cursor 3	0010	0011	00101
Cursor 4	0111	1011	10010
Cursor 5	1000	1000	10000
Cursor 6	1001	0010	01011
Cursor 7	1110	0101	10011
Cursor 8	1111	1111	11110

Questão 3

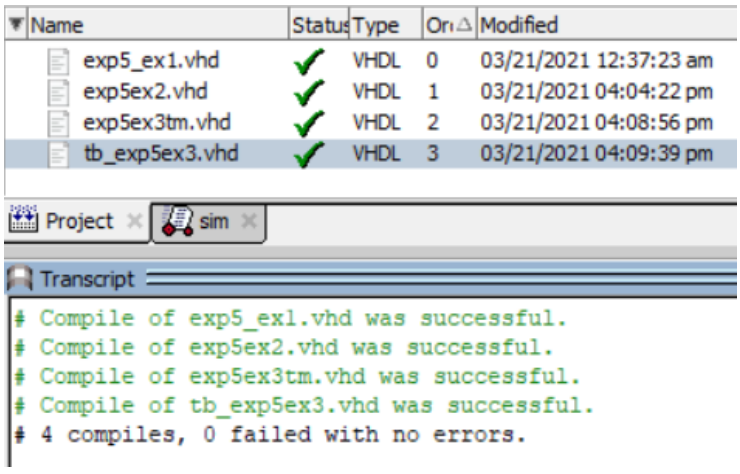
Arquivo exp5ex3tm.vhd:

```
-- ****************************************************
--  Top Module para comparar as saídas dos
--  Circuitos:
--  1. Somador de 4 palavras usando 4
--  somadores completos(Device Under Test);
--  2. Somador de 4 palavras usando o operador
--  '+' da biblioteca std_logic_arith (Golden Model)
--
--
--          A,B   Vetores de Entrada
--          S_dut Saída do circuito 1
--          S_gm  Saída do circuito 2
-- ****************************************************
-------------------------------------------------------
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
-------------------------------------------------------
entity EXP5EX3TM is
end EXP5EX3TM;
-------------------------------------------------------

architecture ex3 of EXP5EX3TM is

    component EXP5_EX1 is port (
    A, B :in  std_logic_vector(3 DOWNTO 0);
    S    :out std_logic_vector(4 DOWNTO 0));
    end component;

    component EXP5EX2 is port (
        A, B :in  std_logic_vector(3 DOWNTO 0);
        S    :out std_logic_vector(4 DOWNTO 0));
    end component;

    component testbench_exp5ex3 is port (
        S_dut, S_gm :in  STD_LOGIC_VECTOR(4 DOWNTO 0);
        A, B        :out STD_LOGIC_VECTOR(3 DOWNTO 0));
    end component;

    signal A, B        : STD_LOGIC_VECTOR(3 DOWNTO 0);
    signal S_dut, S_gm : STD_LOGIC_VECTOR(4 DOWNTO 0);

    begin
        U0: EXP5_EX1 PORT MAP(A, B, S_dut);
        U1: EXP5EX2  PORT MAP(A, B, S_gm);
        U2: TESTBENCH_EXP5EX3 PORT MAP(S_dut, S_gm, A, B);
end ex3;
```

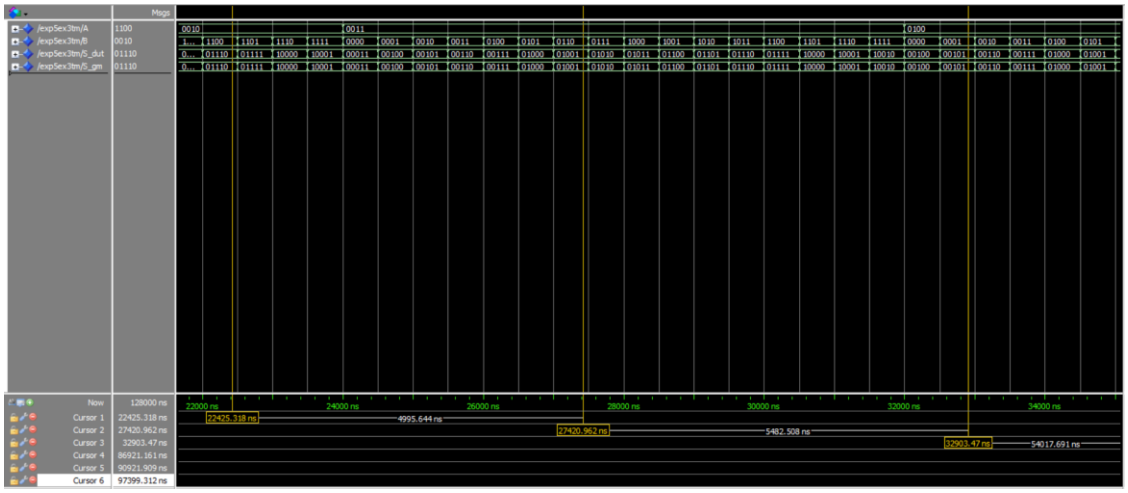
Arquivo tb_exp5ex3.vhd:

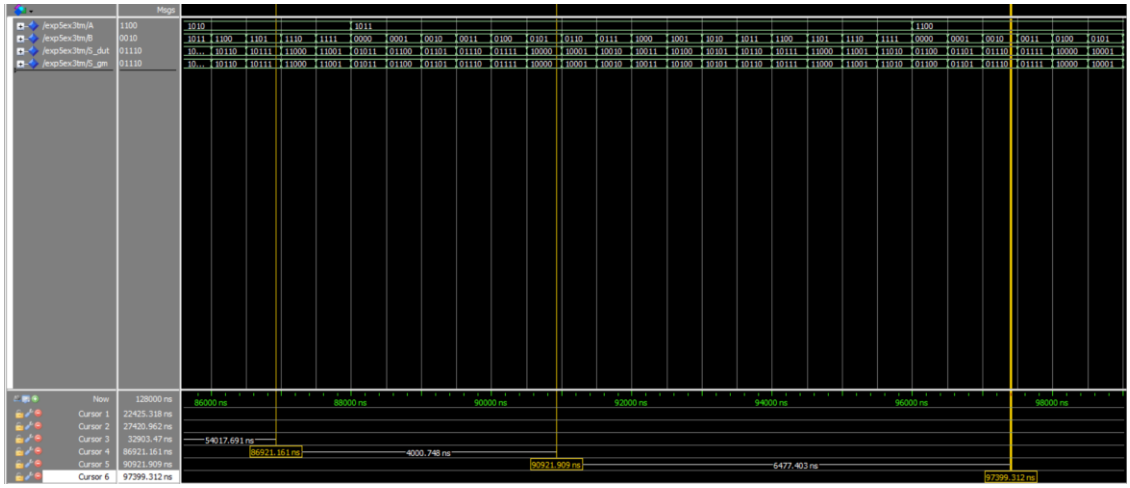
```
14  ----------------------------------------------------------
15  LIBRARY ieee;
16  USE ieee.std_logic_1164.ALL;
17  USE std.textio.ALL;
18  USE ieee.numeric_std.ALL;
19  ----------------------------------------------------------
20
21  ENTITY testbench_exp5ex3 IS
22  port (S_dut, S_gm: in  STD_LOGIC_VECTOR(4 DOWNTO 0);
23        A, B       : out STD_LOGIC_VECTOR(3 DOWNTO 0));
24  END testbench_exp5ex3;
25
26
27  ----------------------------------------------------------
28  ARCHITECTURE tb_exp5ex3 OF testbench_exp5ex3 IS
29
30  Begin
31
32
33  estimulo: PROCESS
34  begin
35      report "Iniciando teste..." severity NOTE;
36
37      for i in 0 to 15 loop
38          A <= std_logic_vector(to_unsigned(i, 4));
39          for j in 0 to 15 loop
40              B <= std_logic_vector(to_unsigned(j, 4));
41              wait for 500 ns;
42              assert (S_gm = S_dut) report "Falhou" severity ERROR;
43          end loop;
44      end loop;
45
46      report "Teste finalizado!" severity NOTE;
47
48      wait;
49
50  end PROCESS estimulo;
51
52  end tb_exp5ex3;
```

Compilação:



Simulação:





	Entrada A	Entrada B	Saída S (DUT)	Saída S (GM)
Cursor 1	0010	1100	01110	01110
Cursor 2	0011	0110	01001	01001
Cursor 3	0100	0001	00101	00101
Cursor 4	1010	1101	10111	10111
Cursor 5	1011	0101	10000	10000
Cursor 6	1100	0010	01110	01110