RELATÓRIO- PROJETO 7

Questão 1

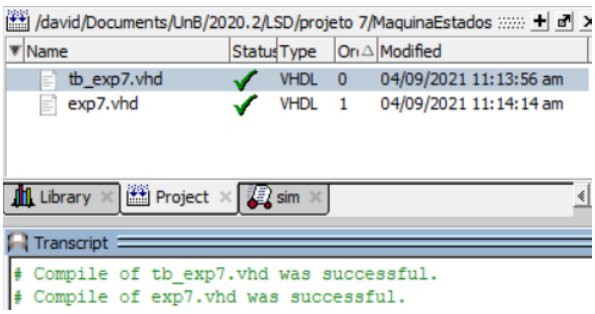
Arquivo exp7.vhd:

```
13  library IEEE;
14  use IEEE.std_logic_1164.ALL;
15  ----------------------------------------------------------
16  entity maquinaEstados is port(
17      A : in std_logic_vector(1 DOWNTO 0);
18      clock, reset : in std_logic;
19      -- Y : out std_logic_vector(2 DOWNTO 0));
20      refrigerante, troco25, troco50 : out std_logic);
21  end maquinaEstados;
22  ----------------------------------------------------------
23  architecture maquinaEstados_arch of maquinaEstados is
24
25
26      type estado is (STinit, ST25, ST50, ST75, ST100, ST125, D25, D50, D75);
27
28      signal currentState, nextState : estado;
29      signal Y : std_logic_vector(2 DOWNTO 0);
30
31  begin
32
33      sync_proc: process (clock, reset)
34      begin
35          if (reset = '1') then
36              currentState <= STinit;
37          elsif rising_edge(clock) then
38              currentState <= nextState;
39          end if;
40      end process sync_proc;
41
42      comb_proc: process(currentState, A)
43      begin
44          case currentState is
45              when STinit => Y <= "000";
46                  case A is
47                      when "01" => nextState <= ST25;
48                      when "10" => nextState <= ST50;
49                      when others => nextState <= STinit;
50                  end case;
51              when ST25 => Y <= "000";
52                  case A is
53                      when "00" => nextState <= ST25;
54                      when "01" => nextState <= ST50;
55                      when "10" => nextState <= ST75;
56                      when others => nextState <= D25;
57                  end case;
58              when ST50 => Y <= "000";
59                  case A is
60                      when "00" => nextState <= ST50;
61                      when "01" => nextState <= ST75;
62                      when "10" => nextState <= ST100;
61                      when "01" => nextState <= ST75;
62                      when "10" => nextState <= ST100;
63                      when others => nextState <= D50;
64                  end case;
65              when ST75 => Y <= "000";
66                  case A is
67                      when "00" => nextState <= ST75;
68                      when "01" => nextState <= ST100;
69                      when "10" => nextState <= ST125;
70                      when others => nextState <= D75;
71                  end case;
72              when ST100 => Y <= "100";
73                  case A is
74                      when "01" => nextState <= ST25;
75                      when "10" => nextState <= ST50;
76                      when others => nextState <= STinit;
77                  end case;
78              when ST125 => Y <= "110";
79                  case A is
80                      when "01" => nextState <= ST25;
81                      when "10" => nextState <= ST50;
82                      when others => nextState <= STinit;
83                  end case;
84              when D25 => Y <= "010";
85                  case A is
86                      when "01" => nextState <= ST25;
87                      when "10" => nextState <= ST50;
88                      when others => nextState <= STinit;
89                  end case;
90              when D50 => Y <= "001";
91                  case A is
92                      when "01" => nextState <= ST25;
93                      when "10" => nextState <= ST50;
94                      when others => nextState <= STinit;
95                  end case;
96              when D75 => Y <= "011";
97                  case A is
98                      when "01" => nextState <= ST25;
99                      when "10" => nextState <= ST50;
100                     when others => nextState <= STinit;
101                 end case;
102             when others =>
103                 Y <= "000";
104                 nextState <= STinit;
105         end case;
106     end process comb_proc;
107     refrigerante <= Y(2);
108     troco25 <= Y(1);
109     troco50 <= Y(0);
110 end maquinaEstados_arch;
```

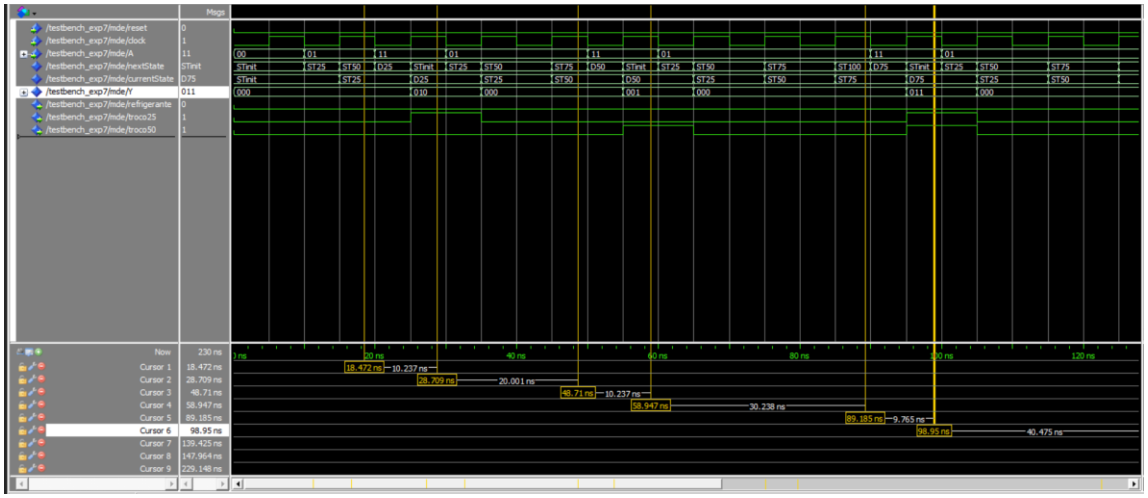
Arquivo tb_exp7.vhd:

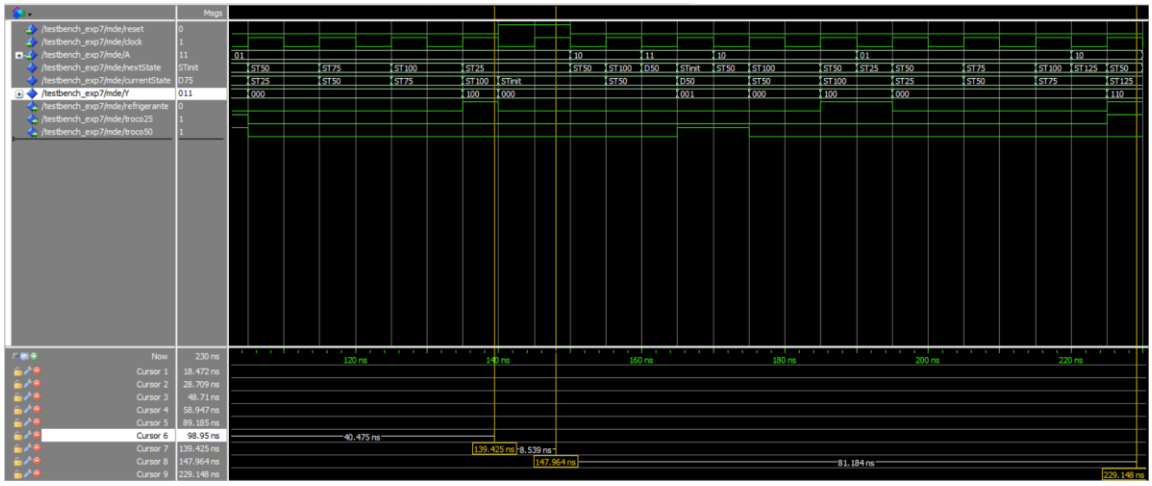
```
-- ************************************************
--  Testbench para simulacao Funcional do
--  Circuito: Máquina de estado síncrona do tipo
--  Moore para controlar uma máquina de refrigerantes
--          clock, reset - Entradas assíncronas
--          A - Entrada síncrona
--          STinit, ST25, ST50, ST75, ST100
--      ST125, D25, D50, D75 - Possíveis
--      estados que a máquina pode assumir
--          refrigerante, troco25, troco50 - Possíveis
--      saídas da máquina
-- ************************************************
-------------------------------------------------------
library IEEE;
use IEEE.std_logic_1164.all;
use std.textio.all;
use ieee.numeric_std.all;
-------------------------------------------------------

entity testbench_exp7 IS END;

architecture tb_exp7 of testbench_exp7 is

    component maquinaEstados
    port (
        clock, reset : in std_logic;
        A : in std_logic_vector(1 DOWNTO 0);
        refrigerante, troco25, troco50 : out std_logic);
    end component;
-------------------------------------------------------
    signal rst : std_logic;
    signal clk : std_logic := '0';
    signal a : std_logic_vector(1 DOWNTO 0);

    Begin

    mde: maquinaEstados PORT MAP (clock => clk, reset => rst, a => A , refrigerante => open, troco25 => open, troco50 => open);
    clk <= not clk after 5 ns;


   estimulo: PROCESS
   begin
       -- Código com reset desativado

       rst <= '0';

       a <= "00"; wait for 10 ns;      -- Mantendo o estado inicial
       a <= "01"; wait for 10 ns;      -- Adicionando 25 centavos
       a <= "11"; wait for 10 ns;      -- Devolvendo 25 centavos
       a <= "01"; wait for 20 ns;      -- Adicionando 25 centavos (x2)
       a <= "11"; wait for 10 ns;      -- Devolvendo 50 centavos
       a <= "01"; wait for 30 ns;      -- Adicionando 25 centavos (x3)
       a <= "11"; wait for 10 ns;      -- Devolvendo 75 centavos
       a <= "01"; wait for 40 ns;      -- Adicionando 25 centavos (x4), Retorna um refri

       rst <= '1'; wait for 10 ns;     -- Retornando ao estado inicial
       rst <= '0';

       a <= "10"; wait for 10 ns;      -- Adicionando 50 centavos
       a <= "11"; wait for 10 ns;      -- Devolvendo 50 centavos
       a <= "10"; wait for 20 ns;      -- Adicionando 50 centavos (x2)
       a <= "01"; wait for 30 ns;      -- Adicionando 75 centavos
       a <= "10"; wait for 10 ns;      -- Adicionando 50 centavos, retorna 25 centavos e um refri


   end PROCESS estimulo;
end tb_exp7;
```

Compilação:



Simulação:





	reset	clock	Current State	Refri	Troco 25	Troco 50	A	Next State
Cursor 1	0	SUBIDA	ST25	0	0	0	01	ST50
Cursor 2	0	SUBIDA	D25	0	1	0	11	INIT
Cursor 3	0	SUBIDA	ST50	0	0	0	01	ST75
Cursor 4	0	SUBIDA	D50	0	0	1	11	INIT
Cursor 5	0	SUBIDA	ST75	0	0	0	01	ST100
Cursor 6	0	SUBIDA	D75	0	1	1	11	INIT
Cursor 7	0	SUBIDA	ST100	1	0	0	01	ST25
Cursor 8	1	SUBIDA	INIT	0	0	0	01	ST25
Cursor 9	0	SUBIDA	ST125	1	1	0	10	ST50