RELATÓRIO- PROJETO 3

Questão 1
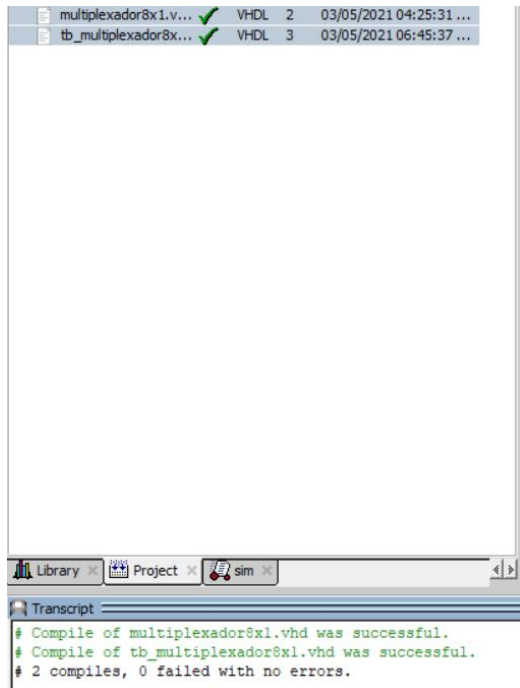
Arquivo multiplexador8x1.vhd:

```vhdl
1    --  ************************************************
2    --  Circuito: Multiplexador 8x1
3    --          D    Vetor de Entradas
4    --          S    Seletor
5    --          Y    Saída
6    --  ************************************************
7    ----------------------------------------------------------
8    library IEEE;
9    use IEEE.std_logic_1164.all;
10   ----------------------------------------------------------
11
12   entity MULTIPLEXADOR8X1 is port (
13       D  :in std_logic_vector (7 DOWNTO 0);
14       S  :in std_logic_vector (2 DOWNTO 0);
15       Y  :out std_logic);
16   end MULTIPLEXADOR8X1;
17   ----------------------------------------------------------
18
19   architecture mux8x1 of MULTIPLEXADOR8X1 is
20   begin
21
22      Y <= D(0) when S = "000" else
23           D(1) when S = "001" else
24           D(2) when S = "010" else
25           D(3) when S = "011" else
26           D(4) when S = "100" else
27           D(5) when S = "101" else
28           D(6) when S = "110" else
29           D(7) when S = "111";
30   end mux8x1;
```
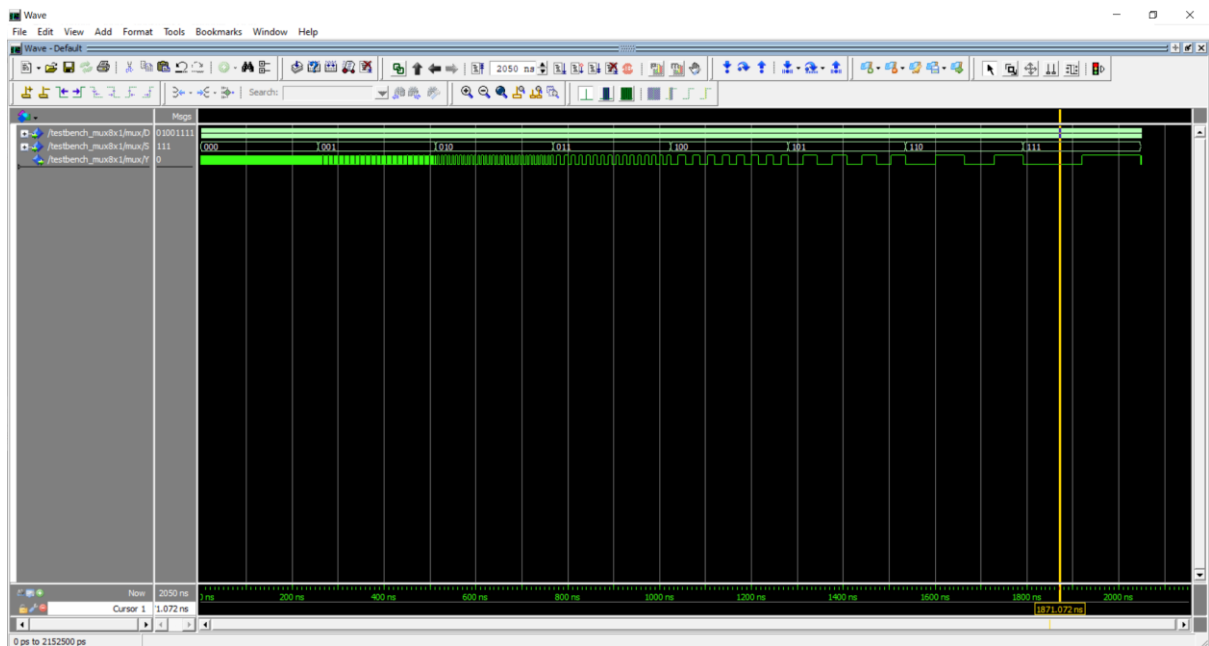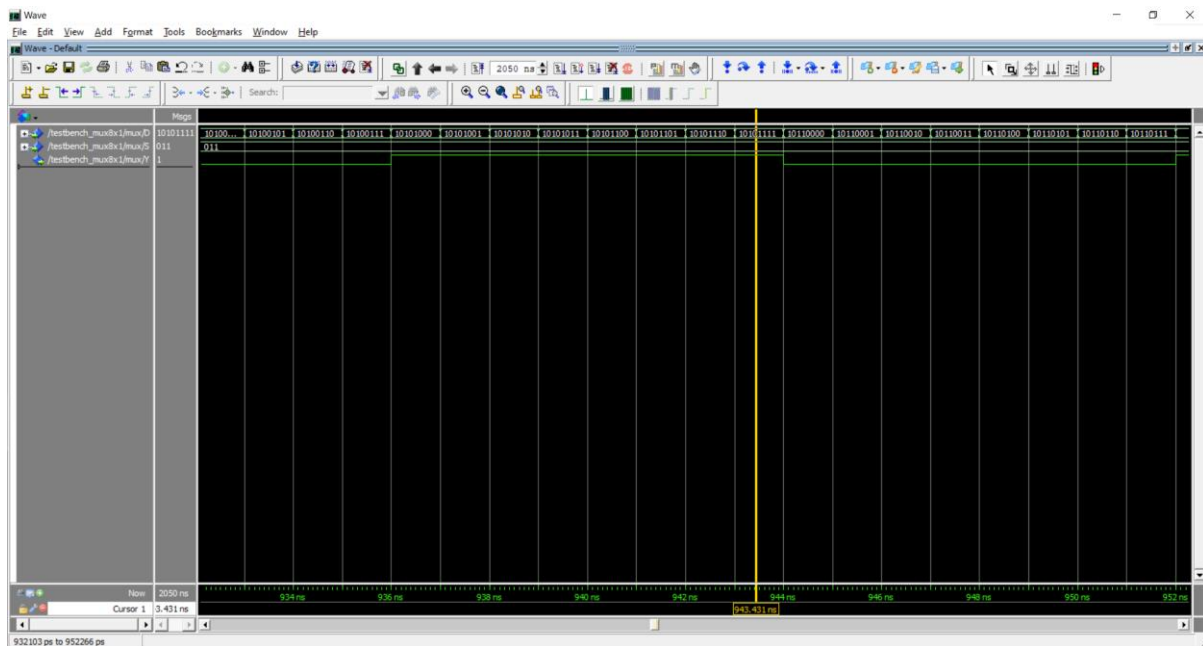
Arquivo tb_multiplexador8x1.vhd:

```vhdl
 7
 8    ENTITY testbench_mux8x1 IS END;
 9
10    -------------------------------------------------------
11    LIBRARY ieee;
12    USE ieee.std_logic_1164.ALL;
13    USE std.textio.ALL;
14    USE ieee.numeric_std.ALL;
15    -------------------------------------------------------
16
17    ARCHITECTURE tb_multiplexador8x1 OF testbench_mux8x1 IS
18
19    component MULTIPLEXADOR8X1
20
21    port(
22        S :in std_logic_vector (2 DOWNTO 0);
23        D :in std_logic_vector (7 DOWNTO 0);
24        Y :out std_logic);
25    end component;
26    -------------------------------------------------------
27
28    signal clk  : std_logic_vector (7 DOWNTO 0);
29    signal tb_s : std_logic_vector (2 DOWNTO 0);
30
31    Begin
32
33    mux: MULTIPLEXADOR8X1 PORT MAP (D => clk, S => tb_s, Y => open);
34
35
36    --Implementacao do processo de estimulo
37
38    clock: PROCESS
39    begin
40        for i in 0 to 255 loop
41            clk <= std_logic_vector(to_unsigned(i, 8));
42            wait for 1 ns;
43        end loop;
44    end process;
45
46
47    tbs: PROCESS
48    begin
49        tb_s <= "000"                , "001" after 256  ns, "010" after 512  ns, "011" after 768  ns,
50                "100" after 1024 ns, "101" after 1280 ns, "110" after 1536 ns, "111" after 1792 ns;
51                wait for 2048 ns;
52    end PROCESS;
53
54    end tb_multiplexador8x1;
```

Compilação:


```
# Compile of multiplexador8x1.vhd was successful.
# Compile of tb_multiplexador8x1.vhd was successful.
# 2 compiles, 0 failed with no errors.
```

Simulação:

Questão 2

Arquivo decodificador4x16.vhd:

```vhdl
6   -------------------------------------------
7   library IEEE;
8   use IEEE.std_logic_1164.all;
9   -------------------------------------------
10
11  entity DECODIFICADOR4X16 is port (
12      A  :in  std_logic_vector (3  DOWNTO 0);
13      Y  :out std_logic_vector (15 DOWNTO 0));
14  end DECODIFICADOR4X16;
15  -------------------------------------------
16
17  architecture dec4x16 of DECODIFICADOR4X16 is
18  begin
19      with A select
20      Y <= "0000000000000001" when "0000",
21           "0000000000000010" when "0001",
22           "0000000000000100" when "0010",
23           "0000000000001000" when "0011",
24           "0000000000010000" when "0100",
25           "0000000000100000" when "0101",
26           "0000000001000000" when "0110",
27           "0000000010000000" when "0111",
28           "0000000100000000" when "1000",
29           "0000001000000000" when "1001",
30           "0000010000000000" when "1010",
31           "0000100000000000" when "1011",
32           "0001000000000000" when "1100",
33           "0010000000000000" when "1101",
34           "0100000000000000" when "1110",
35           "1000000000000000" when "1111",
36           "0000000000000000" when others;
37  end dec4x16;
```

Arquivo tb_decodificador4x16.vhd:

```vhdl
7    ENTITY testbench_dec4x16 IS END;
8
9    --------------------------------------------------------
10   LIBRARY ieee;
11   USE ieee.std_logic_1164.ALL;
12   USE std.textio.ALL;
13   use ieee.std_logic_signed.ALL;
14   --------------------------------------------------------
15
16   ARCHITECTURE tb_decodificador4x16 OF testbench_dec4x16 IS
17
18   component DECODIFICADOR4X16
19
20   port(
21       A  :in  std_logic_vector (3  DOWNTO 0);
22       Y  :out std_logic_vector (15 DOWNTO 0));
23   end component;
24   --------------------------------------------------------
25
26   signal A : std_logic_vector (3  DOWNTO 0);
27   signal Y : std_logic_vector (15 DOWNTO 0);
28
29   Begin
30
31   dec: DECODIFICADOR4x16 PORT MAP (A => A, Y => Y);
32
33   --Implementacao do processo de estimulo
34
35   A <= "0000"             , "0001" after 5  ns, "0010" after 10 ns, "0011" after 15 ns,
36          "0100" after 20 ns, "0101" after 25 ns, "0110" after 30 ns, "0111" after 35 ns,
37          "1000" after 40 ns, "1001" after 45 ns, "1010" after 50 ns, "1011" after 55 ns,
38          "1100" after 60 ns, "1101" after 65 ns, "1110" after 70 ns, "1111" after 75 ns;
39
40   end tb_decodificador4x16;
```

Compilação:

Simulação: