RELATÓRIO- PROJETO 4

Questão 1

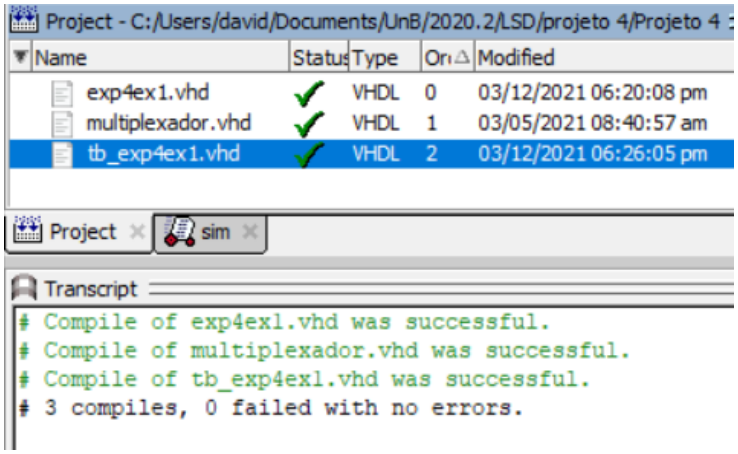
Arquivo exp4ex1.vhd:

```
-- ******************************************************
--  Circuito: Entidade com 3 bits de entrada
--  usando 2 multiplexadores 4x1 como componentes
--          A  Entrada 1
--          B  Entrada 2
--          C  Entrada 3
--          X  Saída 1 (X = (~A)·B·C + A·(~B)·(~C) + A·B)
--          Y  Saída 2 (Y = (~A)·(~B) + (~A)·B·(~C) + A·B·C)
-- ******************************************************
-------------------------------------------------------
library IEEE;
use IEEE.std_logic_1164.all;
-------------------------------------------------------

entity EXP4EX1 is port (
    A, B, C :in  std_logic;
    X, Y    :out std_logic);
end EXP4EX1;

architecture ex1 of EXP4EX1 is

    component MULTIPLEXADOR is
    port (
        S              :in std_logic_vector (1 DOWNTO 0);
        D0, D1, D2, D3 :in std_logic;
        Y              :out std_logic);
    end component;

    signal not_c : std_logic;

    Begin
    not_C <= not C;
    Mux1: MULTIPLEXADOR PORT MAP (D3 => '1', D2 => not_C, D1 => C, D0 => '0', S(1) => A, S(0) => B, Y => X);
    Mux2: MULTIPLEXADOR PORT MAP (D3 => C, D2 => '0', D1 => not_C, D0 => '1', S(1) => A, S(0) => B, Y => Y);
end ex1;
```

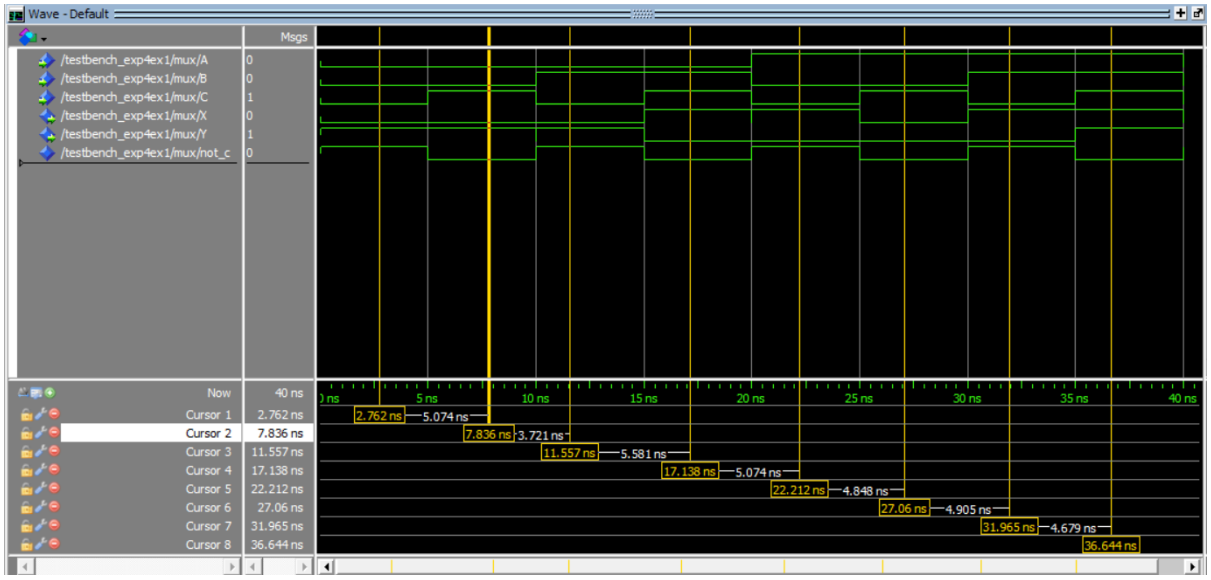
Arquivo tb_exp4ex1.vhd:

```
12  LIBRARY ieee;
13  USE ieee.std_logic_1164.ALL;
14  USE std.textio.ALL;
15  ----------------------------------------------------
16
17  ENTITY testbench_exp4ex1 IS END;
18
19  ARCHITECTURE tb_exp4ex1 OF testbench_exp4ex1 IS
20
21  component EXP4EX1
22
23  port (
24      A, B, C :in  std_logic;
25      X, Y    :out std_logic);
26  end component;
27  ----------------------------------------------------
28
29  signal aa, bb, cc : std_logic;
30
31  Begin
32
33  mux: EXP4EX1 PORT MAP (A => aa, B => bb, C => cc, X => open, Y => open);
34
35  estimulo: PROCESS
36
37  begin
38
39      aa <= '0'; bb <= '0'; cc <= '0'; wait for 5 ns;
40      cc <= '1'; wait for 5 ns;
41      bb <= '1'; cc <= '0'; wait for 5 ns;
42      cc <= '1'; wait for 5 ns;
43      aa <= '1'; bb <= '0'; cc <= '0'; wait for 5 ns;
44      cc <= '1'; wait for 5 ns;
45      bb <= '1'; cc <= '0'; wait for 5 ns;
46      cc <= '1'; wait for 5 ns;
47
48  end PROCESS estimulo;
49
50  end tb_exp4ex1;
```

Compilação:



Simulação:



	Entrada A	Entrada B	Entrada C	Saída X	Saída Y
Cursor 1	0	0	0	0	1
Cursor 2	0	0	1	0	1
Cursor 3	0	1	0	0	1
Cursor 4	0	1	1	1	0
Cursor 5	1	0	0	1	0
Cursor 6	1	0	1	0	0
Cursor 7	1	1	0	1	0
Cursor 8	1	1	1	1	1

Questão 2

Arquivo exp4ex2.vhd:

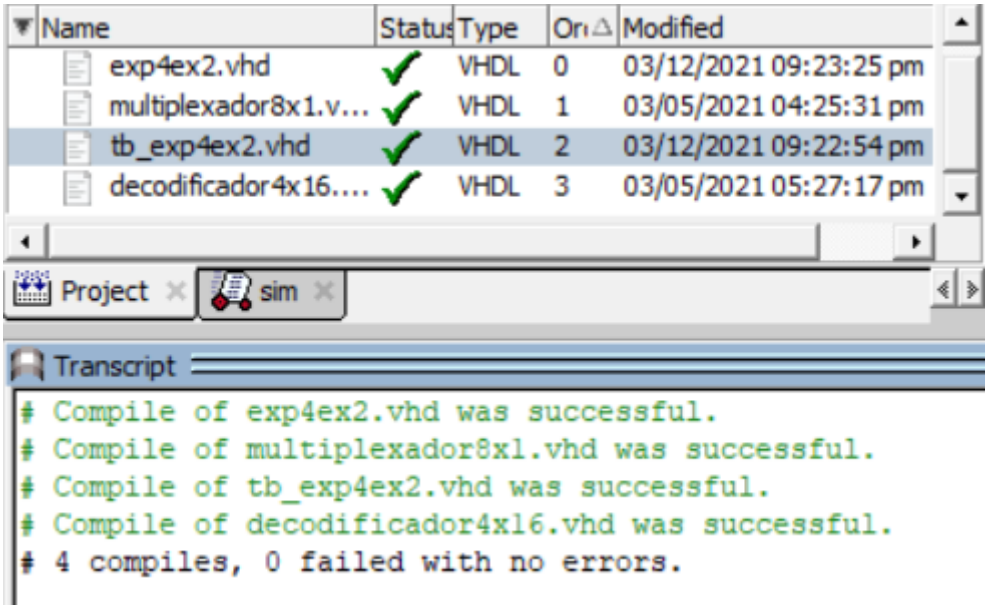
```
-- ********************************************************
--  Circuito: Entidade com 7 bits de entrada
--  usando 1 multiplexador 8x1 e um
--  decodificador 4x16 como componentes
--  A, B, C e D serão as entradas do decodificador
--  e E, F e G atuarão como seletores para o multiplexador
--          A  Entrada 1 (Bit mais significativo)
--          B  Entrada 2
--          C  Entrada 3
--          D  Entrada 4
--          E  Seletor 1 (Bit mais significativo)
--          F  Seletor 2
--          G  Seletor 3
--          S  Saída
--          S = (F·G + A·B·C·D·(~E)·(~F)·G +
--              (~A)·(~B)·(~C)·(~D)·(~E)·(~F)·G +
--              A·(~B)·C·E·F·(~G) + (~A)·B·C·D·(~E)·F·(~G) +
--              A·B·C·D·E·(~F)·(~G) + A·(~B)·(~C)·D·E·(~F)·(~G))
-- ********************************************************
```

```
------------------------------------------------------------
library IEEE;
use IEEE.std_logic_1164.all;
------------------------------------------------------------

entity EXP4EX2 is port (
    A, B, C, D, E, F, G :in  std_logic;
    S                   :out std_logic);
end EXP4EX2;

architecture ex2 of EXP4EX2 is

    component DECODIFICADOR4X16 is
    port (
        A  :in  std_logic_vector (3  DOWNTO 0);
        Y  :out std_logic_vector (15 DOWNTO 0));
    end component;

    component MULTIPLEXADOR8X1 is
    port (
    D  :in std_logic_vector (7 DOWNTO 0);
    S  :in std_logic_vector (2 DOWNTO 0);
    Y  :out std_logic);
    end component;

    signal Y_signal : std_logic_vector (15 DOWNTO 0);
    signal D_signal : std_logic_vector (7  DOWNTO 0);
    signal Y015, Y915, Y1011 : std_logic;

    Begin
    dec: DECODIFICADOR4X16 PORT MAP (A(3) => A, A(2) => B, A(1) => C, A(0) => D, Y => Y_signal);

    Y015  <= Y_signal(0)  or Y_signal(15);
    Y915  <= Y_signal(9)  or Y_signal(15);
    Y1011 <= Y_signal(10) or Y_signal(11);

    D_signal(0) <= '0';
    D_signal(1) <= Y015;
    D_signal(2) <= '0';
    D_signal(3) <= '1';
    D_signal(4) <= Y915;
    D_signal(5) <= '0';
    D_signal(6) <= Y1011;
    D_signal(7) <= '1';

    mux: MULTIPLEXADOR8X1 PORT MAP (D => D_signal, S(2) => E, S(1) => F, S(0) => G, Y => S);
end ex2;
```

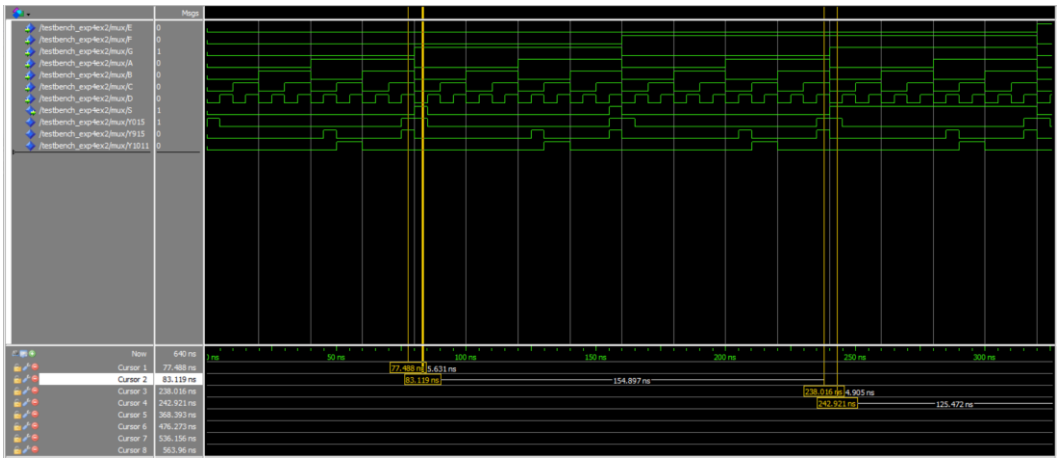
Arquivo tb_exp4ex2.vhd:

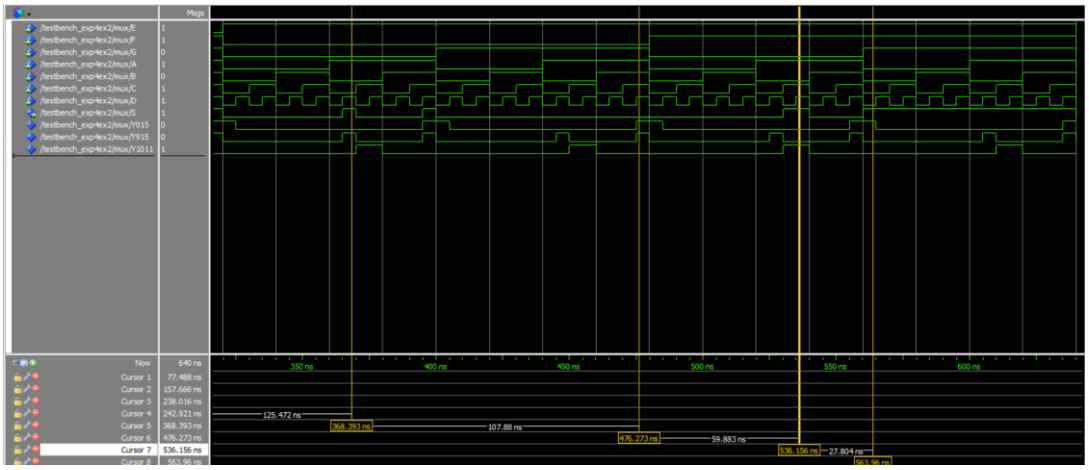
```
21  ----------------------------------------------------
22  LIBRARY ieee;
23  USE ieee.std_logic_1164.ALL;
24  USE std.textio.ALL;
25  USE ieee.numeric_std.ALL;
26  ----------------------------------------------------
27
28  ENTITY testbench_exp4ex2 IS END;
29
30  ARCHITECTURE tb_exp4ex2 OF testbench_exp4ex2 IS
31
32  component EXP4EX2
33
34  port (
35      A, B, C, D, E, F, G :in  std_logic;
36      S                   :out std_logic);
37  end component;
38  ----------------------------------------------------
39
40  signal entrada : std_logic_vector (6 DOWNTO 0);
41
42  Begin
43
44  mux: EXP4EX2 PORT MAP (E => entrada(6), F => entrada(5), G => entrada(4), A => entrada(3), B => entrada(2), C => entrada(1), D => entrada(0), S => open);
45
46  estimulo: PROCESS
47
48  begin
49      for i in 0 to 127 loop
50          entrada <= std_logic_vector(to_unsigned(i, 7));
51          wait for 5 ns;
52      end loop;
53  end PROCESS estimulo;
54
55  end tb_exp4ex2;
```

Compilação:



Simulação:





	Seletor E	Seletor F	Seletor G	Entrada A	Entrada B	Entrada C	Entrada D	Saída S
Cursor 1	0	0	0	1	1	1	1	0
Cursor 2	0	0	1	0	0	0	0	1
Cursor 3	0	1	0	1	1	1	1	0
Cursor 4	0	1	1	0	0	0	0	1
Cursor 5	1	0	0	1	0	0	1	1
Cursor 6	1	0	1	1	1	1	1	0
Cursor 7	1	1	0	1	0	1	1	1
Cursor 8	1	1	1	0	0	0	0	1