數位系統導論

Introduction to Digital System

Pei-Yin Chen, 陳培殷

Syllabus

- Time and Place
  - Tuesday: 9:10 ~ 12:00　　化工系 華立廳
- Contact Information
  - 資訊工程系 新大樓 11F (06-2757575 EXT 62547)
  - E-mail: pychen@mail.ncku.edu.tw
- Office Hour (please confirm with email)
  - Wednesday: 16:00~18:00　Thursday: 10:00~11:00
- Course Assistants
  - 資訊工程系大樓 10F DIC (Digital IC Design) Lab
    陳宥融博士生

因應疫情之上課方式

- 9/28 線上上課 (課程說明與簡介) ---- 同步線上
- 自行觀看課程前7周的教學影片 ---- 非同步(My Tube)
- 11/2 10:00 第一次期中考 ---- 實體考試
- 11/9~11/30 視疫情決定上課方式 ---- 實體 或 非同步
- 12/7 10:00 第二次期中考 ---- 實體考試
- 12/14~1/4 視疫情決定上課方式 ---- 實體 或 非同步
- 1/11 10:00 期末考 ---- 實體考試

Office Hour (請事先以email確認為實體或線上討論)

Wednesday: 16:00~18:00 Thursday: 10:30~12:30

Syllabus (continued)

研讀方式: Text book + 上課投影片

- **Textbook**
  - M. Morris Mano Michael D. Ciletti, "Digital Design: With an Introduction to the Verilog HDL" , 6/e, 滄海書局代理
- **References**
  - Charles H. Roth, "Fundamentals of Logic Design," PWS
  - HDL chip design (Douglas J. Smith), Doone Publications
  - 陳培殷, 數位邏輯設計,滄海書局, 2017
  - 陳培殷, 數位IC設計—Verilog, 滄海書局, 2008
- **Grading Policies**

  Mid-term Exam-I: 30% (11/2)

  Mid-term Exam-II: 30% (12/7)

  Final Exam: 40~30% (1/11, 2022)

Goal

Goal:

1. Understand the basic concepts of digital circuit.

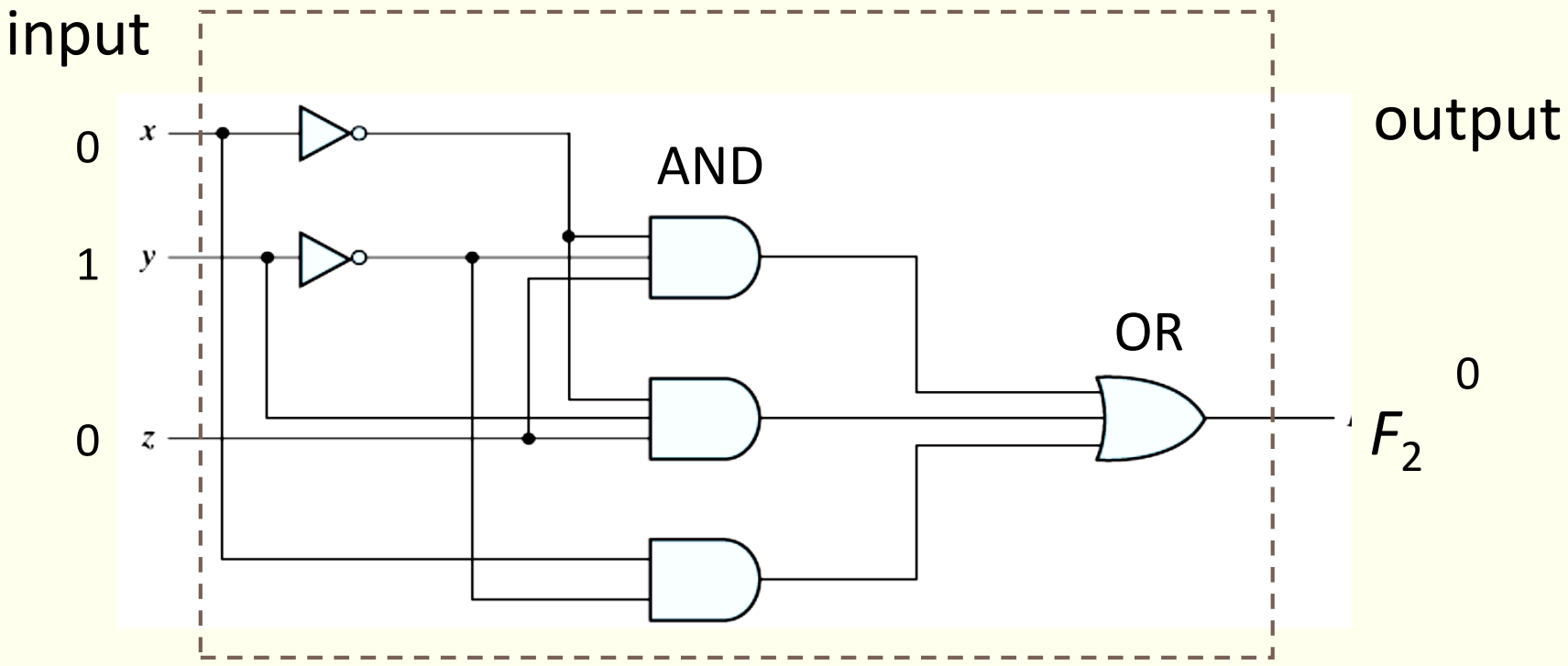
2. Understand the basic skills for digital circuit design

課程概述	介紹數位電路相關的基礎知識，包含：邏輯閘、組合電路、循序電路與數位系統架構設計等。
教學目標	讓學生具備數位電路的基本觀念，並熟悉設計數位電路的相關技巧。

Overview of a Digital Circuit

A digital circuit accepts the input bit-stream (0 and 1), processes it and produces the proper output results (0 and 1).

Inside a Digital Circuit



A lot of logic gates which use the input bitstream to produce the output bitstream.

Operator Precedence

- **Operator Precedence**
  - parentheses
  - NOT
  - AND
  - OR
  - examples
    - x y′ + z ➔ is x • y’ not (xy)’
    - (x y + z)′
- **The operations are implemented with logic gates**

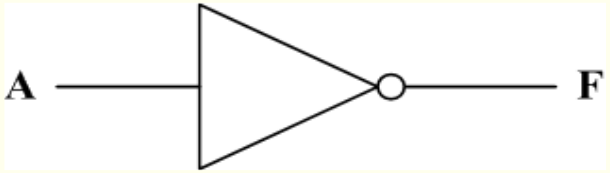
Boolean Functions and Gates (1/6)

- **NOT** gate (反閘/反相閘)

0: false (low-voltage)

1: true (high voltage)

$F = A'$ or $\overline{A}$



Truth Table (真值表)

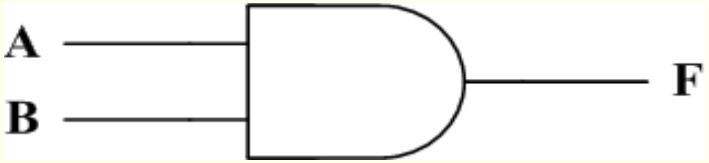
A	F
0	1
1	0

Input output

Boolean Functions and Gates (2/6)

- AND gate (且閘/及閘)

$F = A \cdot B = AB$



Truth Table (真值表)

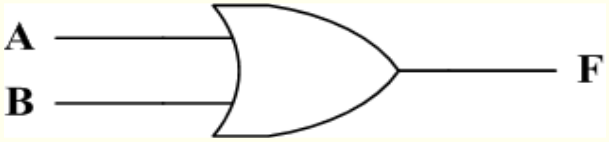
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

Input output

Boolean Functions and Gates (3/6)

- OR gate (或閘)

$F = A + B$



Truth Table (真值表)

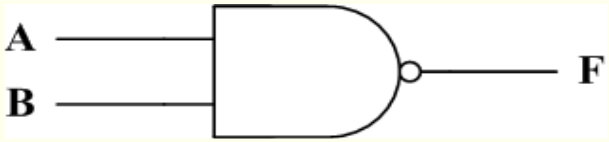
A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

Input output

Boolean Functions and Gates (4/6)

- **NAND** gate (反及閘)

$F = (AB)'$ or $\overline{(AB)}$



Truth Table

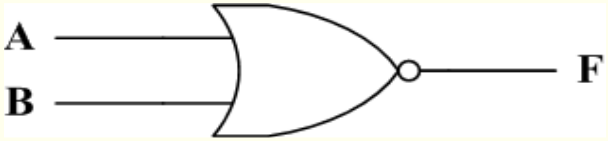
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

Input output

Boolean Functions and Gates (5/6)

- **NOR** gate (反或閘)

$$F = (A + B)' \text{ or } \overline{(A + B)}$$



Truth Table

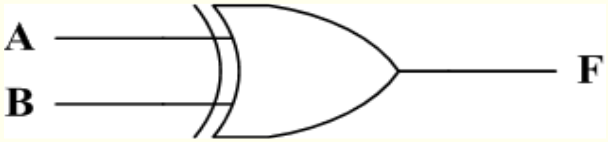
A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

Input output

Boolean Functions and Gates (6/6)

- Exclusive-OR (XOR) gate (互斥或閘)

$F = AB' + A'B = A \oplus B$



Truth Table

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

Input output

真值表

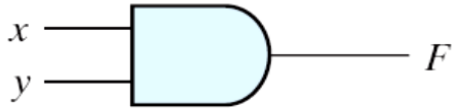
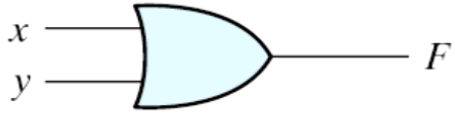
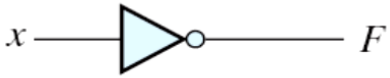
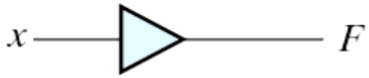
Name	Graphic symbol	Algebraic function	Truth table
AND		$F = xy$	x y | F 0 0 | 0 0 1 | 0 1 0 | 0 1 1 | 1
OR		$F = x + y$	x y | F 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 1
Inverter		$F = x'$	x | F 0 | 1 1 | 0
Buffer		$F = x$	x | F 0 | 0 1 | 1

Figure 2.5 Digital logic gates (continued)

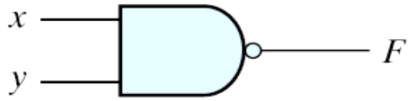
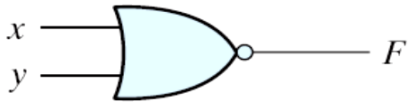
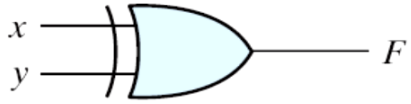
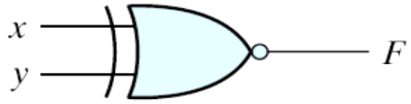
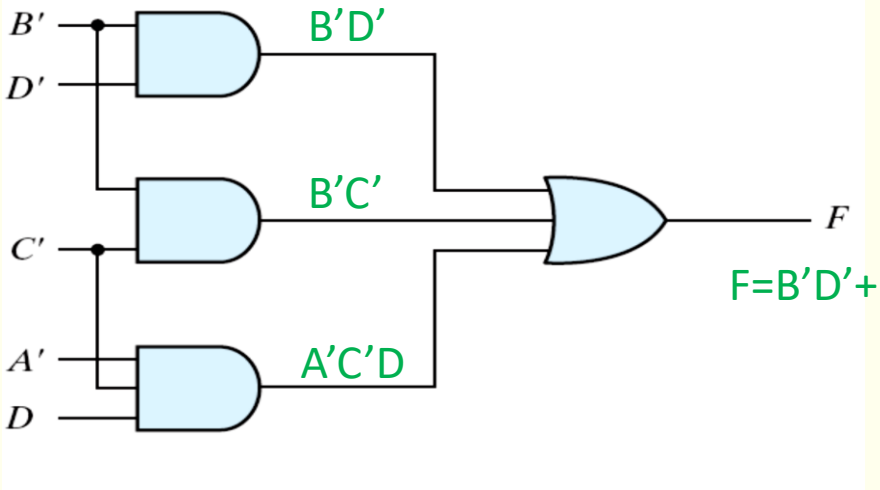
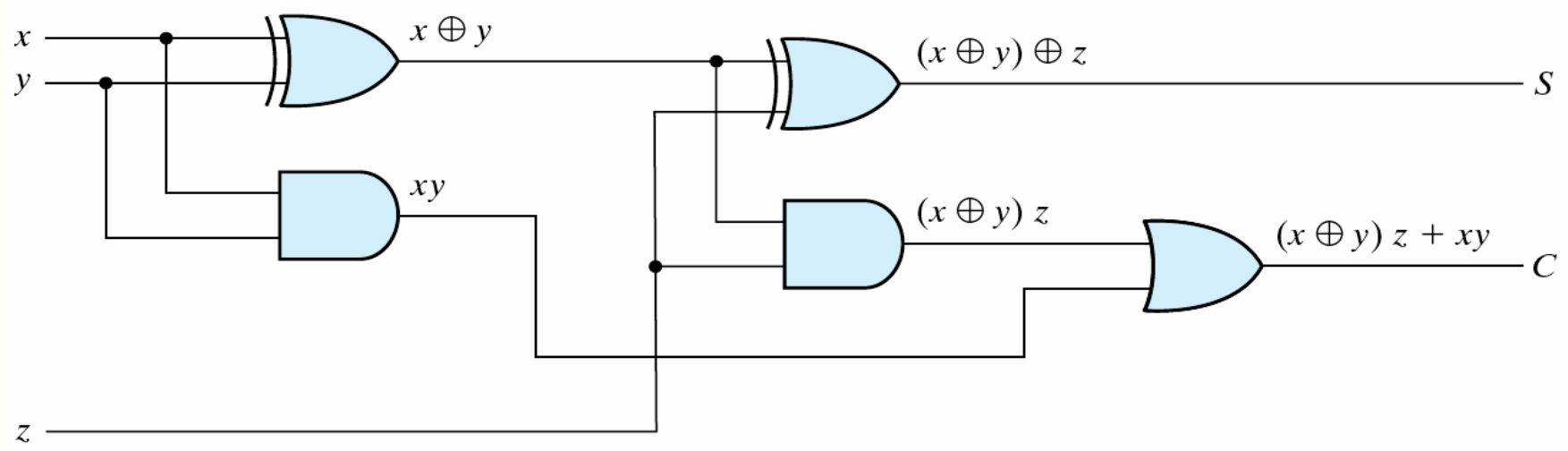
NAND		$F = (xy)'$	x y F 0 0 1 0 1 1 1 0 1 1 1 0
NOR		$F = (x + y)'$	x y F 0 0 1 0 1 0 1 0 0 1 1 0
Exclusive-OR (XOR)		$F = xy' + x'y$ $= x \oplus y$	x y F 0 0 0 0 1 1 1 0 1 1 1 0
Exclusive-NOR or equivalence		$F = xy + x'y'$ $= (x \oplus y)'$	x y F 0 0 1 0 1 0 1 0 0 1 1 1

Figure 2.5 Digital logic gates

A Simple Circuit



F=B’D’+B’C’+A’C’D

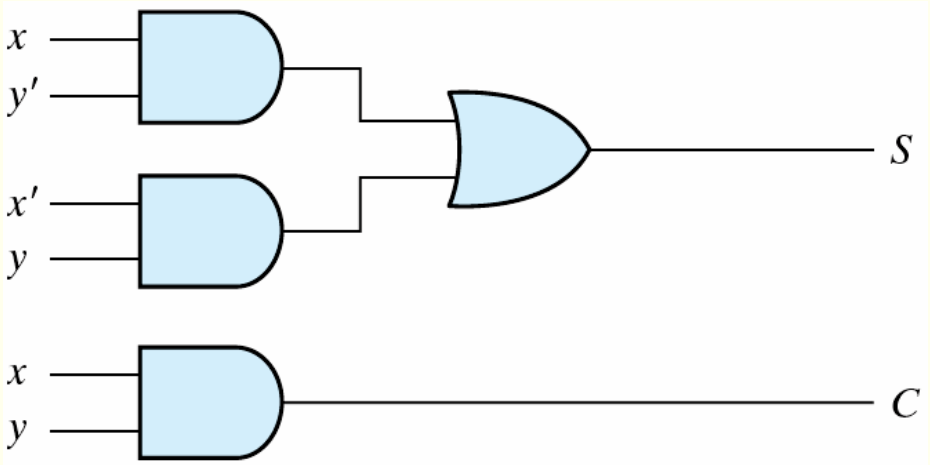


Half Adder

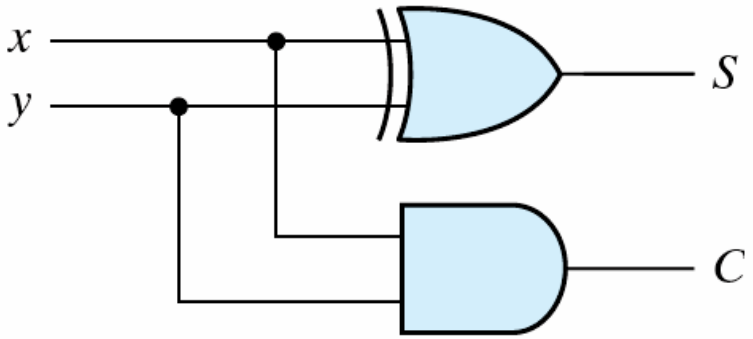
	x	0	0	1	1
+	y	0	1	0	1
		00	01	01	10

Table 4.3
Half Adder

		carry	sum
x	***y***	***C***	***S***
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

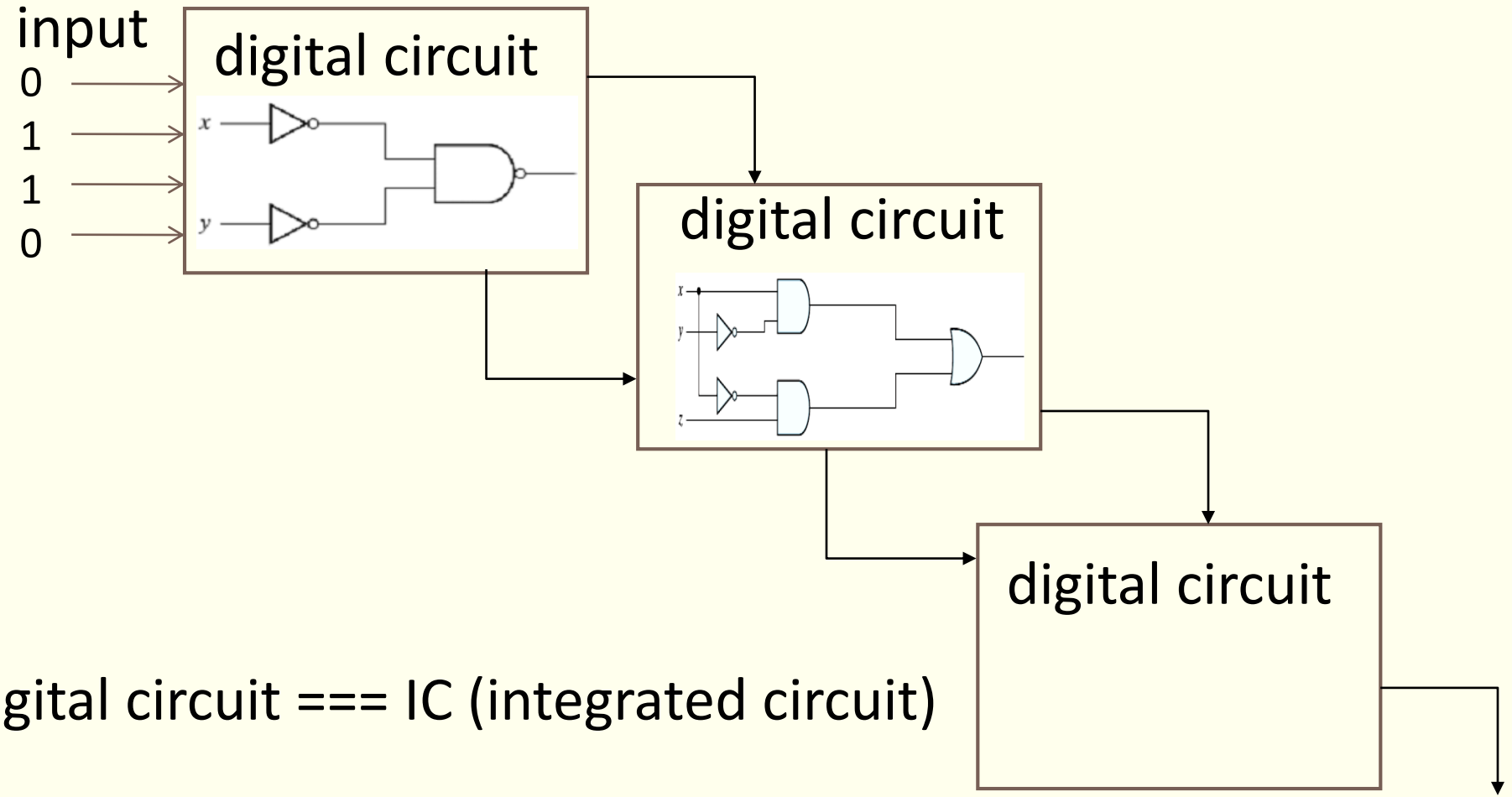


(a) $S = xy' + x'y$
$C = xy$



(b) $S = x \oplus y$
$C = xy$

Digital System



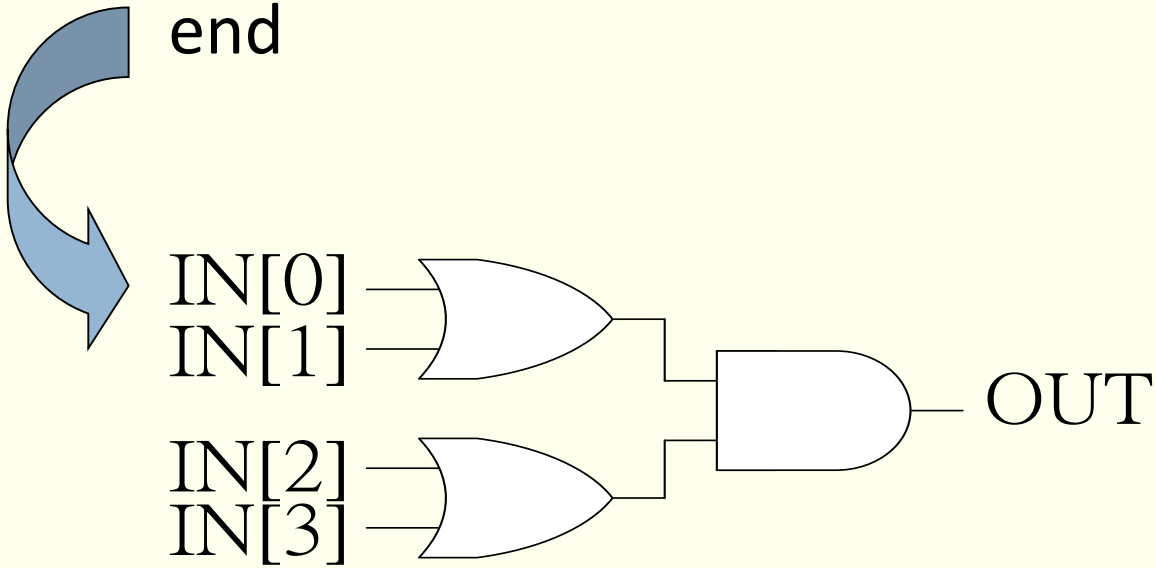
digital circuit === IC (integrated circuit)

semiconductor

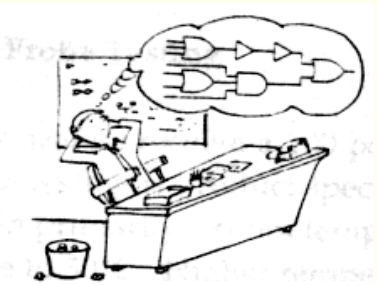
Digital IC Design

Example:

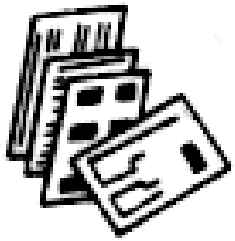
```
always @(IN)
begin
  OUT = (IN[0] | IN[1]) & (IN[2] | IN[3]);
end
```



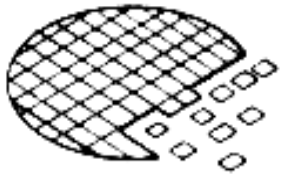
IC Industry in Taiwan



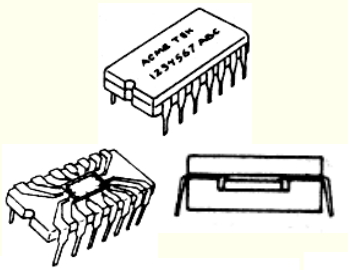
邏輯設計



光罩設計



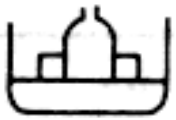
晶粒測試及切割



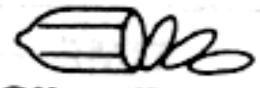
封 裝

成品測試

設計 → 光罩 → 製造 → 封裝 → 測試



長晶



晶圓切割

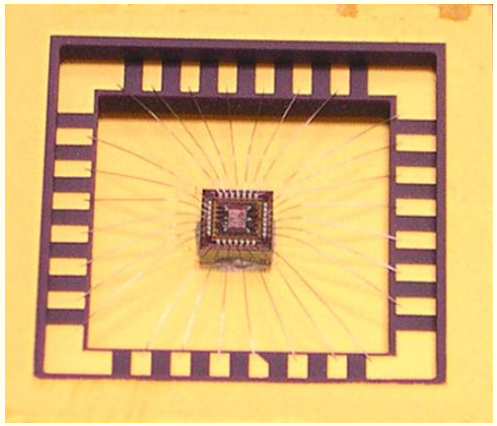
晶圓

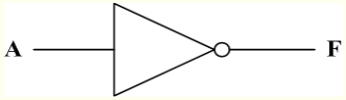
化學品

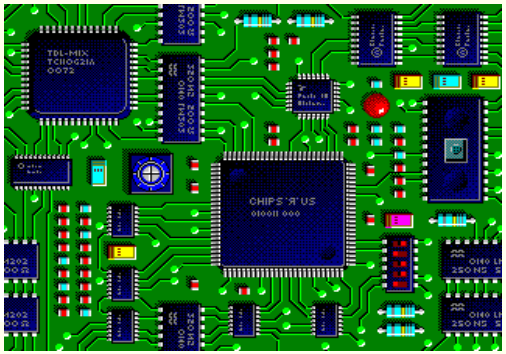
導線架

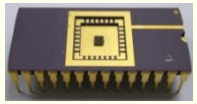
Chip/Circuit Everywhere!

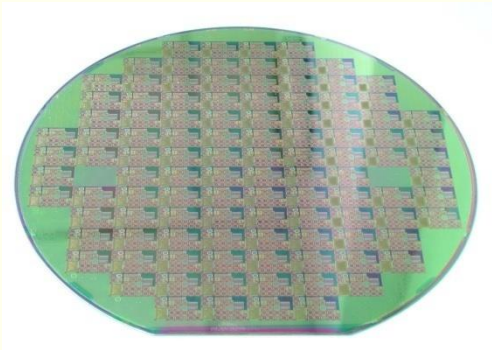
Applications

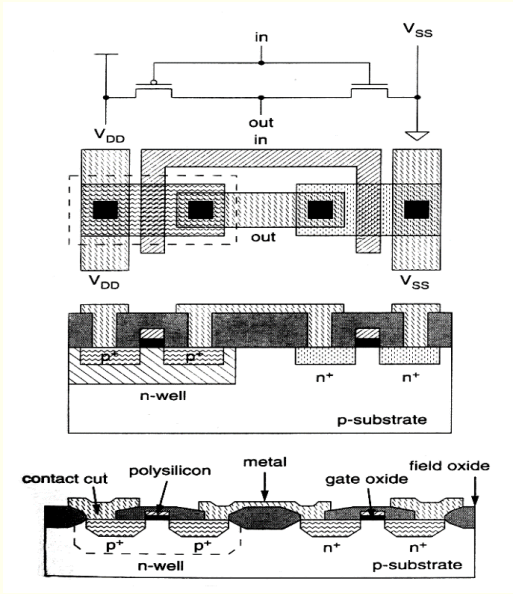












2020 Top 10 Fabless IC Suppliers

http://www.thelec.net/news/articleView.html?idxno=2567

Rank	Company	2020 Revenue	2019 Revenue	YoY Change
1	Qualcomm	19,407	14,518	33.7%
2	Broadcom	17,745	17,246	2.9%
3	Nvidia	15,412	10,125	52.2%
聯發科 ★ 4	MediaTek	10,929	7,962	37.3%
5	AMD	9,763	6,731	45.0%
6	Xilinx	3,053	3,234	-5.6%
7	Marvell	2,942	2,708	8.7%
聯詠 ★ 8	Novatek	2,712	2,085	30.1%
瑞昱 ★ 9	Realtek	2,635	1,965	34.1%
10	Dialog	1,376	1,421	-3.2%
Top 10 Total		85,974	67,995	26.4%

2019台灣IC設計公司營收

三千兩百億

排名	公司	千元
1	聯發科	322,145,988
2	聯詠	79,955,521
3	瑞昱	77,759,469
	群聯 [*]	48,496,522
	擎亞 [*]	26,889,818
4	奇景光電	26,214,000
	新唐 [*]	20,668,056
5	慧榮	15,507,030
6	譜瑞	15,278,350
7	晶豪	15,268,091
8	義隆	15,099,690
9	瑞鼎	14,425,152
10	矽力	13,936,157
11	矽創	13,804,562
12	敦泰	13,800,348
13	創意	13,569,441
14	天鈺	10,884,838
15	原相	8,148,017
16	致新	7,407,799
17	祥碩	6,987,470
18	威盛	6,502,741
19	神盾	6,224,427
20	盛群	5,614,539
21	智原	5,498,295
22	凌陽	6,439,865
23	茂達	5,389,874

Outline

Chapter 1: Binary System

Chapter 2: Boolean Algebra and Logic Gates

Chapter 3: Gate-Level Minimization

Chapter 4: Combinational Logic

Chapter 5: Synchronous sequential Logic

Chapter 6: Registers and Counters

Chapter 7: Memory and Programmable Logic

Chapter 8: Design at the Register Transfer Level

系上教育目標(工程認證)

- 課程成績評量參考指標

■紙筆測驗	■書面報告	□口頭報告
□課堂問答	□實作表現	■上課表現
■指定作業	□專題研究	■課堂出席

- 修習本課程後，學生可獲得以下核心能力

■ 1.1 具備基礎專業數學及資訊理論知識之基本能力
■ 1.2 具備理論推導及實驗數據分析歸納之能力
□ 1.3 具備終身學習之能力
■ 2.1 具備發掘、分析及解決資訊應用問題之能力
■ 2.2 具備資訊工程設計、創新、測試及驗證之能力
■ 2.3 具備系統整合之能力
□ 3.1 具備科技人文素養及資訊工程倫理之精神
□ 3.2 具備良好溝通技巧及國際觀
□ 3.3 具備負責之工作態度及團隊合作之能力