ECE411 PCB Checklist

v2011-10-31

- Pre-layout Checklist
  - Create board from schematic.
  - Verify that your design rules in the DRC dialog match your manufacturer's design rules: trace/space, board edge, minimum drill size, etc.
  - Set the via shape to 'round' with the minimum size drill possible.
  - Set your grid to something reasonable (e.g., 0.1 mm grid, or 0.01 inch grid).
  - Set the outline of your board in the dimension layer (if different than the default).
  - Create keyboard shortcuts or layer aliases to be able to quickly switch between layer groupings
    - to = top only = tplace tdocu torigin top pads vias unrouted dimension document
    - bo = bottom only = bplace bdoc borigin bottom pads vias unrouted dimension document
    - tb = top and bottom = both above
    - ctrl-g for group, ctrl-m for move, ctrl-r for route, ctrl-d delete, etc
- Lay out strategies
  - Place all components that must be in a certain spot (e.g., connectors and mounting holes)
  - Move components that are in a “schematic block” together, then optimally rotate and place components to reduce crossed airwires, then route.
  - Optimally rotate and place grouped components to minimize airwires, then route.
  - Route power lines and ground planes.
- Layout checklist
  - Optional but recommended: are components snapped to the grid?
  - Is there enough physical space around components?
  - Are your test points in easily accessible places?
  - Are there any hidden traces that you can't probe?
- Best Practices
  - Are all of the small bypass caps right next to the power and ground leads of the ICs?
  - Are the power lines as wide as reasonably possible?
  - Did you use either larger drills for power lines, or multiple small vias for power lines?
  - Are there ground planes (polygons with name 'GND') on both sides? (Make sure your polygons have an isolate of >> design rule; e.g., with a design rule of 0.006 in, make the isolate 0.01 in).
  - Are your ground planes stitched together with vias?
  - Is your board as small as possible?
- Post-layout checklist
  - Turn on the 'tnames' layer (and 'bnames' if bottom silkscreen) and use 'smash' and 'size' to position component names until reasonably small and usable during component placement. Avoid placing text on pads and vias.
  - Verify that at least the board name, version number, and group number is on the 'tplace' layer for board identification.
- Final checkout
  - Print out 1:1 PCB and lay components on printout to double check packages **or** carefully verify package types between layout and component ordered.
  - Run DRC; there should be no un-approved errors.
  - Re-check approved errors for mis-approved errors.
  - Make sure all you either have all components in stock, or that components you specified are in stock before firing off board.