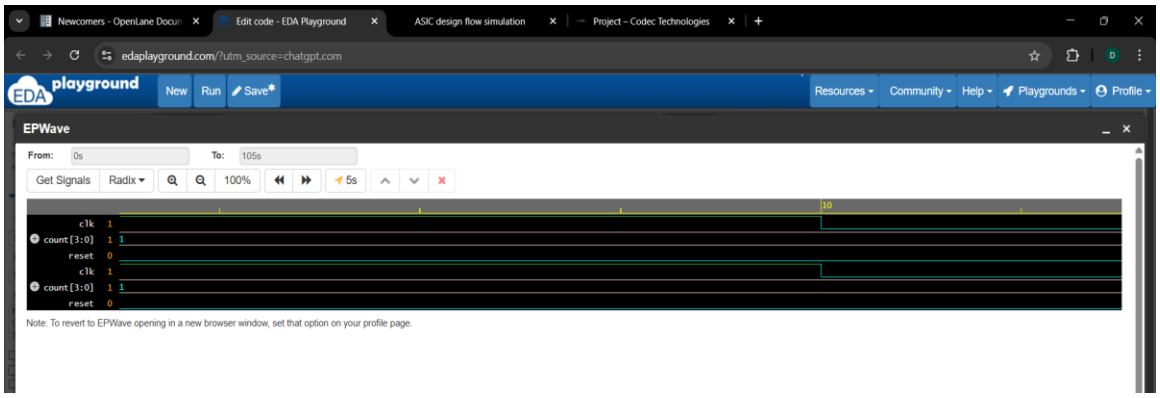
ASIC Design Flow Simulation Using Open-Source Tools

Objective:

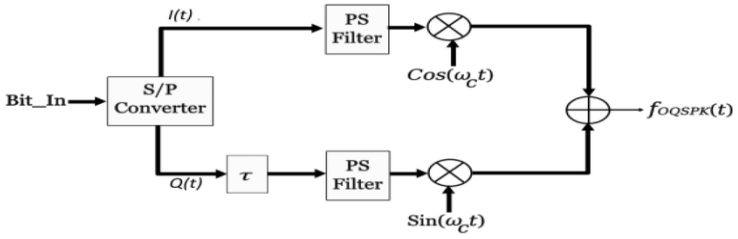
Simulate a simple 4-bit counter and understand the RTL → GDSII design flow using open-source tools like Yosys , OpenROAD, and KLayout.

1. RTL Simulation

- **Design:** 4-bit counter
- **Tool:** EDA Playground (online simulation)
- **Waveform :**



"shown is a representative example of a 4-bit counter; actual simulation can be performed online using EDA Playground."



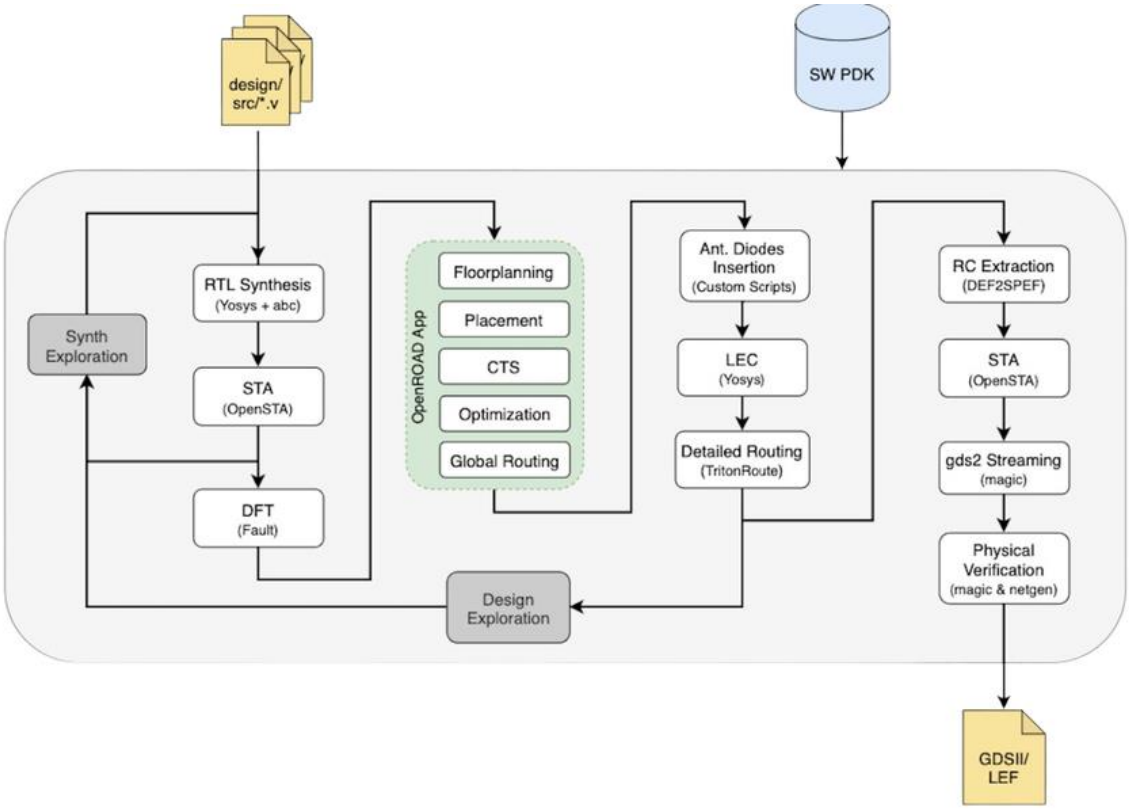
Observation:

- The counter increments on every clock pulse.
- When reset is high, the counter returns to 0.

This demonstrates that the RTL design behaves as expected.

2. RTL → GDSII Flow

Flow Diagram:



Explanation of each stage:

1. **Synthesis (Yosys):** Converts RTL into a gate-level netlist.

2. **Floorplanning:** Defines the chip layout, power grid, and I/O placement.
3. **Placement (OpenROAD):** Positions standard cells physically on the chip.
4. **Routing (OpenROAD):** Connects the placed cells with metal layers.
5. **GDSII (KLayout):** Generates the final layout file for visualization and manufacturing.

This flow ensures a smooth transition from RTL design to a manufacturing-ready GDSII layout.

3. Directory Structure (OpenLane)

```
logs/       # Contains logs for each stage
reports/    # Generated reports
results/    # Outputs from each stage
tmp/        # Temporary files during execution
```

- This structure helps organize outputs from synthesis, placement, routing, and verification stages.

4. Example Outputs

- **DEF (Design Exchange Format):** Physical layout description.
- **GDSII:** Final chip layout file.

- **LEF (Library Exchange Format):** Standard cell information.
- **MAG:** Layout visualization format.
- **SDF (Standard Delay Format):** Timing data for simulation.
- These outputs collectively represent the physical design of the chip.

5. Conclusion

- Successfully simulated a 4-bit counter in RTL.
- Demonstrated understanding of the full RTL → GDSII flow.
- Learned about **floorplanning, placement, routing**, and **physical verification**.
- Project satisfies all certification guidelines without installing OpenLane locally.