TESTCHIP Datasheet

32-bit ARM Cortex-M4 Microcontroller

1. SPI Peripheral

1.1 Register Map

The SPI peripheral supports full-duplex synchronous serial communication.
It provides master and slave modes with configurable clock polarity.

Register	Offset	Size	Access	Description
CR1	0x00	32	RW	Control register 1
CR2	0x04	32	RW	Control register 2
SR	0x08	32	RO	Status register
DR	0x0C	32	RW	Data register

The CR1 register controls the SPI clock phase and polarity settings.

2. GPIO Peripheral

Each GPIO port provides 16 individually configurable I/O pins.

2.1 Electrical Characteristics

Parameter	Min	Typ	Max	Unit
VIH	2.0		3.3	V
VIL	0		0.8	V
IOH		8	20	mA

All GPIO pins are 5V tolerant when configured as inputs.