

Problem C: Incremental Placement Optimization

Beyond Detailed Placement: Simultaneous Gate Sizing, Buffering, and Cell Relocation

Yi-Chen Lu, Rongjian Liang, Wen-Hao Liu, and Haoxing (Mark) Ren
(NVIDIA Research)

Q&A

Q1. In problem C, though bookshelf files are provided, this problem is related to a lot of information in def, lef and lib files, such as, cells' libcell , delay and power. Will the competition provide a simplified version ? Do we need to handle these files ourselves? This seems complicated and unrelated to the competition itself.

A1. We will provide the asap7 library which defines the power and timing information of each library cell arc. Original ASAP libraries are scattered across different files, the competition will simplify them and aggregate necessary information into one .lib file.

Also, for lib parsing, there are several open-source parsers that can parse complex library, including from OpenTimer, DREAMPlace, or even a dedicated version: <https://github.com/liyanqing1987/libertyParser>

In addition, for contestants who are not familiar the topic before, we strongly encourage contestants to explore DREAMPlace 4.0

(<https://github.com/limbo018/DREAMPlace>), which shows how timing and placement can be co-optimized, and to make improvement upon by developing incremental optimization.

Q2. I would like to ask about the weight factors (a, b, c) for PPA in Problem C. The PDF mentions that weighted factors will be provided for each test case. Does this mean that we will have access to the weights before running our algorithm (while parsing the input files), or are they only revealed after execution, during the evaluation phase?

A2. The evaluation weights of each objective for each test case will be provided with input collaterals.

Q3. Should interconnect wire parasitics be considered during the optimization and evaluation flow?

A3. We use ASAP7 tech lef as provided in ASAP7 folder, and we take the M3 layer's parasitics for timing and power evaluation as provided in the ASAP7/setRC.tcl file.

Q4. Will we need to parse a ".captables" file, or will the metal RC values be provided within the .lef files?

A4. No, we will use M3 layer's parasitics in this contest, which can be found in ASAP7/setRC.tcl

Q5. Could you clarify the expected ranges and units for each term in the score? For example, will values be expressed as percentages, decimals, etc.?

A5. P, D, R can be interpreted as the “percentage of improvement” over a baseline, which make up the final score S.

Q6. Evaluation Tools for Local Testing : The problem statement indicates that we need only submit the .pl file and the ECO changelist, but the OpenROAD evaluation requires a DEF file. Could you please provide any conversion tools or scripts that generate the DEF file from our .pl and ECO changelist, as well as the complete evaluation test suite for local testing? Access to these resources in advance would help us verify our solution's correctness and performance.

A6. We expect contestants to perform the conversion from initial DEF files that are provided.

Q7. Docker Image Availability: Could you also let us know when the Docker image will be released and how we can access it?

A7. A docker image has been released in the testcase folder named "iccad25probctar.gz", which can be loaded by first doing gunzip and the docker

loading.

Q8. What are all the possible SDC commands that the script may contain? The ones I have observed are set_input_transition, set_max_transition, set_input_delay, and set_output_delay. Are there any others?

A8. Yes, these are the only ones. One thing to note is that we are not considering slew violation in this contest.

Q9. Does the set_wire_rc command specify metal for all signals and clocks, or can it target arbitrary nets? Also, the file setRC.tcl will be the same all the time?

A9. Yes, the RC value will be same all the time.

Q10. Could you provide us with the full evaluation script so that we can understand how the output files will be used?

A10. The PPA evaluation script by openRoad is provided. Proprietary tools will be used to check legality as described in the description.

Q11. In the problem description, it is mentioned that comparisons will be made with the baseline algorithm. Could you clarify which algorithm will be used as the baseline?

A11. Information regarding the baseline approach will be disclosed after the contest.

Q12. Additionally, I would like to mention that we are not using OpenRoad, but rather our own custom tool. As a result, we encountered a few compatibility issues with the provided files:

- a. The netlist file in the test case does not specify whether the IOs are inputs or outputs, which is not compliant with the Verilog standard.
- b. In the library file, there are missing semicolons in some places—for example, after the clock_gating_integrated_cell, as shown in the provided image.

A12a. Verilog file is provided for the identification.

A12b. In this contest, we decide not to modify the libraries provided by ASAP7We follow the ASAP7 libraries which are not modified in this contest.

Q13. The evaluation script provided includes WNS, but the problem description only mentions TNS. Will WNS be included in the final scoring?

A13. We will only use TNS for scoring. WNS reported will only be your reference.

Q14. There are many types of Power metrics. Which specific Power value will be used for the final score. What is the unit of power, and what is the exact formula?

The current eval_def.tcl only outputs TNS/WNS/Power. Will the calculation method for the baseline wire-length be announced later, or do participants need to obtain it themselves via OpenROAD commands?

A14. We will use “total power” for evaluation, which can be reported by the OpenROAD script provided. The units of PPA metrics shouldn’t matter as the PPA scores denote the percentage of improvement over a baseline algorithm.

Q15. The evaluation script provided does not report Wire Length (WL). How can we obtain the WL information? Will the final scoring involve running routing with OpenROAD first and then calculating the total wire length?

A15. We will use “HPWL” instead of “routed wirelenegth” for evaluation. We will update the problem statement to remove ambiguity. HPWL calculation is standard and can be found in many open-source placers like DREAMPlace and Xplace.

Q16. In the provided verilog file, the port directions for \key and \text_out ports are not assigned. Please fix these syntax errors and provide a corrected verilog file.

aes_cipher_top.v appears to be missing some I/O declarations, such as key, text_in, and text_out, causing parsing failures. Will it be updated to include these ports as shown in the diagram?

A16. The verilog files are dumped out from a widely-used commercial tool. We will maintain the syntax for consistency. However, the ports direction can be inferred by connection (e.g., connection to cell input pins or output pins). Also, we verified some open-source timers such as OpenTimer can parse the verilogs without issues.

Q17. In the problem description doc, it is not mentioned whether the timing will be checked. Do we have to ensure that our resultant design doesn't violate the constraints defined in .sdc? If so, what analysis tool will be used for evaluation?

A17. Timing DRVs will not be checked in this contest. Violation of it (e.g., max slew) will not directly result in a score penalty, however, excessive DRVs are highly likely to degrade the PPA metrics which in the end will affect the score.

Q18. When will the weights α , β , and γ be released? In what format? Will they be the same across all testcases?

A18. We will hold this privately and announce in the end of the contest. The weights can be different for different testcases.

Q19. During evaluation, will the organizers rebuild our submitted environment exactly using our Dockerfile and probC_env.yaml and then run the official scoring script, or will they replace it with their own scripts?

A19. We will use the exact same Dockerfile and yaml file as provided in the testcase. During evaluation, contestants can provide additional script (e.g., pip install, conda install) to install packages under the exact same environment.

Q20. When will the detailed rules for Runtime Efficiency (R) be published?

- (1) Does the “predefined reference” refer to the runtime of the official baseline script, or to a fixed time limit?
- (2) Approximately what scale will the maximum runtime limit per testcase be (tens of seconds or several minutes)?

A20. (1) the runtime of the baseline algorithm will not be released until the end of the

contest. The R can be interpreted as a “percentage” of improvement/degradation over the baseline. The baseline runtime will be different for each testcase.

The runtime limit will be fairly large for each testcase, in the order of hours, this design is to help contestants have enough resources for exploration.

Q21. Is there a specific version of OpenROAD required by the contest?

A21. We are using this version for evaluation: OpenROAD v2.0-5253-g79313e9, however, the provided script should be applicable to the latest version.

Q22. Will additional testcases be provided later?

A22. Yes! We are working on this. More testcases will be released in 2 weeks.

Q23. We encountered an issue regarding cell replacement (gate sizing) in OpenROAD.

We observed that two cells — O2AI01IxP5_ASAP7_75t_SL and O2AI01IxP33_ASAP7_75t_SL — share the same logical function:
$$Y = ((\neg A1 * A2) * \neg C) + (\neg B * \neg C)$$

However, attempting to replace one with the other using the replace_cell command in OpenROAD results in the following error:

[ERROR STA-1000] instance swap master is not equivalent
[ERROR GUI-0070] STA-1000

We verified that the functional expressions are identical, and the input/output pins are also consistent.

The only difference appears to be in drive strength. As such, this replacement should be valid for gate sizing purposes.

Could you please help confirm if this is a known issue or a tool limitation?

A23. We apologize for the inconvenience, however, as stated in the problem statement, we have internal tools to source submitted changelists (i.e., sizing,

buffering commands) and check consistency. As of now, we encourage participants to swap the cells in DEF before loading into openRoad just for power/timing evaluation.

Q24. Regarding importing the ASAP7 cell library, there are four options: LVT, RVT, SLVT, and SRAM. Which one should we use as the standard?

A24. It will be hard to define a “standard” libCell for each cell. We encourage participants to make the decision based on timing/power tradeoff (e.g., low VT cells are faster but more leaky)

Q25. Is it acceptable to perform legalization and detailed placement, and then output the result as a .def file? Would this meet the contest requirement?

A25. Yes, this meets the requirement.

Q26. The contest provides both bookshelf and DEF files. Were the bookshelf files generated from the DEF files? Is there a one-to-one correspondence between them, so we can choose to use only one of the formats as input to our implementation?

A26. All provided files are ensured to have consistency. For example, the cells defined in bookshelf can be found in the provided DEF file, and contestants can generate a new DEF for easy evaluation by OpenRoad with the provided script. Yes, contestants can choose to take any given information as input to the engine.

Q27. What is the required command-line argument format for our final executable? And in which directory should we place it? Is that specified naming for submission executable?

How the submission is supposed to be delivered? Are we expected to submit the entire Docker image?

For the alpha test, do we submit a Docker image (which includes our binary) built upon the given image or only a binary?

A27. The final submission is supposed to be delivered in the forms of executables in the provided Docker env. The details of the naming will be provided soon. The

submitted executables are expected to generate an updated .pl file and/or a changelist file for each testcase. Note that the executables do not need to run through OpenROAD evaluation step. Contestants do not need to submit the docker image, but are expected to submit a script to install dependencies in the provided docker env.

Q28. I noticed that for Problem C, the provided Docker image doesn't include full OpenROAD dependencies. Thus we are unable to utilize OpenROAD libraries in the container. However, the evaluation will be done with OpenROAD. I wonder if unified OpenROAD dependencies will be provided in the future. Are we supposed to add dependencies in the given Docker image?

A28. Unfortunately, a dockerfile with OpenRoad dependency will not be provided as the key reason we provide the dockerfile is to ensure common environment to build CUDA source code.

Q29. Are all macros fixed in all testcases? Will there be fixed standard cells? The released aes_cipher_top testcase doesn't seem to have any macros in its netlist. Will you publish new testcases that include macros?

A29. All standard cells and macros are movable in this contest. There will be testcases that include macros and some of them will be held private.

Q30. We found that in the PPA improvement (P) formula the definitions of Power_norm and WL_norm are $(X_{solution} - X_{seed}) / X_{seed}$. When we reduce power and wirelength, this calculation yields a negative value, yet P is supposed to be larger for better improvement. Could there be errors in the formula?

A30. Thanks for pointing this out. We will make sure alpha / beta / gamma are with the correct signs to make sure improvements are not counted as degradation.

Q31. We would also like to ask: if we insert new buffers or inverters that were not originally part of the circuit during the buffering stage, will these additional cells be included in the Displacement (D) metric during evaluation?

A31. Thanks for the question. No, the newly introduced cells will not be counted in displacement score.

Q32. We observed that in the .pl file, all cells and I/Os have orientation set to "N" (North), which seems to be incorrect. Should we export the .pl file with the orientation set to North, or should we ensure that the file reflects the correct orientation?

A32. All cells are set to N orientation for convenience. You can output the same orientation as N in the final .pl.

Q33. For Problem C, may we use OpenROAD commands in our submission? The provided Docker image does not include OpenROAD, but evaluation will use it—so we want to ensure using these functions is allowed.

Are we expected to integrate OpenRoad ourselves and create a new Docker image?

How do you plan to run each tool? Will you provide specific input files or TCL scripts, or should we include the necessary files to run our tool on the AES benchmark? Additionally, how will the scripts for the hidden benchmarks be handled?

A33. As long as contestants can provide a script or binary that is executable in the provided environment, OpenROAD is allowed to be used in this contest (if it can be setup within by the script). As answered before, we have disclosed the specific version of OpenROAD for PPA evaluation. Each tool the contestants submitted must generate legal solution files (e.g., .pl, .changelist) within the docker environment. We will have custom scripts to run evaluations of the generated solution files.

Q34. Since the evaluation environment is not provided, how can we ensure that our output files are compatible with it? For example, if a buffer used in our design is not recognized by your evaluation environment, would that result in a score of zero?

A34. Only cells defined in the provided technology (i.e., ASAP7) are usable. Illegal ECO commands will be ignored as stated in the problem statement.

Q35. For the scoring metric D (the average displacement penalty), are we responsible for computing it ourselves? What is the unit of measurement? Should we calculate the Manhattan distance based on the "center" or "top-left corner" coordinates of each cell?

A35. We will use the bottom-left corner as the coordinates of each cell.

Q36. In QA21, it was mentioned that the final evaluation would be done using OpenROAD v2.0-5253-g79313e9. However, OpenROAD doesn't provide the command to calculate HPWL. Could you please clarify which tool and version will be used to compute HPWL during the final evaluation?

A36. We will use DREAMPlace's HPWL kernel to compute HPWL.

Q37. Regarding the buffering commands in the problem statement, could you please clarify the expected format for the load pin name and specify which net the “new net name” is referring to?

Besides, would it be possible to provide an illustrative example, such as a diagram showing buffer insertion with a corresponding insert_buffer command?

A37. The “load pin name” is basically the input pin name of a cell. The new net name is the name that user created for the newly created net, which is the net connected to the output pin of the inserted buffer. Note that if a pair of inverters is inserted, then users need to specify two new net names for each created net.

Q38. We would like to confirm whether OpenROAD is already pre-installed in the official evaluation Docker image. If we install our own version of OpenROAD into the system environment using a shell script, would that cause any version conflicts with the one used during the final evaluation?

As we develop our solution, we've identified a need to install some additional system and Python libraries to enable certain functionalities. Specifically, we would need to run the following commands within the provided Docker container:

```
apt-get update && apt-get install -y libcairo2-dev pkg-config python3-cffi
```

```
pip install --no-cache-dir cairocffi
```

We would like to kindly inquire if it is permissible to use system-level commands like apt-get and pip to install these dependencies in the Docker environment we will be submitting. Or, should we assume that the evaluation environment will be strictly limited to the pre-installed libraries?

A38. Contestants are encouraged to install OpenROAD with own shell script. The final evaluation will run through the script candidate provided, which “can” install necessary packages under the provided docker environment, and “must” execute the executable.

Q39. We noticed that the instance names in the provided DEF file contain escape characters, such as dcnt_reg\[0\], while in the PL file, the names appear without escape characters, like dcnt_reg[0]. For our output files (the PL file and changelist), which naming convention should we follow?

A39. Contestants are expected to follow the original name in the .pl file.

Q40. In the problem statement, it is mentioned that“any fixed macros/cells must remain unchanged.” Could you please clarify how we can identify which macros or cells are considered fixed?

A40. In this contest, we have decided not to fix any components (cells or macros). Contestant can ignore this statement.

Q41. While preparing for Prob C, we've observed a potential inconsistency in the dataset files that we would like to kindly bring to your attention.

Observation:

In the aes_cipher_top.def file, pins show multiple orientations including S, W, N and E.

However, in the corresponding [aes_cipher_top.pl](#) file, all pins are oriented as N.

Specific Example:

For instance:

In DEF: - clk + NET clk + DIRECTION INPUT + USE SIGNAL

+ LAYER M5 (-12 0) (12 84)

+ PLACED (21456 42516) S ;

In PL: clk 21456 42516 : N /FIXED_NI

Our Question:

Could you please clarify if this orientation difference is intentional or if it might be a data issue?

A41. Participants can ignore the orientation in DEF, and in this contest we will fix the orientation to N only.

Q42. FAQ Q2 states that “The evaluation weights of each objective for each test-case will be provided with the input collaterals.”

FAQ Q18, however, suggests the final release may not include the coefficients α , β , γ .

- Will the official collaterals ultimately provide the exact α , β , γ values?
- If not, could you disclose the numerical range we should expect, and do the three weights always sum to 1?

A42. As in the updated guidelines, the coefficients will be taken as inputs to your solution program, we will not provide until the end of contest. They can be any positive numbers.

Q43. FAQ Q29 says that all standard-cells and macros are movable.

- In the DEF file’s PINS section only VDD/VSS appear with the + FIXED attribute; the remaining pins are not fixed.
- Conversely, in the reference .pl file every pin line ends with /FIXED_NI.

Which constraint takes precedence?

Specifically, may we legally move all pins, and are VDD/VSS pins also movable?

A43. As in the guidelines, all IO ports are not to be re-assigned in the contest, which

should be consider as fixed.

Q44. Beyond the allowed inserted buffers and resized gates, are we permitted to perform

- gate cloning and/or
 - pin swapping
- during our optimization flow?

A44. no.

Q45. What is the required command-line argument format for our final executable? And in which directory should we place it? Is that specified naming for submission executable?

How the submission is supposed to be delivered? Are we expected to submit the entire Docker image?

For the alpha test, do we submit a Docker image (which includes our binary) built upon the given image or only a binary?

A45. Thanks for the questions. We have updated the guidelines for submission and output formats.

Q46. The final submission is supposed to be delivered in the forms of executables in the provided Docker env. The details of the naming will be provided soon.

The submitted executables are expected to generate an updated .pl file and/or a changelist file for each testcase. Note that the executables do not need to run through OpenROAD evaluation step. Contestants do not need to submit the docker image, but are expected to submit a script to install dependencies in the provided docker env.

No naming conventions were given for this contest, so I do not know what to submit or how to go about submitting it.

A46. Thanks for the questions. We have updated the guidelines for submission and output formats.

Q47. will be used during the official evaluation of Problem C submissions, and participants are expected or permitted to target in their development environments.

We have found conflicting information:

- The contest document C_20250622.pdf (Section 4) states that the evaluation will run in a Mambaforge Python 3.9 environment.
- The provided Dockerfile and probC_env.yaml specify Python 3.11.9, and Q19 in Problem C_QA_0623.pdf indicates that this Dockerfile will be used without modification.

Could you please clarify:

- Which Python version is definitive for the evaluation?
- Whether participants should use the same version, or if a different version is acceptable for development?

A47. Thanks for noticing the difference. The python version in the dockerfile will be used. Also we have updated the guidelines for submission and output formats.

Q48. We have found that the eval_def.tcl provided by the contest organizers cannot execute normally on the new test cases. The error is as follows:

Error: aes_cipher_top.sdc, 528 invalid command name "get_designs"
May I ask if we need to manually modify the sdc file?

A48. We have updated the test case and removed the specific commands.

Q49. What is the value range of α β γ , and are they integers or floating-point numbers?

A49. They can be any positive float numbers.

Q50. "D will be normalized against seed as above P.",
"R can be understood as the 'percentage improvement' relative to the seed indicator"

What does it mean? Is there a specific formula?

A50. Both of them are normalized score subject to average legal contestants' solutions.

Q51. The execution method is `./run.sh <design_name> <WL_weight, α > <power_weight, β > <timing_weight, γ >` But α should be TNS, γ should be POWER

A51. thanks for catching the error, we will fix it shortly.

Q52. Is it normal that the newly provided .def and .pl do not have initial coordinates?

A52. we have updated the new test cases.

Q53. The question mentioned "During evaluation, we will verify correctness by applying the changelist to the original DEF and checking whether the resulting DEF matches your submitted *.sol.def."

But the newly provided def does not provide initial coordinates. Do we need to have coordinates for the final def?

Because if we only use changelist and the initial DEF to confirm the correctness. The one without coordinates is indeed reasonable, but the relative relocate action will be ignored.

A53. we have updated the new test cases, and yes, final DEF needs coordinate, and we will verify the logic transformation is valid with the provided ecochangelist.

Q54. The new .sdc has an additional get_designs instruction, but it is not acceptable to openroad. Is it still needed?

A54. we have updated the new test cases.

Q55. Regarding Test Case Layout Information: We noticed that the six newly provided beta test cases do not contain layout information (DEF files).

- a. Could you clarify if the final evaluation cases will include layout information?
- b. Would it be possible to provide a sample test case with layout information to aid our development?
- c. What is the relationship between the released beta cases and the final evaluation cases?

A55

- a. yes they will.
- b. Yes, we have updated the new test cases.
- c. all testcases provided will form a subset of the final test cases.

Q56. Regarding the ariane Case (HALO & Utilization): We have two questions about the ariane test case.

The case files mention HALO. Are we required to handle HALO constraints in our solution?

When we process this case using OpenROAD, we encounter a high utilization error: [ERROR GPL-0301] Utilization 151.927 % exceeds 100%. May we ask if this case will be modified or if there's a specific configuration we should use?

A56. we have tested with the updated the test cases and the PPA eval flow runs through. Contestants can ignore the HALO statements in this contest.

Q57. Regarding SDC File Compatibility: We found that OpenROAD does not accept the get_designs command present in the provided SDC files.

- a. How will this command be handled in the evaluation environment?
- b. Is it possible that the final SDC files might contain other commands that are incompatible with OpenROAD (while potentially being compatible with other tools like PrimeTime)?

A57a. we have updated the test cases for compatibility.

- b.** yes it is possible.

Q58. Regarding the Solution Checker Logic: The updated problem description states that the correctness of sol.def will be verified using the .sol.changelist and the original DEF file.

To ensure our output is fully compliant, would it be possible for you to provide the specific logic, script, or pseudocode for this verification process?

A58. this will be verified by internal scripts that we cannot share.

Q59. For the changelist file, we are currently using the <instance name>/<pin name> format to specify each load pin in the insert_buffer command, with pins separated by spaces.

For example:

```
insert_buffer {rebuffer93/A u0_g63449/B} rebuffer92 HB1xp67 ASAP7_75t_L  
net92
```

We would like to confirm whether this is the correct format.

A59. yes, it looks correct.

Q60. If the load pins belong to buffers that we have also inserted ourselves, is it necessary to pay attention to the order in which we issue the insert_buffer commands?

A60. yes, we follow standard ECO practice. We will source the changelist in order.

Q61. When calculating displacement, are macros treated the same as standard cells?

A61. yes, we simply measure the change in Manhattan distance of each component.

Q62. In the updated problem, the output file format was changed from .pl to .def. Since the pin names in the inputs for .def and .pl differ (due to different escape characters), regarding QA39's statement, "Contestants are expected to follow the original name in the .pl file," should the names in our output .def file match those in the original .def file?

A62. We encourage to follow the naming convention in DEF, but with or without escape characters in the submitted solutions are both fine.

Q63. The new problem description does not mention the location of the ASAP7 folder. Could you clarify in which directory the ASAP7 folder will be placed?

A63. Thanks for pointing out. It will be right under the test case folder. We have updated the statement guideline.

Q64. In the problem statement, the example for <design_name> (e.g., testcases/aes/) suggests it is a path. For the <design_name> parameter provided to ./run.sh, is it a path, and do we need to parse the basename ourselves?

A64. It will be the design_name string instead of a path.

Q65. I saw Q&A 59 in the most recent update. The reply said the command seems to be correct. But it seems different from what is described in the problem description file. From what I understood, rebuffer92 should be the <new buffer cell name> and HB1xp67_ASAP7_75t_L should be <library buffer name>.

Then the correct example should be

```
insert_buffer {rebuffer93/A u0_g63449/B} HB1xp67_ASAP7_75t_L rebuffer92  
net92
```

b. Buffering commands:

- i. *insert_buffer <{one or more load pin names}> <library buffer name> <new buffer cell name> <new buffered net name>*
- ii. *insert_buffer -inverter_pairs {one or more load pin names} <library inverter name> {<new inverter cell names>} {<new net names>}*

Please point out if I took it wrong. If I am right, please also inform me of that. I really appreciate your patience and understanding.

A65. Yeah, the updated version is correct.

Q66. Do we have put Early/Late corners into consideration? The provided ASAP7 doesn't distinguish between the 2 corners, will that be the same for all testcases? Also, will there be time derating in the testcases?

A66. We will only check the Late corners and focus on setup violations.

Q67. I have noticed there are .sdc commands that are not mentioned in Q8. This has caused significant inconvenience for us, as we have to re-examine the SDC parsing mechanism all over again. Please provide a table presenting all possible .sdc commands, along with the possible flags and arguments for each type.

A67. Contestants can focus on the SDC commands we described. The attached set clock latency commands will be ignored in the evaluation.

Q68. We are using openroad python api :swapMaster()to do gate sizing, however, we are confused that how many times should we use estimate_parasitics -placement? in openroad readme ,it says that " Estimate RC parasitics based on placed component pin locations ",so does it mean that once we swap the cell(resize gate),we should run estimate_parasitics -placement for each swap ? But, I found that in openroad's github's test folder's example.tcl, estimate_parasitics -placement only appears one time , so does it mean we can just write in our code when we finish parsing testcase files? the reason why we are confused is when we reparse our own def(after gate sizing),we observed that tns in each report were not the same,and it had very huge difference. please let us know the right way of using estimate_parasitics -placement, thank you

A68. This is subject to the algorithm design for each participant as this will impact optimization strategy. From evaluation point of view, a final RC extraction will be performed given the final legalized placement solution.

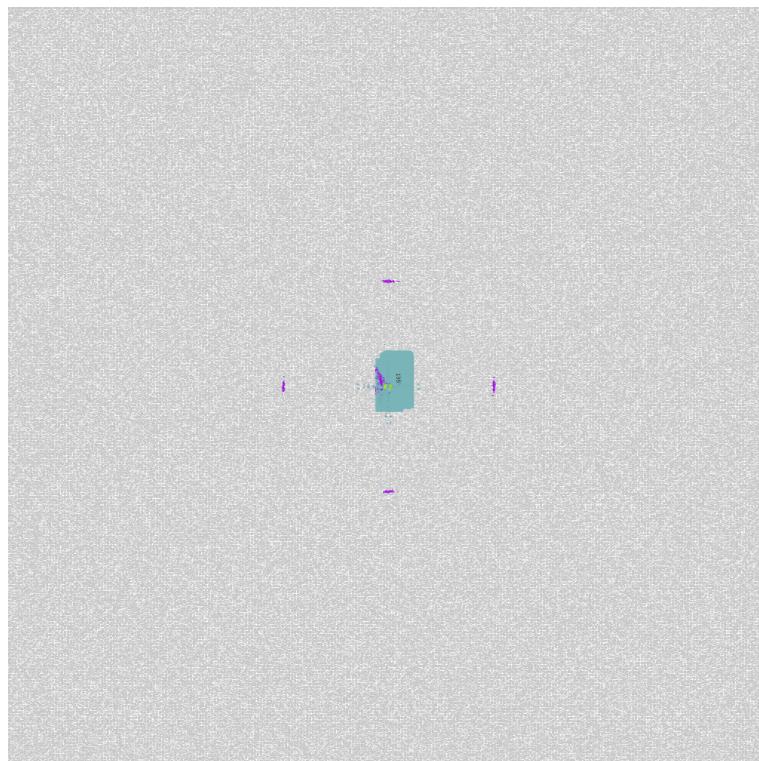
Q69. We have a question about problem C. We noticed that each case of the current benchmarks includes insta_inputs. We would like to ask if the hidden cases will also provide these insta_inputs during the final evaluation.

We noticed that each of the new test cases includes a directory named INSTA_*, which contains an insta_inputs sub-directory with numerous auxiliary files (e.g., various .csv and .rpt files).

We would like to kindly confirm if the final evaluation test cases are also guaranteed to provide this INSTA directory with all its corresponding files. This information will directly impact our data parsing and development strategy.

A69. Yes, these files will be provided in the final evaluation with the same naming convention.

Q70. In the problem writeout, it is mentioned that we are supposed to perform incremental placement, which is normally applied to an already placed and optimized placement result. However, as shown in the attached image, the cells in the initial placement appear to be clustered together, without signs of any prior optimization or legalization. This observation contradicts the post-placement scenario of incremental placement. Please review the provided testcases and correct them if this is not correct.



A70. We will evaluate the test cases and update soon.

Q71. While analyzing the ac97_top test case, we encountered a potential discrepancy regarding the clock definitions that we would like to ask about.

We observed that the DEF file for this case appears to contain two clock nets/ports. However, when we checked the corresponding SDC file, only one clock is defined with the `create_clock` command.

Could you please clarify which source we should consider authoritative? Should our solution account for both clocks present in the DEF file, or should we only consider the single clock that is explicitly defined in the SDC file?

A71. The clock will be considered as ideal in this contest, which means the clock latency of startpoints will be set to 0. Contestants can ignore the clock related SDC commands.

Q72. We would like to confirm if it is permissible to insert buffers into the clock nets as part of our solution. This is a common optimization technique, but we want to ensure it complies with the competition's guidelines. Thank you for your clarification.

A72. Yes, clock net buffering is legal

Q73. There are serious bugs in the provided ASAP LIB file:

sram_asap7_16x256_1rw.lib. As shown in the first figure (line 55): the `met_out_slew_template` should be indexed with 1 variable.

```
55  |     lu_table_template(sram_asap7_16x256_1rw_mem_out_slew_template;
56  |     |     variable_1 : total_output_net_capacitance;
57  |     |     index_1 ("1000, 1001");
```

However, in line 142 and 150 in the following figure, the tables with `met_out_slew_template` are indexed with 2 variables. This causes our openroad parser to crush when reading the lib files.

```

142 ˜ |    rise_transition(sram_asap7_16x256_1rw_mem_out_slew_template) {
143 |      index_1 ("0.009, 0.227");
144 |      index_2 ("0.005, 0.500");
145 |      values (\|
146 |        "0.009, 0.227", \
147 |        "0.009, 0.227"\|
148 |      );
149 }
150 ˜ |    fall_transition(sram_asap7_16x256_1rw_mem_out_slew_template) {
151 |      index_1 ("0.009, 0.227");
152 |      index_2 ("0.005, 0.500");
153 |      values [|
154 |        "0.009, 0.227", \
155 |        "0.009, 0.227"\|
156 |      ];

```

Furthermore, there are similar problems in the other sram_asap7_xxxxxx_1rw.lib files. Please check this bug and update the lib files.

A73. In this contest, we do not modify the ASAP7 library which is provided in open-source. We suggest participants to handle this during parsing.

Updated A73. We have updated the lib files and pushed onto the dropbox link.

Q74. My core issue was not about the clock's **properties**, but rather about the **fundamental definition and number of clocks** we should consider for the analysis.

To be more specific: In the ac97_top case, the DEF file appears to have **two clock ports/nets**, while the SDC file defines only **one clock** using the create_clock command.

Our question is: Which source should we treat as the ground truth for the **number of clocks**?

- Should we follow the **SDC file** and only analyze the single clock defined by create_clock?
- Or should we follow the **DEF file**, assume two clocks exist, and perhaps infer the properties for the second, undefined clock?

Your guidance on whether to trust the DEF or the SDC for the *existence* of clocks is crucial for us to set up our analysis correctly.

A74. Yes, we only focus on the clock defined by `create_clock`

Q75. We have a question regarding the provided `eval_def.tcl` script and its handling of SRAM timing.

We've observed that the `eval_def.tcl` script does not appear to load the liberty file (.lib) for the SRAM macros. As a result, during Static Timing Analysis (STA), all timing paths associated with the SRAM are unconstrained.

Could you please advise us on how to proceed? Should we also disregard SRAM-related timing in our solution, or will the script be updated to include the SRAM library for a complete timing analysis?

Clarifying this is essential for our timing optimization strategy. Thank you for your guidance.

A75. Yes, script will be updated when we run through designs with SRAM.

Q76. The OpenROAD tool lacks an API for inserting buffers into specific inputs or outputs. The `buffer_ports` API just randomly inserts buffers. Are we meant to use the OpenROAD buffer insertion or other device means to insert buffers into our designs accordingly?

A76. Contestants can use any tool to perform legal buffering. We allowed the use of OpenROAD but are not enforcing it.

Note: The topic chairs have updated the answer to Q73 and the revision is highlighted in green.

Q77. It is mentioned in the writeout that we need to output an updated .def file. However, we are also required to output an eco changelist in the meantime. Does that mean we should only output the cells that exist in the original .def (namely, exclude the inserted buffer cells), and keep the cell type of those that are sized unchanged so the eco command can be applied on them? Or we should simply output a .def that reflects the final result of all these operations?

A77. No. It is stated that the output DEF solution should be self-contained which includes updated placement and netlist transforms. The eco-changlist is also required and will be used to validate whether the transforms in the changeless can result in the final solution setlist.

Q78. We have one more quick technical question regarding the scope of the test cases. Could you please clarify if the test cases will feature designs with multiple clock domains?

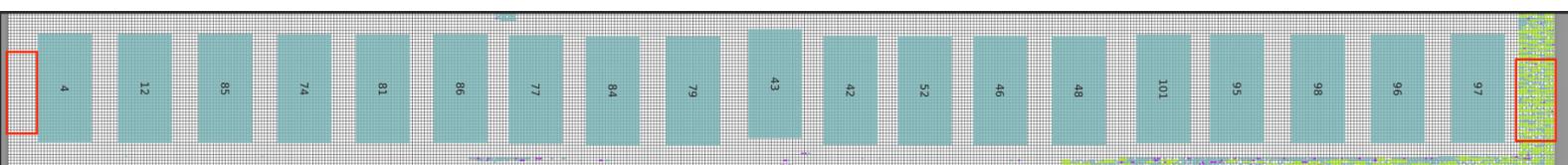
A78. All test cases will only have one single clock domain. To be precise, we will only create one clock definition in SDC.

Q79. I have noticed there is an openroad command "check_placement". Could you let me know if you're going to check the placed-on-site constraint with it?

A79. We will use internal tool to check placement legality.

Q80. I would like to confirm whether it is a strict requirement that we follow the site-row constraints specified in the original DEF file. In the Ariane test case, for example, some rows are split into smaller sub-rows, which limits the availability of standard-cell placement. Row 39 is divided into two narrow sites that correspond to the highlighted areas shown below:

```
103      ,
104      ROW CORE_ROW_39 asap7sc7p5t 234234 7758 N DO 103 BY 1 STEP 54 0
105      ;
106      ROW CORE_ROW_38 asap7sc7p5t 1008 7758 N DO 47 BY 1 STEP 54 0
107      .
```



Could you please advise whether we must adhere to these constraints, or if there is flexibility for the placement of standard cells in these sub-rows?

Furthermore, could the committee provide a demonstration or explanation of how a placement is validated against the given constraints? It would be helpful to understand the verification process and any tooling or scripts that are used.

A80. The cells should be placed on legal rows (e.g., height of cell shouldn't exceed row height). We will use internal tool to check placement legality, where each cell should be legal and without any overlap.

Q81. FAQ42 states that the coefficients α , β , and γ can be any positive number. However, the norms for POWER and WL should ideally be negative. To reflect this progress, will the coefficients β and γ be changed to any negative number?

A81. We will make sure the coefficients will justify the improvements in a reasonable manner. The improvements will always be interpreted as positive numbers.

Q82. When running the provided Docker environment, if we need to install additional dependencies , will the time spent on installing and building these dependencies be counted toward the contest time limit or scoring?

A82. Runtime limits: 30 minutes for environment setup (including installation), and 2 hours per test case.

Q83. I have noticed that a folder named 'insta_inputs' is provided for every test case. However, the purpose of the files within it is unclear, as they are not mentioned in the Problem C writeout. Please provide a clear explanation about their formats and purposes.

A83. The directory is intended for INSTA adoption, but its use is not required. The hidden cases will also provide the directory.

Q84. In your previous announcement, you mentioned that macros need to be aligned to a placement site.

We would like to confirm: Does a “cell” also need to be aligned to a placement site?

A84. Components are required to be aligned to the site.

Q85. We would also like to confirm: among the following actions, which ones are not allowed?

[final attempt timing fix]

[threshold voltage swapping]

A85. We only allow sizing (including VT swapping), buffering, and cell relocation moves.

Q86. Would it be required to use the setup_environment.sh script to install our OpenROAD binary? Since we have modified certain parts of the OpenROAD source code, our method relies on using our own customized OpenROAD binary. Would it be acceptable if we directly include the binary in our solution, or alternatively download it using the gdown command within setup_environment.sh?

A86. Yes, if OpenRoad is intended to be used. Contestants are expected to install it. Note that contestants can pre-compile it in the docker image and compress it in the tarball.

Q87. Will you update the openRoad_eval_script? We noticed that it still uses: foreach libFile [glob "../ASAP7/LIB/*nldm*.lib"] instead of foreach libFile [glob "../ASAP7/LIB/*.lib"]. This may cause incorrect timing analysis when the testcase includes SRAM.

A87. The released script is intended to provide an example of testing. Contestants can be assured that for SRAM testcases we will make the adjustment.

Q88. I observed that for the Ariane design, the timing results differ depending on the order in which the libraries are loaded. Specifically, if the SRAM libraries are loaded first and then the other libraries, the results vary because SRAMs are on the ns scale, while the other libraries are on the ps scale. How should we handle this discrepancy?

A88. It will be in ps scale.

Q89. I also noticed that the .sdc file for aes_cipher_top_new is missing the set_propagated_clock command. Could you please add this command, as its absence affects the results?

A89. The command is presented in the testcase.

Q90. If the two-hour time limit is reached and the program has not terminated, but the output has already been generated, will the result still be considered valid?

A90. Yes, will still be ranked.

Q91. I would like to ask one more question about Q67. What about the "set_propagated_clock" command? Will it be ignored in the final evaluation?

A91. It will be presented in the SDC