Integrated Systems Architectures

Lab 1: design and implementation of a digital filter Assignment

Read the Lab 1 description and address the following points.

1 Reference model development

- Design the filter with Matlab/Octave.
- Develop the fixed point model as a C program.
- Compare and comment the results.

2 VLSI implementation

- Develop the VHDL model of the filter and verify it with e proper testbench.
- Peform the logic synthesis $\rightarrow$ find the maximum clock frequency at which the design can correctly run. Then, find the area.
- Set $f_{clk} = f_M/4$, find the area, verify the design and estimate the power consumption.
- Place & Route the design at $f_{clk} = f_M/4$, find the area, verify the design and estimate the power consumption.

3 Advanced architecture development

Repeat all the step in 2