



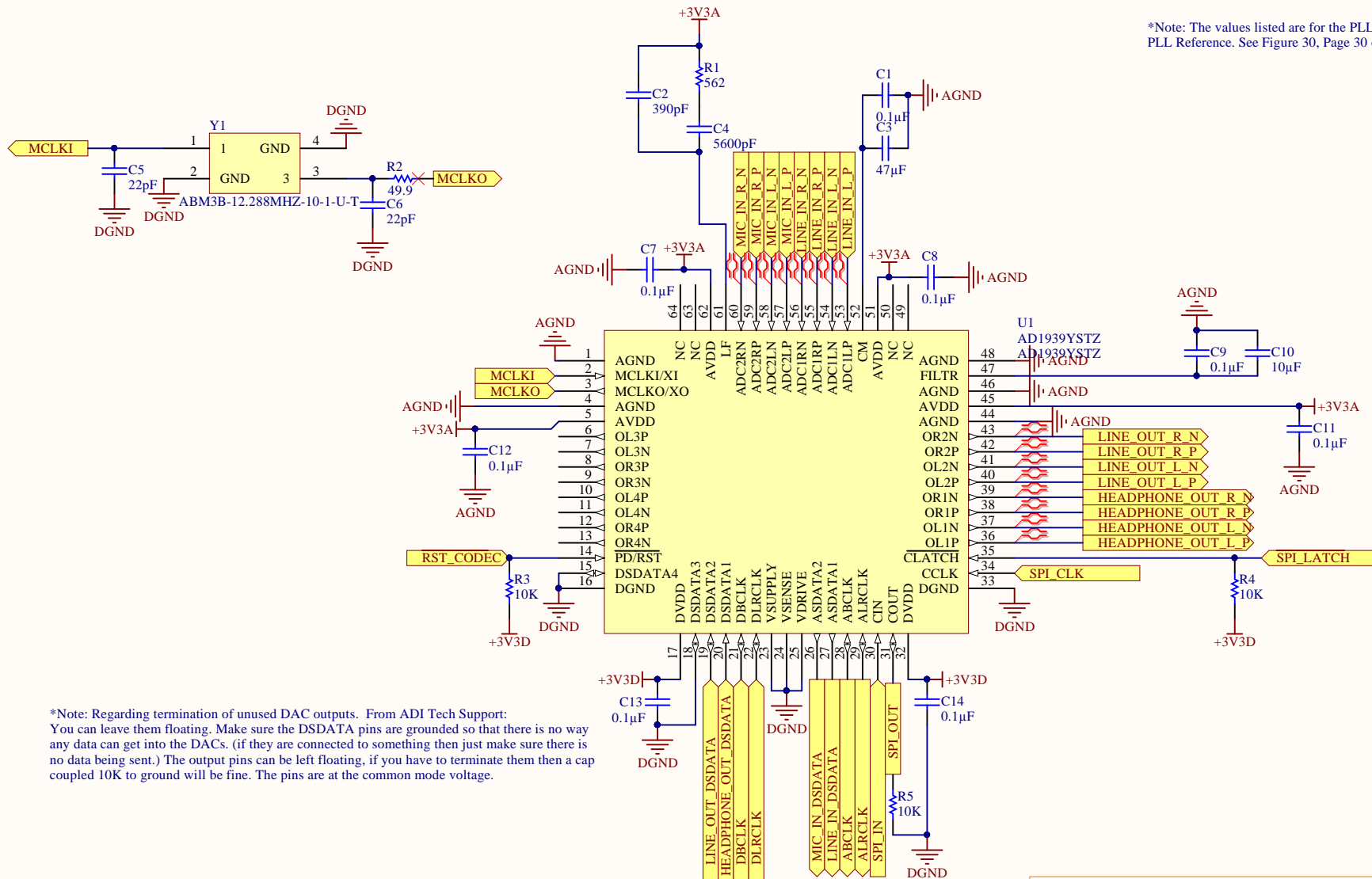
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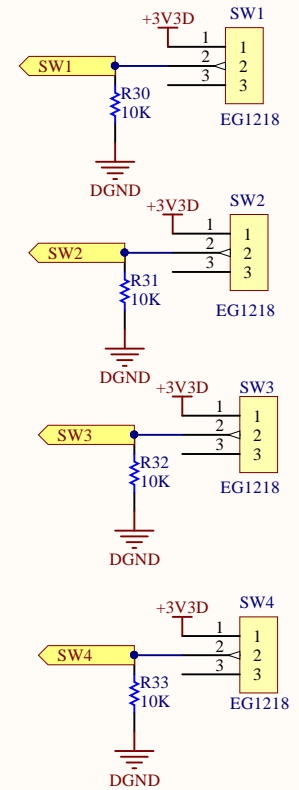
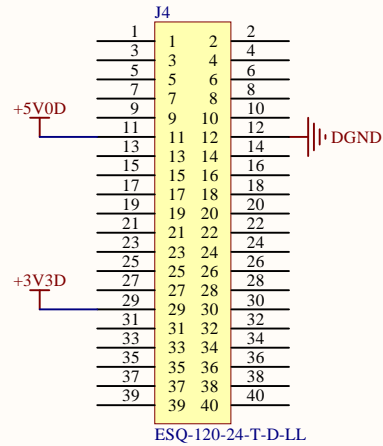
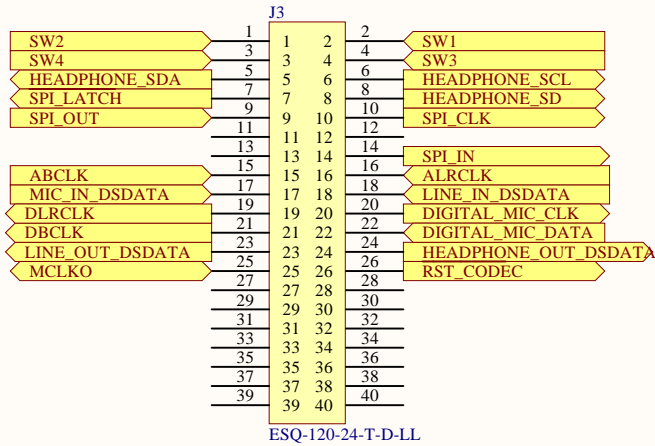
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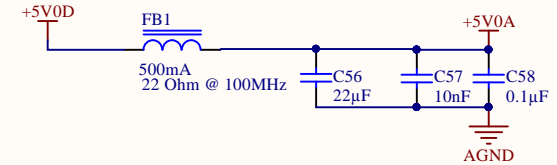
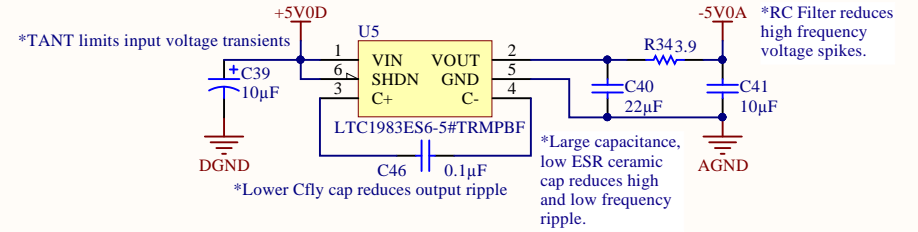
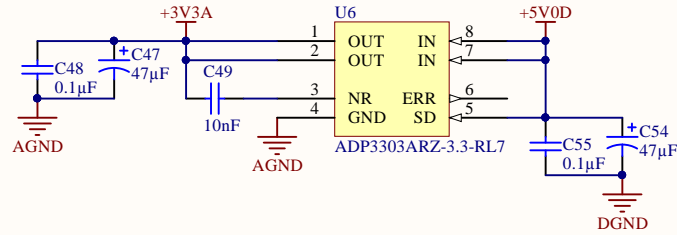
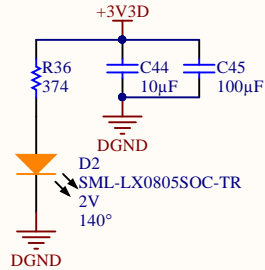
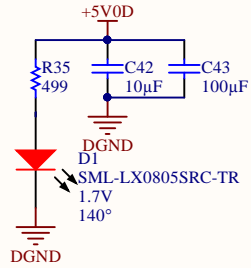



\*Note: The values listed are for the PLL Loop Filter for the MCLK PLL Reference. See Figure 30, Page 30 of the AD1939 Data Sheet.

\*Note: Regarding termination of unused DAC outputs. From ADI Tech Support: You can leave them floating. Make sure the DSDATA pins are grounded so that there is no way any data can get into the DACs. (if they are connected to something then just make sure there is no data being sent.) The output pins can be left floating, if you have to terminate them then a cap coupled 10K to ground will be fine. The pins are at the common mode voltage.

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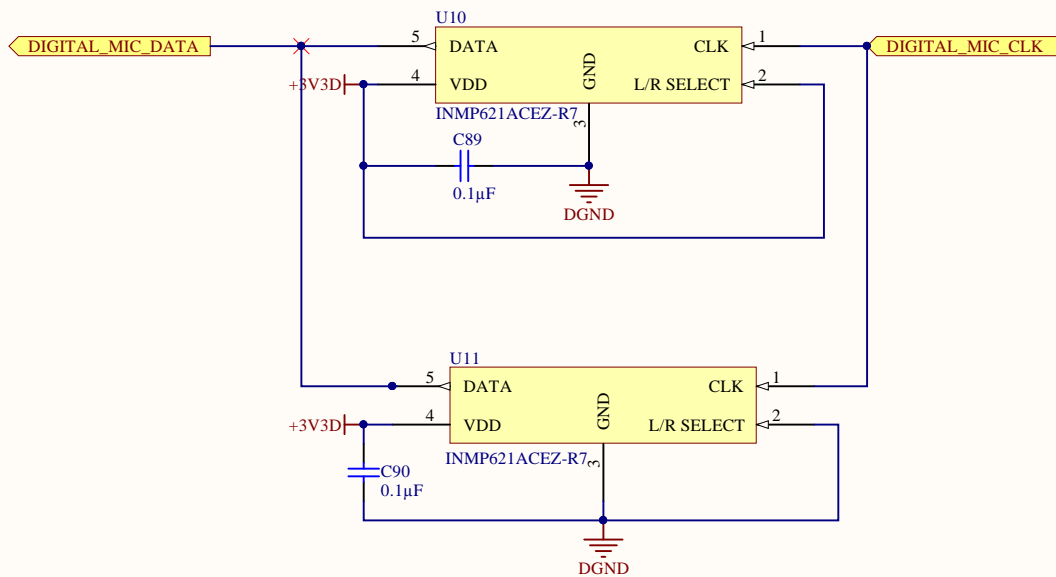




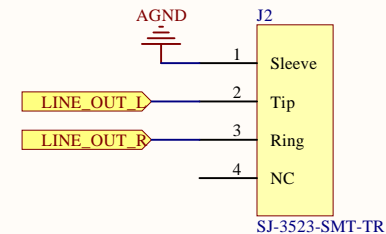
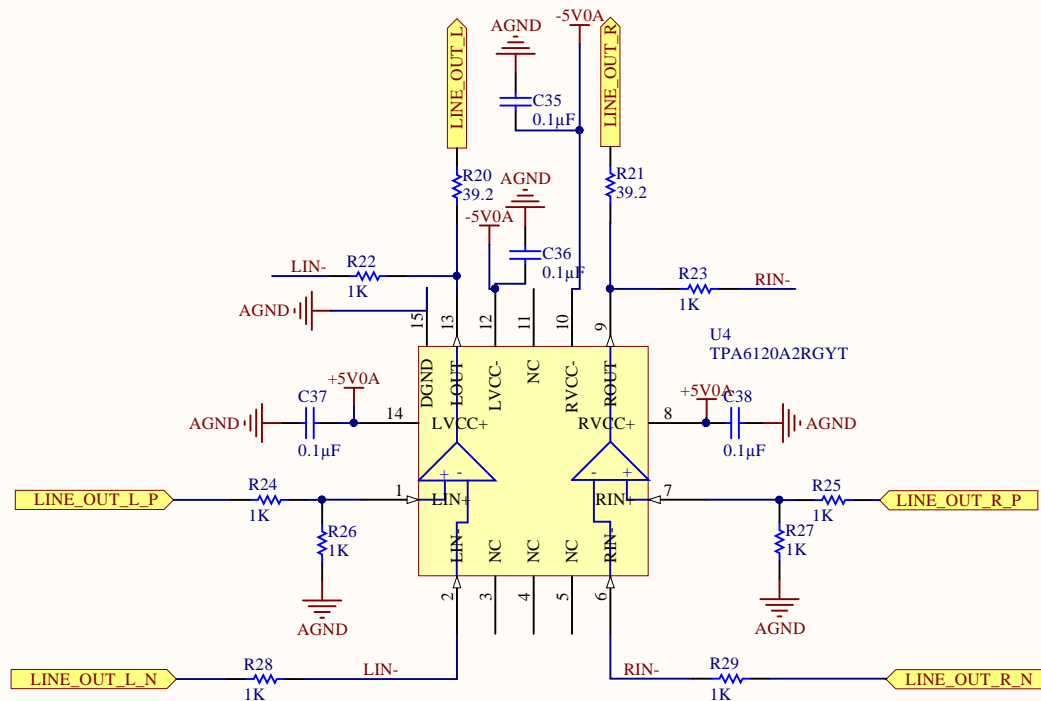
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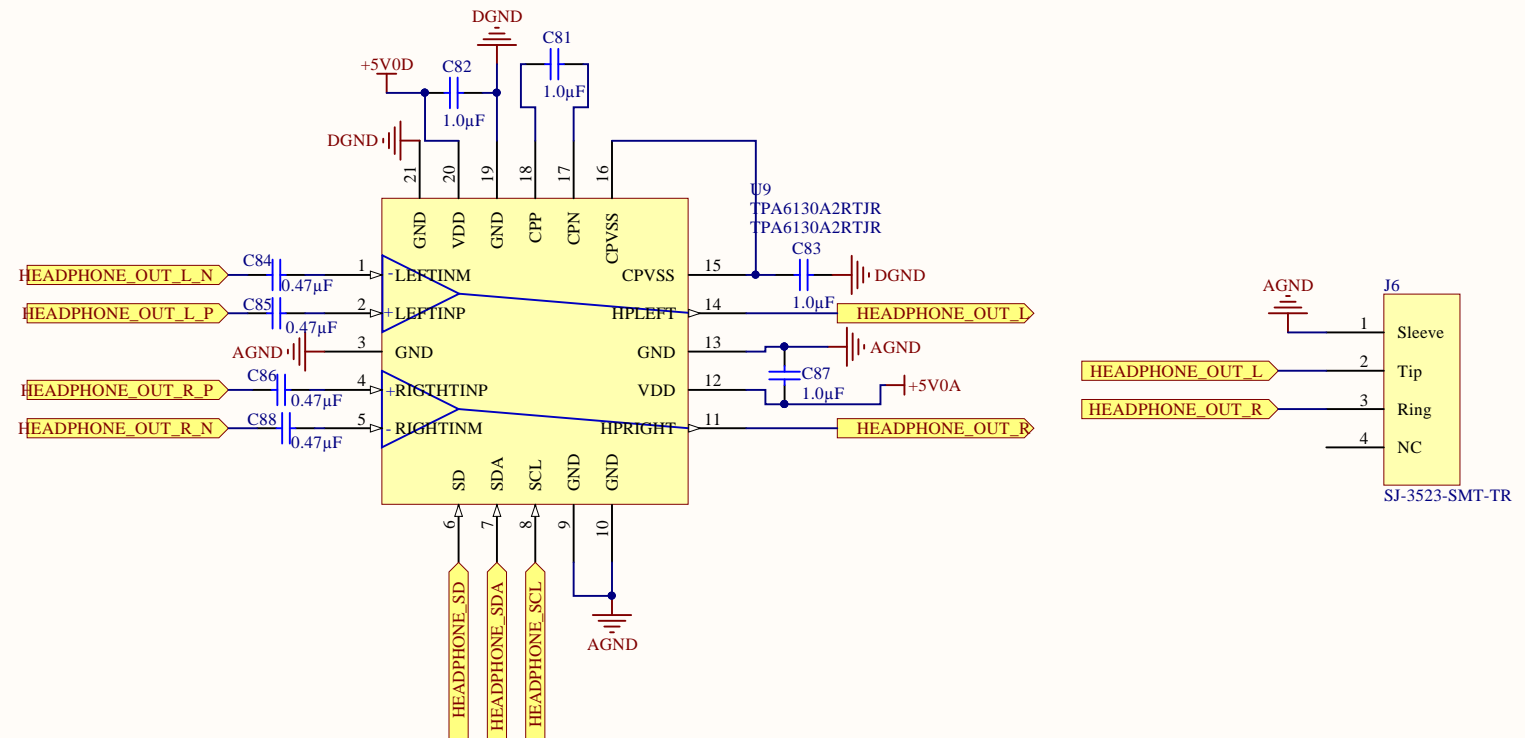



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