- 一、名词解释题(本大题共7小题,每小题3分,共21分)。提示:解释每小题所给名词的含义,若解释正确则给分,若解释错误则无分,若解释不准确或不全面,则酌情扣分。
- 1. Name the three basic components of every computer.
- 2. Describe how an interrupt works and name four different types interrupt at least.
- 3. What is the difference between synchronous buses and nonsynchronous buses?
- 4. Explain the differences between data buses, address buses, and control buses?
- 5. What is an address mode? List five types of address mode.
- 6. What are the advantages and disadvantages of fixed-length and variable-length instructions? Which is currently more popular?
- 7. Explain the concept of pipelining.

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1. the main functions of the CPU is
2. What unit is typically used to measure the speed of a computer clock
3. Virtual memory can be implemented with different techniques, including:
4. List the three fields in a set associative cache address,
5. Given a memory of 2048 bytes consisting of several 32 Byte × 8 RAM chips, and assuming byte-addressable memory, the correct way is usingbits for chip select andbits for address on chip.

三、判断改错题(本大题共5小题,每小题2分,共10分)

提示: 正确打√, 错误打x, 将其结果填写在下表中。

- 1. The Principle of Equivalence of Hardware and Software says that hardware and software are basically equivalent, and implementations done via either method will run at the same speeds.
- 2. Amdahl's Law states that the performance enhancement possible with a given improvement is limited by the amount that the improved feature is used.
- 3. Registers are storage locations within the CPU itself.
- 4. MARIE has a common bus scheme, which means a number of entities share the bus...
- 5. A fixed length instruction must have a fixed length opcode.

四、问答题(本大题共7小题,共28分)。

1. Write down the characteristics present in a von Neumann architecture. (4 分)

- 2. (1) Explain how programmed I/O is different from interrupt-driven I/O. (3 分)
 - (2) How does direct memory access (DMA) work? (3 分)
- 3. Discuss the advantages and disadvantages of dynamic linking. (4 分)
- 4. Explain the functions of the following codes . (4 分)

```
Address Instruction Comments
     100 Load Addr
     101
         Store Next
     102 Load Num
     103 Subt One
     104 Store Ctr
     105 Clear
Loop, 106 Load
                Sum
     107
         AddI Next
     108 Store Sum
     109 Load Next
     10A Add One
     10B Store Next
     10C Load Ctr
     10D Subt One
     10E Store
                 Ctr
     10F Skipcond 00 /If control variable < 0, skip next instruction
     110 Jump Loop
     111 Halt
Addr, 112 Hex 118
Next, 113 Hex 0
Num, 114 Dec 5
Sum, 115 Dec 0
Ctr.
     116 Hex 0
One,
     117 Dec 1
```

5. Convert the following expressions from infix to reverse Polish (postfix) notation. (6 分)

a)
$$X \times Y + W \times Z + V \times U$$

b) $W \times X + W \times (U \times V + Z)$
c) $(W \times (X + Y \times (U \times V)))/(U \times (X + Y))$

6. Suppose we have the instruction Load 500. Given that memory and register R1 contain the values

below: (4 分)

Memory	7
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100	600
 400	300
 500	100
600	500
700	800

R1 200

Assuming R1 is implied in the indexed addressing mode, determine the actual value loaded into the accumulator and fill in the table below:

Mode	Value Loaded into AC
Immediate	
Direct	
Indirect	
Indexed	

五、计算题(本大题共2小题,共21分)。

- 1. (共7分)Suppose that a $2M \times 32$ main memory is built using 256KB $\times 8$ RAM chips and memory is word-addressable. Answer the following questions and write down the reason.
 - a) How many RAM chips are necessary?
 - b) How many RAM chips are there per memory word?
 - c) How many address bits are needed for each RAM chip?
 - d) How many banks will this memory have?
 - e) How many address bits are needed for all of memory?
 - f) If high-order interleaving is used, where would address 14 (which is E in hex) be located?
 - g) If low-order interleaving is used, where would address 14 be located?
- 2. (共14分) Suppose a computer using direct mapped cache has 2¹⁵ words of main memory, and a cache of 8 blocks, where each cache block contains 8 words. If a block is missing from cache, the entire block is brought into the cache and the access is restarted. Initially, the cache is empty.
 - a) How many blocks of main memory are there?(3分)
 - b) What is the format of a memory address as seen by the cache, that is, what are the sizes of the tag, block, and word fields? (3分)
 - c) To which cache block will the memory reference 0x28C map? (3分)
 - d) Compute the hit ratio for a program that loops 4 times from locations 0 to 6710 in memory. (5分)