四川大学期末考试试题（闭卷）

（2017~2018 学年第 1 学期）　　A 卷

课程号：311077030　课程名称：计算机组成和体系结构　任课教师：＿＿＿＿＿＿

适用专业年级：软件工程 2016 级　学号：＿＿＿＿＿＿　姓名：＿＿＿＿＿＿

考生承诺

我已认真阅读并知晓《四川大学考场规则》和《四川大学本科学生考试违纪作弊处分规定（修订）》，郑重承诺：

1、 已按要求将考试禁止携带的文具用品或与考试有关的物品放置在指定地点；

2、 不带手机进入考场；

3、 考试期间遵守以上两项规定，若有违规行为，同意按照有关条款接受处理。

考生签名：

题　　号	一(20%)	二(15%)	三(10%)	四(20%)	五(30%)	六(15%)	七(10%)	八(20%)
得　　分								
卷面总分			教师签名		阅卷时间			

注意事项： 1. 请务必将本人所在学院、姓名、学号、任课教师姓名等信息准确填写在试题纸和添卷纸上；

2. **请将答案全部填写在本试题纸上；**

3. 考试结束，请将试题纸、添卷纸和草稿纸一并交给监考老师。

评阅教师	得分

一、单项选择题（本大题共 10 小题，每小题 2 分，共 20 分）

提示： 在每小题列出的四个备选项中只有一个是符合题目要求的，请将其代码填写在下表中。错选、多选或未选均无分。

1	2	3	4	5					

1. The Von Neumann architecture includes all of the following except:（　　）

（A） a stored program.

（B） sequential processing of instructions.

（C） parallel processing.

（D） a CPU, memory and I/O system

2. The levels of integration in circuits discussed in the book include all but which of the following:（　　）

（A） SSI

（B） MSI

（C） LSI

（D） VLSI

（E） all of these are levels of integration in circuits

3. Identify the following register transfer statements as not legal for the datapath used in MARIE.（　　）

（A） IR ← MAR

（B） MBR ← M[MAR]

（C） AC ← AC + PC

（D） MAR ← PC

4. How many address lines (bits in the address) and I/O lines (bits in the actual data) are needed for 2K x 16 word-addressable memories?（　　）

（A） 11 address bits and 16 I/O lines

（B） 14 address bits and 8 I/O lines

（C） 22 address bits and 16 I/O lines

（D） 12 address bits and 16 I/O lines

5. Which of the following statements is correct（　　）

（A） Input Register holds data just read from memory.

（B） Accumulator holds data the CPU needs to process.

（C） Memory Buffer Register holds next instruction to be executed.

（D） Instruction Register holds address of next instruction to be executed.

评阅教师	得分

二、判断题（本大题共 15 小题，每小题 1 分，共 15 分）

提示：正确打✓，错误打×，将其结果填写在下表中。

1	2	3	4	5	6	7	8	9	10
11	12	13	14	15					

1. The Principle of Equivalence of Hardware and Software says that hardware and software are basically equivalent, and implementations done via either method will run at the same speeds.（　　）

2. A Hertz is one million cycles per second.（　　）

3. Amdahl's Law states that the performance enhancement possible with a given improvement is limited by the amount that the improved feature is used.（　　）

4. A byte is 8 bits, but a word may vary in size (16-bits, 32-bits, etc.) from one architecture to another.（　　）

5. If a computer uses hardwired control, the hardwired part determines the instruction set for the machine. This instruction set can never be changed unless

the architecture is redesigned.（ ）

6. Accumulator architectures use sets of general purpose registers to store operands.（ ）
7. A fixed length instruction must have a fixed length opcode.（ ）
8. The best architecture for evaluating postfix notation is the Registers-based architecture.
9. The core elements of an ISA include the memory model, registers, data types, instruction formats, addressing, and instruction types.（ ）
10. The term endian refers to the byte ordering, or the way a computer stores the bytes of a multiple-byte data element.（ ）
11. Manufacturers use standards so they can market their products to a wider audience than if they came up with separate – and perhaps incompatible – specifications.（ ）
12. As assembler is a program that accepts a symbolic language program and produces the binary machine language equivalent, resulting in a 1-to-1 correspondence between the assembly language source program and the machine language object program.（ ）
13. Indexed or based addressing techniques add the value in the index or base register to the operand to produce the effective address.（ ）
14. MARIE has a common bus scheme, which means a number of entities do not share the bus.
15. The MAR, MBR, PC and IR registers in MARIE can be used to hold arbitrary data values.（ ）

评阅教师	得分

三、名词解释题（本大题共 5 小题，每小题 2 分，共 10 分）。

提示：解释每小题所给名词的含义，若解释正确则给分，若解释错误则无分，若解释不准确或不全面，则酌情扣分。

1. What is a bus in a computer, Name three different types of buses.

2. Name the three basic components of every computer

3. Temporal locality

4. What is an address mode? List four types of address mode

5. What, exactly, is effective access time (EAT)?

评阅教师	得分

四、填空题（本大题共 20 空，每空 1 分，共 20 分）。

1. How many milliseconds (ms) are in 1 second 10^3，How many kilobytes (KB) are in 1 gigabyte (GB) 2^{20}。
2. In MARIE, there are seven registers, PC holds next instruction to be executed, MAR holds address of next instruction to be executed, MBR holds memory address of data being referenced, INREG holds data written from the keyboard.
3. Virtual memory can be implemented with different techniques, including: 人, FIFO, _____.
4. Name three different types of buses _____, _____, _____
5. How many bits are required to address a 2M × 32 main memory if

   a) Main memory is byte-addressable? _____

   b) Main memory is word-addressable? (each word is 32bits) _____
6. Suppose that a 2M x 16 main memory is built using 256K × 8 RAM chips and memory is word-addressable. How many RAM chips are necessary? 16
7. What are the three fields in a Direct Mapped Cache address:

   _____, _____, _____,
8. Given a memory of 2048 bytes consisting of several 32 Byte×8 RAM chips, and assuming byte-addressable memory, the correct way is using _____bits for chip select and _____ bits for address on chip.

评阅教师	得分

五、简答题（本大题共 6 小题，每小题 5 分，共 30 分）。

1. Convert the following expressions from infix to reverse Polish (postfix) notation.

   a. W * (X + Y - Z)
   b. U + (V * (W + (X * (Y + Z))))
   c. X + ((Y + Z) * (V - W) + Z)

2. In a computer instruction format, the instruction length is 11 bits and the size of an address field is 4 bits. Is it possible to have:
   5　2-address instructions
   45　1-address instructions
   32　0-address instructions
   using the format? Justify your answer.

3. Suppose a computer using set associative cache has 216 words of main memory, a cache of 32 blocks and each cache block contains 8 words.
   a. If this cache is 2-way set associative, what is the format of a memory address as seen by the cache, i.e., what are the sizes of the tag, set, and word fields?
   b. b. If this cache is 4-way set associative, what is the format of a memory address as seen by the cache?

4. Suppose we have the instruction Load 500. Given that memory and register R1 contain the values below, Assuming R1 is implied in the indexed addressing mode, determine the actual value loaded into the accumulator and fill in the table below

100	600
…	
400	300
…	
500	100
…	
600	500
…	
700	800

R1

200

Mode	Value Loaded into AC
Immediate	
Direct	
Indirect	
Indexed	

5. Suppose a disk drive has the following characteristics:
   - 4 surfaces
   - 1,024 tracks per surface
   - 128 sectors per track
   - 512 bytes/sector
   - Tract-to-track seek time of 5 milliseconds
   - Rotational speed of 5,000 RPM.

   a. What is the capacity of the drive?
   b. What is the access time

6. A nonpipelined system takes 400ns to process a task. The same task can be processed in a 8-segment pipeline with a clock cycle of 50ns. Determine the speedup ratio of the pipeline for 200 tasks. What is the maximum speedup that could be achieved with the pipeline unit over the nonpipelined unit?

评阅教师	得分

六、计算题（本大题共 2 小题，共 15 分）。

1. (共 8 分)Suppose a computer using direct mapped cache has 2^{15} words of main memory, and a cache of 8 blocks, where each cache block contains 8 words. If a block is missing from cache, the entire block is brought into the cache and the access is restarted. Initially, the cache is empty.

a) How many blocks of main memory are there?
b) What is the format of a memory address as seen by the cache, that is, what are the sizes of the tag, block, and word fields?
c) To which cache block will the memory reference 0x0B63 map?
d) Compute the hit ratio for a program that loops 4 times from locations 0 to 67_{10} in memory.

2. (共 7 分)Suppose that a 2M ×32 main memory is built using 256KB ×8 RAM chips and memory is word-addressable. Answer the following questions and write down the reason.
a) How many RAM chips are necessary?
b) How many RAM chips are there per memory word?
c) How many address bits are needed for each RAM chip?
d) How many banks will this memory have?
e) How many address bits are needed for all of memory?
f) If high-order interleaving is used, where would address 14 (which is E in hex) be located?
g) If low-order interleaving is used, where would address 14 be located?