四川大学期末考试试题（闭卷）

（2014~2015 学年第 1 学期）

课程号：311077030 课程名称：计算机组成和体系结构（A 卷） 任课教师：_____

适用专业年级：软件工程 2013 级 学号：_____ 姓名：_____

考试须知

四川大学学生参加由学校组织或由学校承办的各级各类考试，必须严格执行《四川大学考试工作管理办法》和《四川大学考场规则》。有考试违纪作弊行为的，一律按照《四川大学学生考试违纪作弊处罚条例》进行处理。

四川大学各级各类考试的监考人员，必须严格执行《四川大学考试工作管理办法》、《四川大学考场规则》和《四川大学监考人员职责》。有违反学校有关规定的，严格按照《四川大学教学事故认定及处理办法》进行处理。

题　　号	一(21%)	二(20%)	三(10%)	四(34%)	五(15%)	卷面成绩
得　　分						
阅卷时间						

注意事项：1. 请务必将本人所在学院、姓名、学号、任课教师姓名等信息准确填写在试题纸和添卷纸上；

2. 请将答案全部填写在本试题纸上；

3. 考试结束，请将试题纸、添卷纸和草稿纸一并交给监考老师。

评阅教师	得分

一、名词解释题（本大题共 7 小题，每小题 3 分，共 21 分）。

提示：解释每小题所给名词的含义，若解释正确则给分，若解释错误则无分，若解释不准确或不全面，则酌情扣分。

1. What is the Principle of Equivalence of Hardware and Software

2. What is an opcode?

3. What is a stack?

4. What is the difference between a byte and a word?

5. Describe how an interrupt works and name four different types

6. Explain the concept of a memory hierarchy

7. Explain the concept of pipelining.

评阅教师	得分

二、填空题（本大题共10空，每空2分，共20分）。

1. _____kilobytes (KB) are in 1 gigabyte (GB)
2. List the three fields in a direct mapped cache address_____ , _____ , _____ .
3. Given a memory of 2048 bytes consisting of several 32 Byte×8 RAM chips, and assuming byte-addressable memory, the correct way is using _____bits for chip select and _____bits for address on chip.
4. Cache is accessed by its _____, whereas main memory is accessed by its _____.
5. When a 32bit hex value 12345678 stored in a big endian byte-addressable machine from address 0, the value from byte address 0 to 7 will be _____ , when stored in a little endian machine, the value will be_____

评阅教师	得分

三、判断题（本大题共5小题，每小题2分，共10分）

提示：正确打✓，错误打×，将其结果填写在下表中。

1	2	3	4	5

1. A branch instruction changes the flow of information by changing the PC.
2. The MAR, MBR, PC, and IR registers in MARIE can be used to hold arbitrary data values
3. Registers are storage locations within the CPU itself.
4. MARIE has a common bus scheme, which means a number of entities share the bus..
5. A fixed length instruction must have a fixed length opcode.

评阅教师	得分

四、 问答题（本大题共 6 小题，共 34 分）。

1. Explain what the CPU should do when an interrupt occurs. Include in your answer the method the CPU uses to detect an interrupt, how it is handled, and what happens when the interrupt has been serviced. (5分)

2. Explain the steps in the fetch-decode-execute cycle. Your explanation should include what is happening in the various registers(5分)

3. What kinds of problems do you think endian-ness can cause if you wished to transfer data from a big endian machine to a little endian machine? Explain(5分)

4. Explain the functions of the following codes . (5分)

```
          Load One
          Store X
Loop,   Load X
          Subt Ten
          SkipCond 000
          Jump Endloop
          Load Sum
          Add X
          Store Sum
          Load X
          Add One
          Store X
          Jump Loop
Endloop,  Load Sum
          Output
          Halt
Sum,     Dec 0
X,       Dec 0
One,     Dec 1
Ten,     Dec 10
         END
```

5. Convert the following expressions from reverse Polish notation to infix notation. (6分)

a) W X Y Z - + *
b) U V W X Y Z + * + * +
c) X Y Z + V W - * Z + +

6. Suppose we have the instruction Load 1000. Given that memory and register R1 contain the values below: (8分)

Memory

1000	1400
...	
1100	400
...	
1200	1000
...	
1300	1100
...	
1300	1300

R1 200

Assuming R1 is implied in the indexed addressing mode, determine the actual value loaded into the accumulator and fill in the table below:

Mode	Value Loaded into AC
Immediate	
Direct	
Indirect	
Indexed	

评阅教师	得分

五、计算题（本大题共2小题，共15分）。

1. （共7分）Suppose that a 1M * 16 main memory is built using 128KB * 8 RAM chips and memory is word-addressable.

a) How many RAM chips are necessary?
b) How many RAM chips are there per memory word?
c) How many address bits are needed for each RAM chip?
d) How many banks will this memory have?
e) How many address bits are needed for all of memory?
f) If high-order interleaving is used, where would address 14 (which is E in hex) be located?
g) Repeat Exercise f for low-order interleaving.

2. （共8分）A 2-way set-associative cache consists of four sets. Main memory contains 2K blocks of eight words each.

a. Show the main memory address format that allows us to map addresses from main memory to cache. Be sure to include the fields as well as their sizes.

b. Compute the hit ratio for a program that loops 3 times from locations 8 to 51 in main memory.