四川大学期末试题（闭卷）

（2014~2015 学年第 1 学期）

课程号：311077030 课程名称：计算机组成和体系结构（B 卷） 任课教师：_____

适用专业年级：软件工程 2013 级 学号：_____ 姓名：_____

考试须知

四川大学学生参加由学校组织或由学校承办的各级各类考试，必须严格执行《四川大学考试工作管理办法》和《四川大学考场规则》。有考试违纪作弊行为的，一律按照《四川大学学生考试违纪作弊处罚条例》进行处理。

四川大学各级各类考试的监考人员，必须严格执行《四川大学考试工作管理办法》、《四川大学考场规则》和《四川大学监考人员职责》。有违反学校有关规定的，严格按照《四川大学教学事故认定及处理办法》进行处理。

题　　号	一(10%)	二(14%)	三(24%)	四(30%)	五(22%)	卷面成绩
得　　分						
阅卷时间						

注意事项：1. 请务必将本人所在学院、姓名、学号、任课教师姓名等信息准确填写在试题纸和添卷纸上；

2. **请将答案全部填写在本试题纸上；**

3. 考试结束，请将试题纸、添卷纸和草稿纸一并交给监考老师。

评阅教师	得分

一、判断题（本大题共 10 小题，每小题 1 分，共 10 分）

提示：正确打✓，错误打×，将其结果填写在下表中。

1	2	3	4	5	6	7	8	9	10

1、Accumulator architectures use sets of general purpose registers to store operands.（　　）

2、A branch instruction changes the flow of information by changing the PC（　　）

3、One million bytes can be represented as 1000K bytes.（　　）

4、Manufacturers use standards so they can market their products to a wider audience than if they came up with separate – and perhaps incompatible – specifications.（　　）

5、Amdahl's Law states that the performance enhancement possible with a given improvement is limited by the amount that the improved feature is used.（　　）

6、MARIE has a common bus scheme, which means a number of entities share the bus.（　　）

7、As assembler is a program that accepts a symbolic language program and produces the binary machine language equivalent, resulting in a 1-to-1 correspondence between the assembly language source program and the machine language object program.（　　）

8、The core elements of an ISA include the memory model, registers, data types, instruction formats, addressing, and instruction types. （ ）

9、A fixed length instruction must have a fixed length opcode. （ ）

10、DRAM is often used for cache. （ ）

评阅教师	得分

二、名词解释题（本大题共 7 小题，每小题 2 分，共 14 分）。

提示：解释每小题所给名词的含义，若解释正确则给分，若解释错误则无分，若解释不准确或不全面，则酌情扣分。

1．Name the three basic components of every computer.

2．What is the difference between synchronous buses and nonsynchronous buses ?

3．Explain how programmed I/O is different from interrupt-driven I/O.

4．How does direct memory access (DMA) work?

5．Explain the concept of pipelining.

6．What is an address mode? List five types of address mode.

7．Discuss the advantages and disadvantages of dynamic linking

评阅教师	得分

三、填空题（本大题共 24 空，每空 1 分，共 24 分）。

1. In MARIE , there are seven registers, _____ holds next instruction to be executed, _____ holds address of next instruction to be executed, _____holds memory address of data being referenced, _____ holds data written from the keyboard.

2. Flynn's taxonomy considers two factors. They are _____and_____.

3. Give three different types of buses_____, _____, _____.

4. Virtual memory can be implemented with different techniques, including: _____, _____, _____.

5. How many address lines (bits in the address) and I/O lines (bits in the actual data) are needed for each of the following word-addressable memories?

   a. 2K ×16: _____ address bits and _____ I/O lines
   b. 16K × 8: _____ address bits and _____ I/O lines
   c. 4M × 12: _____ address bits and _____I/O lines

6. What are the three fields in a set associative cache address：_____, _____, _____.

7. Given a memory of 2048 bytes consisting of several 32 Byte x 8 RAM chips, and assuming byte-addressable memory, the correct way is using _____bits for chip select and____bits for address on chip.

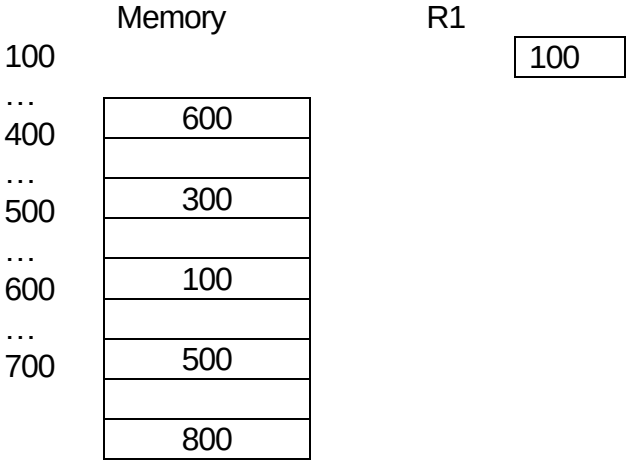
8. the hardware designer must make some decisions on how the CPU should store data. This is the most basic means to differentiate ISAs. There are three choices : _____, _____, _____.

评阅教师	得分

四、问答题（本大题共 3 小题，每小题 10 分，共 30 分）。

1. Suppose we have the instruction Load 500. Given that memory and register R1 contain

the values below:



Assuming R1 is implied in the indexed addressing mode, determine the actual value loaded into the accumulator and fill in the table below:

Mode	**Value Loaded into AC**
Immediate	
Direct	
Indirect	
Indexed	

2．A 2-way set-associative cache consists of four sets. Main memory contains 2K blocks of eight words each.

a. Show the main memory address format that allows us to map addresses from main memory to cache. Be sure to include the fields as well as their sizes.

b. Compute the hit ratio for a program that loops 2 times from locations 8_{10} to 51_{10} in main memory. You may leave the hit ratio in terms of a fraction. one-address instructions that can be added to the instruction set? How to organize?

3. Convert the following expressions from reverse Polish notation to infix notation.

a. W X Y Z - + *

b. U V W X Y Z + * + * +

c. X Y Z + V W - * Z + +

评阅教师	得分

五、计算题（本大题共 2 小题，每小题 11 分，共 22 分）。

1. （共 7 分）Suppose that a 2M × 32 main memory is built using 256KB × 8 RAM chips and memory is word-addressable. Answer the following questions and write down the reason.

a) How many RAM chips are necessary?

b) How many RAM chips are there per memory word?

c) How many address bits are needed for each RAM chip?

d) How many banks will this memory have?

e) How many address bits are needed for all of memory?

f) If high-order interleaving is used, where would address 14 (which is E in hex) be located?

g) If low-order interleaving is used, where would address 14 be located?

2. You have a virtual memory system with a two-entry TLB, a 2-way set associative cache and a page table for a process P. Assume cache blocks of 8 words and page size of 16 words. In the system below, main memory is divided up into blocks, where each block is represented by a letter. Two blocks equals one frame.

Given the system state as depicted above, answer the following questions:

a. How many bits are in a virtual address for process P? Explain.

b. How many bits are in a physical address? Explain.

c. Show the address format for virtual address 18_{10} (specify field name and size) that would be used by the system to translate to a physical address and then translate this virtual address into the corresponding physical address. (Hint: convert 18 to its binary equivalent and divide it into the appropriate fields.) Explain how these fields are used to translate to the corresponding physical address.

d. Given virtual address 6_{10} converts to physical address 54_{10}. Show the format for a physicaladdress (specify the field names and sizes) that is used to determine the cache location for this address. Explain how to use this format to determine where physical address 54 would be located in cache. (Hint: convert 54 to binary and divide it into the appropriate fields.)

e. Given virtual address 25_{10} is located on virtual page 1, offset 9. Indicate exactly how this address would be translated to its corresponding physical address and how the data would be accessed. Include in your explanation how the TLB, Page Table, Cache and Memory are used.