

# Computer Organization and Architecture

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#### Chapter 4

MARIE: An Introduction to a Simple Computer

## Chapter 4 REVIEW OF ESSENTIAL TERMS AND CONCEPTS

- 1. What is the function of a CPU?
- 2. What purpose does a datapath serve?
- 3. What does the control unit do?
- 4. Where are registers located and what are the different types?
- 10. What is a bus cycle?
- 11. Name three different types of buses and where you would find them.
- 12. What is the difference between synchronous buses and nonsynchronous buses
- 13. What are the four types of bus arbitration?



- 4. How many bits would you need to address a 2M X 32 memory if
- ◆ a) The memory is byte-addressable?
- **♦** b) The memory is word-addressable?



- 9. How many 256x8 RAM chips are needed to provide a memory capacity of 4096 bytes?
- ◆ a) How many bits will each address contain?
- b) How many lines must go to each chip?
- ◆ c) How many lines must be decoded for the chip select inputs? Specify the size of the decoder.



- 10. Suppose that a 2M X 16 main memory is built using 256K X 8 RAM chips and memory is word-addressable.
- ◆ a) How many RAM chips are necessary?
- ◆ b) How many RAM chips are there per memory word?
- ◆ c) How many address bits are needed for each RAM chip?
- ♦ d) How many banks will this memory have?
- e) How many address bits are needed for all of memory?
- ♦ f) If high-order interleaving is used, where would address 14 (which is E in hex) be located?
- g) Repeat Exercise 6f for low-order interleaving



- 10. Suppose that a 2M X 16 main memory is built using 256KB X 8 RAM chips and memory is word-addressable.
- . ◆ f) If high-order interleaving is used, where would address 14 (which is E in hex) be located?
- g) Repeat Exercise 6f for low-order interleaving



- 13. A digital computer has a memory unit with 24 bits per word. The instruction set consists of 150 different operations. All instructions have an operation code part (opcode) and an address part (allowing for only one address). Each instruction is stored in one word of memory.
- a) How many bits are needed for the opcode?
- b) How many bits are left for the address part of the instruction?
- c) What is the maximum allowable size for memory?
- d) What is the largest unsigned binary number that can be accommodated in one word of memory?

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19. Explain the steps in the fetch-decodeexecute cycle. Your explanation should include what is happening in the various registers.



- 24. Consider the MARIE program below.
- a) List the hexadecimal code for each instruction.
- b) Draw the symbol table.
- c) What is the value stored in the AC when the program terminates?

Hex Address	Label	Instruction
100	Start,	LOAD A
101		ADD B
102		STORE D
103		CLEAR
104		OUTPUT
105		ADDI D
106		STORE B
107		HALT
108	Α,	HEX 00FC
109	В,	DEC 14
10A	C,	HEX 0108
10B	D,	HEX 0000



- 26. Given the instruction set for MARIE in this chapter, Decipher the following MARIE machine language instructions (write the assembly language equivalent):
  - i) 001000000000111
- ii) 100100000001011
- iii) 001100000001001



## 29. Write the following code segment in MARIE's assembly language:

```
if X > 1 then
    Y = X + X;
    X = 0;
end if;
Y = Y + 1;
```



31. What are the potential problems (perhaps more than one) with the following assembly language code fragment (implementing a subroutine) written to run on MARIE? The subroutine assumes the parameter to be passed is in the AC and should double this value. The Main part of the program includes a sample call to the subroutine. You can assume this fragment is part of a larger program.

Main, Load X

Jump Sub1

Sret, Store X

• • •

Sub1, Add X

**Jump Sret** 



37. A linked list is a linear data structure consisting of a set of nodes, where each one except the last one points to the next node in the list. (Appendix A provides more information about linked lists.) Suppose we have the set of 5 nodes shown in the illustration below. These nodes have been scrambled up and placed in a MARIE program as shown below. Write a MARIE program to traverse the list and print the data in order as stored in each node.

