一、判断题（本大题共 15 小题，每小题 1 分，共 15 分）提示：正确打✓，错误打×。

1. The Principle of Equivalence of Hardware and Software supports the claim that it is not possible to build a special purpose computer to perform only word processing.（ ）
2. A byte is 8 bits, but a word may vary in size (16-bits, 32-bits, etc.) from one architecture to another.（ ）
3. A branch instruction changes the flow of information by changing the PC.（ ）
4. If a computer uses microprogrammed control, the microprogram determines the instruction set for the machine.（ ）
5. A fixed length instruction must have a fixed length opcode.（ ）
6. The term endian refers to the byte ordering, or the way a computer stores the bytes of a multiple-byte data element.（ ）
7. Accumulator architectures use sets of general purpose registers to store operands（ ）
8. The best architecture for evaluating postfix notation is the stack-based architecture.（ ）
9. A two pass assembler generally creates a symbol table during the first pass and finishes the complete translation from assembly language to machine instructions on the second.（ ）
10. The MAR, MBR, PC and IR registers in MARIE can be used to hold arbitrary data values.（ ）
11. A Hertz is one million cycles per second.（ ）
12. Amdahl's Law states that the performance enhancement possible with a given improvement is limited by the amount that the improved feature is used.（ ）
13. Registers are storage locations within the CPU itself.（ ）
14. Indexed or based addressing techniques add the value in the index or base register to the operand to produce the effective address.（ ）
15. Most architectures today are accumulator based.（ ）

二、名词解释题（本大题共 5 小题，每小题 2 分，共 10 分）。提示：解释每小题所给名词的含义，若解释正确则给分，若解释错误则无分，若解释不准确或不全面，则酌情扣分。

1. CPU
2. What is the Principle of Equivalence of Hardware and Software?
3. the three basic components of every computer
4. Immediate Addressing

5. Temporal locality

三、填空题（本大题共 25 空，每空 1 分，共 25 分）。

1. How many milliseconds (ms) are in 1 second_____，How many kilobytes (KB) are in 1 gigabyte (GB)_____。
2. Write the main components of a von Neumann computer _____, _____, _____, _____.
3. How many bits would you need to address a 2M X 32 memory if the memory is byte-addressable? _____.
4. Name three different types of buses _____, _____, _____.
5. The first two bytes of a 2M x 16 main memory have the following hex values:Byte 0 is FE; Byte 1 is 01.If these bytes hold a 16-bit two's complement integer, what is its actual decimal value if memory is little endian? _____.
6. Convert the following expressions from infix to reverse Polish (postfix) notation.

   X * Y + W * Z + V * U _____

7. What are the three fields in a set associative cache address：_____, _____, _____,
8. Name the four types of I/O architectures：_____, _____, _____, _____。
9. Over the years, several attempts have been made to find a satisfactory way to categorize computer architectures. Flynn’s taxonomy considers two factors: _____ and _____。
10. The basic computer performance equation：$\frac{time}{program} = \frac{time}{cycle} \times \frac{\text{cycles}}{\text{instructio n}} \times \frac{(\quad)}{(\quad)}$ For increasing the overall performance of a system, we have the following options：CPU optimization；_____ and _____。

四、问答题（本大题共 5 小题，每小题 6 分，共 30 分）。

1. Recently accessed items tend to be accessed ag2. The von Neumann architecture, which is the basis for most digital computers today, suffers from the von Neumann bottleneck. Explain.in in the near future.
2. How many address lines (bits in the address) and I/O lines (bits in the actual data) are needed for each of the following word-addressable memories?

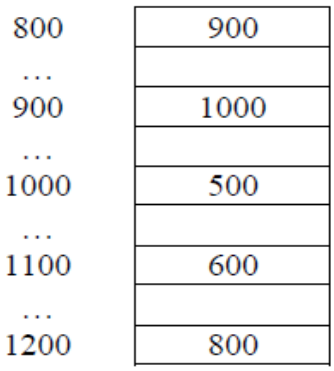
a. 2K x 16

b. 16K x 8

c. 4M x 12

3. Suppose we have the instruction LDA 800. Given memory as follows:

Memory



What would be loaded into the AC if the addressing mode for the operand is:

a. immediate_____

b. direct _____

c. indirect _____

4. A 2-way set-associative cache consists of four sets. Main memory contains 2K blocks of eight words each.

a. Show the main memory address format that allows us to map addresses from main memory to cache. Be sure to include the fields as well as their sizes.

b. Compute the hit ratio for a program that loops 2 times from locations 8_{10} to 51_{10} in main memory. You may leave the hit ratio in terms of a fraction.

5. A nonpipelined system takes 300ns to process a task. The same task can be processed in a 5-segment pipeline with a clock cycle of 60ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speedup that could be achieved with the pipeline unit over the nonpipelined unit?

五、编程、设计及分析题（本大题共 2 小题，每小题 10 分，共 20 分）。提示：每小题给出了一个程序设计要求，请按照要求写出源程序代码，如果源程序代码中出现语法错误或逻辑错误，则酌情扣分。

1. Given the following program

```
   100 Load D
   101 Subt C
   102 Store D
   103 Add A
   104 Store A
   105 JumpI A
   106 AddI B
   107 Subt C
   108 Store B
   109 Jump X
X, 10A Halt
```

```
A, 10B Hex 99
B, 10C Hex 10F
C, 10D Hex 1
D, 10E Hex 8
E, 10F Hex 3
```

When this program terminates, what values will be in:

a. Memory location 10B

b. Memory location 10C

c. Memory location 10D

d. Memory location 10E

e. Memory location 10F

f. The Accumulator

g. The Program Counter

2. You have a virtual memory system with a two-entry TLB, a 2-way set associative cache and a page table for a process P. Assume cache blocks of 8 words and page size of 16 words. In the system below, main memory is divided up into blocks, where each block is represented by a letter. Two blocks equals one frame.

Given the system state as depicted above, answer the following questions:

a. How many bits are in a virtual address for process P? Explain.

b. How many bits are in a physical address? Explain.

c. Show the address format for virtual address 18_{10} (specify field name and size) that would be used by the system to translate to a physical address and then translate this virtual address into the corresponding physical address. (Hint: convert 18 to its binary equivalent and divide it into the appropriate fields.) Explain how these fields are used to translate to the corresponding physical address.

d. Given virtual address 6_{10} converts to physical address 54_{10}. Show the format for a physicaladdress (specify the field names and sizes) that is used to determine the cache location for this address. Explain how to use this format to determine where physical address 54 would be located in cache. (Hint: convert 54 to binary and divide it into the appropriate fields.)

e. Given virtual address 25_{10} is located on virtual page 1, offset 9. Indicate exactly how this address would be translated to its corresponding physical address and how the data would be accessed. Include in your explanation how the TLB, Page Table, Cache and Memory are used.

0	3
4	1

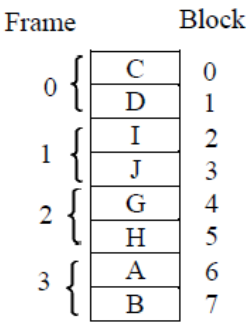
TLB

Set 0	tag	C	tag	I
Set 1	tag	D	tag	H

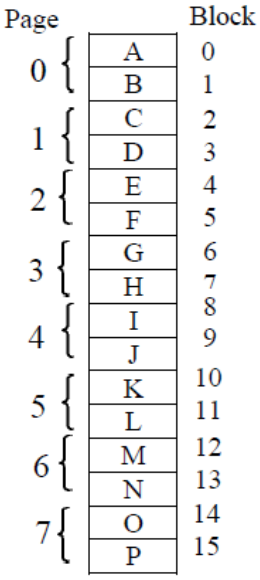
Cache

	Frame	Valid
0	3	1
1	0	1
2	-	0
3	2	1
4	1	1
5	-	0
6	-	0
7	-	0

Page Table



Main Memory



Virtual Memory
For Process P