一、简答题（本大题共 5 小题，每小题 3 分，共 15 分）。

提示：解释每小题所给名词的含义，若解释正确则给分，若解释错误则无分，若解释不准确或不全面，则酌情扣分。

1. What is the difference between a point-to-point bus and a multipoint bus?
2. How does the fetch-decode-execute cycle work?
3. What is Virtual Memory?
4. What is interrupt-driven I/O?
5. What is effective access time (EAT)?

二、填空题（本大题共 15 空，每空 2 分，共 30 分）。

1. Flynn's taxonomy considers two factors: the number of _____and the number of _____that flow into the processor.
2. RAID level _____offer the best performance. RAID level _____uses a mirror (shadow) set. RAID levels _____ offer the best economy while providing adequate redundancy.
3. _____creates internal fragmentation, _____, on the other hand, suffers from external fragmentation。
4. The Amdahl's Law $S = \frac{1}{(1-f)+f/k}$, where S is the speedup, f is_____, k is_____.
5. Suppose a disk drive has the following characteristics: a)4 surfaces; b) 2048 tracks per surface; c)256 sectors per track; d) 512 bytes/sector; e) Track-to-track seek time of 5 milliseconds; f)Rotational speed of 7200 RPM. The capacity of the drive is _____. The access time of the drive is _____
6. Cache is accessed by its _____, whereas main memory is accessed by its _____.
7. Byte 0 is FE and Byte 1 is 01. If these bytes hold a 16-bit two's complement integer and memory is big endian, the actual decimal value is _____. If memory is little endian, the actual decimal value is _____.

三、判断改错题（本大题共 5 小题，每小题 2 分，共 10 分）

提示：正确打✓，错误打×，将其结果填写在下表中。

1. The Principle of Equivalence of Hardware and Software supports the claim that it is not possible to build a special purpose computer to perform only word processing.
2. A branch instruction changes the flow of information by changing the PC.
3. MPP (massively parallel processors) = few processors + shared memory + communication via memory
4. A two-pass assembler generally creates a symbol table during the first pass and finishes the complete translation from assembly language to machine instructions on the second.
5. The geometric mean is more helpful to us than the arithmetic average when we are comparing the relative performance of two systems.

四、问答题（本大题共 5 小题，每小题 5 分，共 25 分）。

1. Explain the functions of MARIA's following registers: AC, MAR, MBR, PC and IR.

2. Give the functions in C language to explain the following code in MARIA assembly language.

```
Loop,   100   Load      Sum
        101   Add       Ctr
        102   Store     Sum
        103   Load      Ctr
        104   Subt      One
        105   Store     Ctr
        106   Skipcond  01      / If AC = 0, skip next instruction
        107   Jump      Loop
        108   Halt
Sum,    109   Dec       0
Ctr,    10A   Dec       5
One,    10B   Dec       1
```

3. Suppose we have the instruction Load 200. Given that memory and register R1 contain the values below:

Memory

100	600
…	
200	300
…	
300	100
…	
400	500
…	
500	400

R1 | 200 |

Assuming R1 is implied in the indexed addressing mode, determine the actual value loaded into the accumulator and fill in the table below:

Mode	Value Loaded into AC
Immediate	
Direct	
Indirect	
Indexed	
Indirect indexed	

4. A digital computer has a memory unit with 32 bits per word. The instruction set consists of 128 different operations. All instructions have an operation code part (opcode) and an address part (allowing for only one address). Each instruction is stored in one word of memory.

a. How many bits are needed for the opcode?

b. How many bits are left for the address part of the instruction?

c. What is the maximum allowable size for memory?

5. Suppose we wish to evaluate the following expression:

Z = (A * B) - (C / D)

a) Convert the expression in postfix notation.

b) Write a program to evaluate the above arithmetic statement using a stack organized computer with zero-address instructions (so only pop and push can access memory).

五、计算题（本大题共 3 小题，共 20 分）。

1. （5 分）A 2-way set-associative cache consists of four sets. Main memory contains 2K blocks of eight words each.

a) Show the main memory address format that allows us to map addresses from main memory to cache. Be sure to include the fields as well as their sizes.

b)Compute the hit ratio for a program that loops 3 times from locations 8_{10} to 51_{10} in main memory. You may leave the hit ratio in terms of a fraction.

2. （5 分）A nonpipelined system takes 300ns to process a task. The same task can be processed in a 5-segment pipeline with a clock cycle of 60ns.

a) Determine the speedup ratio of the pipeline for 100 tasks.

b) What is the maximum speedup that could be achieved with the pipeline unit over the nonpipelined unit?

3.（共 10 分）A system implements a paged virtual address space for each process using a one-level page table. The maximum size of virtual address space is 32MB. The page table for the running process is the following:

Page	Page Table	
	Frame #	Valid Bit
0	1	1
1	2	1
2	4	1
3	16	1
4	9	1
5	-	0
6	-	0
7		

The page size is 512 bytes and the maximum physical memory size of the machine is 4MB.

a) How many bits are required for each virtual address?

b) How many bits are required for each physical address?

c)What is the maximum number of entries in a page table?

d)To which physical address will the virtual address 1524_{10} translate?

e) Which virtual address will translate to physical address 1024_{10}?