计算机组成和体系结构

复习大纲

题型：

判断题：　　10
填空题：　　30
问答题：　　36
计算题：　　24
[分值为大约值]

关注学院：2018-2019学年秋季学期期末专业课考试安排
考试时间：

第一章　引言

1.2 1.5(不含1.5.1 1.5.2) 1.6 1.7

1.2 THE MAIN COMPONENTS OF A COMPUTER

硬件、软件等效性原理

计算机三个基本组成部分　等基本概念

一些度量单位 图**1-2.**

1.5

Moore’s Law ; CPU； ALU;

1.7 THE VON NEUMANN MODEL

von Neumann architecture

main components of a von Neumann

第一章　引言

REVIE OF ESSENTIAL TERMS AND CONCEPTS
基本概念和术语复习

2、
3、　　等效原理
4、
7、8、
18 、
21、22　　摩尔定律
24、25　　冯诺伊曼体系结构
26

练习题
2　　基本单位

第四章 MARIE:简单的模型机

不包含4.8

Chapter 4 Conclusion

- The major components of a computer system are its control unit, registers, memory, ALU, and data path.
- A built-in clock keeps everything synchronized.
- Control units can be microprogrammed or hardwired.
- Hardwired control units give better performance, while microprogrammed units are more adaptable to changes.

Chapter 4 Conclusion

- Computers run programs through iterative fetch-decode-execute cycles.
- Computers can run programs that are in machine language.
- An assembler converts mnemonic code to machine language.
- The Intel architecture is an example of a CISC architecture; MIPS is an example of a RISC architecture.

第四章 MARIE:简单的模型机 -1

4.1 掌握基本概念

CPU概念、功能；控制单元、**ALU**等相关概念

4.1.2 总线概念； **bus master , slave**； 点对点、多点总线；分类(传递信息类型不同：地址、数据、控制)；**synchronous buses** 和 **nonsynchronous buses**

总线仲裁(4种)　总线周期-**bus cycle; clock cycle-**时钟周期

4.1.5 Memory Organization and Addressing(存储器组成和寻址方式)

4.1.6 Interrupts： 中断概念、及类型：

4.2 模型机中**MAR, MBR, PC and IR** 等寄存器功能

表**4-2 MARIE**的指令集，看懂**load store**、**add**、**subt**、**skipcond**等简单指令编写的程序，及编写加、减程序。

4.5 编译汇编程序过程：两次扫描

第四章 MARIE:简单的模型机 -2

一、基本概念和术语复习

1, 2, 3, 4, 5	**CPU, ALU等基本概念**
9, 10, 11, 12, 13	**总线等相关概念**
32,	**取指-译指-执行**
33	**中断驱动I/O**
39	**知道RISC CISC概念**

二、练习题：

1	**CPU主要功能**
3、4、5	**计算地址位数**
6, 7	**构建存储器**
11	~~**了解寄存器变化过程，参见表4-3、图4-13**~~
17、18	~~编写~~、看懂简单的汇编程序（如加、减）

第四章 MARIE:简单的模型机 -2

二、练习题:

~~19 Write a MARIE program using a loop that multiplies two positive numbers by using repeated addition. For example, to multiple 3 x 6, the program would add 3 six times, or~~ 3+3+3+3+3+3.

```
          ORG       100
          Load      Y         /Load second value to be used as counter
          Store     Ctr       /Store as counter
Loop,     Load      Sum       /Load the sum
          Add       X         /Add X to Sum
          Store     Sum       /Store result in Sum
          Load      Ctr
          Subt      One       /Decrement counter
          Store     Ctr       /Store counter
          SkipCond  400       /If AC=0 (Ctr = 0), discontinue looping
          Jump      Loop      /If AC not 0, continue looping
Endloop,  Load      Sum
          Output              /Print product
          Halt                /Sum contains the product of X and Y
Ctr,      Dec       0
X,        Dec       ?         /Initial value of X (could also be input)
Y,        Dec       ?         /Initial value of Y (could also be input)
Sum,      Dec       0         /Initial value of Sum
One,      Dec       1         /The constant value 1
          END
```

第四章 MARIE:简单的模型机 -3

三、是非题：（第四章练习题后）

1、If a computer uses hardwired control, the microprogram determines the instruction set for the machine. This instruction set can never be changed unless the architecture is redesigned. F

2、A branch instruction changes the flow of information by changing the PC. T

3、Registers are storage locations within the CPU itself. T

4、A two pass assembler generally creates a symbol table during the first pass and finishes the complete translation from assembly language to machine instructions on the second. T

第四章 MARIE:简单的模型机 -4

三、是非题：

5、The MAR, MBR, PC and IR registers in MARIE can be used to hold arbitrary data values. F

6、MARIE has a common bus scheme, which means a number of entities share the bus. T

7、As assembler is a program that accepts a symbolic language program and produces the binary machine language equivalent, resulting in a 1-to-1 correspondence between the assembly language source program and the machine language object program. T

8、If a computer uses microprogrammed control, the microprogram determines the instruction set for the machine. T

第五章 指令系统体系结构概览

（不含**5.6 ISA**体系结构的真实案例）

Chapter 5 Conclusion

- ISAs are distinguished according to their bits per instruction, number of operands per instruction, operand location and types and sizes of operands.
- Endianness as another major architectural consideration.
- CPU can store store data based on
  1. A stack architecture
  2. An accumulator architecture
  3. A general purpose register architecture.

Chapter 5 Conclusion

- Instructions can be fixed length or variable length.
- To enrich the instruction set for a fixed length instruction set, expanding opcodes (扩展操作码)can be used.
- The addressing mode of an ISA is also another important factor. We looked at:
  - Immediate
  - Direct
  - Register
  - Register Indirect
  - Indirect
  - Indexed
  - Based
  - Stack

Chapter 5 Conclusion

- A *k*-stage pipeline can theoretically produce execution speedup of *k* as compared to a non-pipelined machine.
- Pipeline hazards such as resource conflicts and conditional branching prevents this speedup from being achieved in practice.
- The Intel, MIPS, and JVM architectures provide good examples of the concepts presented in this chapter.

第五章 -1

基本概念：

ISA；opcode 、Expanding Opcodes 扩展操作码

寻址模式：

5.2 INSTRUCTION FORMATS(指令格式)

5.2.1 Design Decisions for Instruction Sets(指令系统的设计)

5.2.2 Little versus Big Endian(大小端位序问题)

5.2.3 Internal Storage in the CPU: Stacks versus Registers

- **3种体系结构：堆栈、累加器、通用寄存器体系结构；大部分采用?(Given that most architectures today are GPR-based)**

5.2.4 Number of Operands and Instruction Length

- 操作码、操作数、指令长度等关系
- **reverse Polish notation (RPN).** 反向波兰表示法(能转换)

5.2.5 Expanding Opcodes

第五章 -1

5.3 INSTRUCTION TYPES

- **3种体系结构：堆栈、累加器、通用寄存器体系结构；大部分采用?(Given that most architectures today are GPR-based)**

5.4 ADDRESSING(寻址)

- **Immediate Addressing、Direct Addressing、Register Addressing、Indirect Addressing、Indexed and Based Addressing、indirect indexed(间接变址寻址)**

5.5 INSTRUCTION-LEVEL PIPELINING(指令流水线)

第五章 -2

基本概念和术语复习

7、固定长度、可变长度指令结构

12、 13： address mode寻址模式 (five types of address mode: Indirect Addressing…)

16、pipelining(概念)

练习题

1、2、3： 关于大小端

8、9 中缀↔后缀表示法；（会转换、如何编程实现）

10、 堆栈、0地址指令编写程序

11、 扩展操作码

13、14 各种寻址方式 ()

15、16 流水线（概念、计算）

第六章 存储器

（不含**6.6**）

Chapter 6 Conclusion

- Computer memory is organized in a hierarchy, with the smallest, fastest memory at the top and the largest, slowest memory at the bottom.
- Cache memory gives faster access to main memory, while virtual memory uses disk storage to give the illusion of having a large main memory.
- Cache maps blocks of main memory to blocks of cache memory. Virtual memory maps page frames to virtual pages.
- There are three general types of cache: Direct mapped, fully associative and set associative.

Chapter 6 Conclusion

- With fully associative and set associative cache, as well as with virtual memory, replacement policies must be established.
- Replacement policies include LRU(最近最少被使用), FIFO(先进先出). These policies must also take into account what to do with dirty blocks.
- All virtual memory must deal with fragmentation, internal for paged memory, external for segmented memory.

第六章 存储器 -1

存储器的层次结构图**6-1**

6.2 TYPES OF MEMORY：

•***RAM*** (*random access memory*) and ***ROM*** (*read-only memory*).

•SRAM is faster and much more expensive than DRAM; however, designers use DRAM because it is much denser (can store many bits per chip), uses less power, and generates less heat than SRAM.

6.3 THE MEMORY HIERARCHY

ESSENTIAL TERMS AND CONCEPTS:

•Hit, Miss, Hit rate, Miss rate, Miss penalty

•Locality of Reference: Temporal locality, Spatial locality, Sequential locality

第六章 存储器 -1

6.4 CACHE MEMORY

ESSENTIAL TERMS AND CONCEPTS:

Cache Mapping Schemes:

Direct Mapped Cache: Direct mapped cache assigns cache mappings using a modular approach

Fully Associative Cache: allowing a main memory block to be placed anywhere in cache.

Set Associative Cache: N-way set associative cache mapping, a combination of these two approaches. This scheme is similar to direct mapped cache, in that we use the address to map the block to a certain cache location. The important difference is that instead of mapping to a single cache block, an address maps to a set of several cache blocks.

6.4.3 有效存取时间和命中率

EAT

第六章 存储器 -1

6.5 VIRTUAL MEMORY

ESSENTIAL TERMS AND CONCEPTS:

Virtual Memory, Virtual address, Physical address Mapping, Page frames, Pages, Paging, Fragmentation, Page fault

TLB--→EAT

第六章 存储器 -1

掌握
引用的局部性：时间、空间、顺序。**Temporal locality** 、**Spatial locality**、 Sequential locality
三种高速缓存映射模式，域的划分，命中率计算

Cache 和 **main memory** 访问方式
cache write policies：

virtual memory: 实现方式：分页、分段、或分页与分段； 虚拟地址到物理地址的转换

第六章 存储器 -2

REVIEW OF ESSENTIAL TERMS AND CONCEPTS:

- **1、2:** 存储器类型
- **9:** **Cache访问(内容、地址Cache is not accessed by address; it is accessed by content. For this reason, cache is sometimes called content addressable memory or CAM.)**
- **10、14、15** 三种映射模式、域的划分
- **19、20、22** 有效存取时间等概念、计算
- **30** **TLB EAT**
- **28、33** 内部碎片、外部碎片

EXERCISES

1, 2; 3, 4, 5; 三种高速缓存映射模式、域划分

6, 7, 8,10,11 命中率

6，10 : 计算命中率(掌握)

12,13 : 虚拟地址到物理地址的转换

14,16: 虚拟存储器

第七章 输入/输出和存储系统

第7章

（不含7.4.2 软盘，7.8）

Chapter 7 Conclusion
-本章小结

- I/O systems are critical to the overall performance of a computer system.
- Amdahl's Law quantifies this assertion.
- I/O systems consist of memory blocks, cabling, control circuitry, interfaces, and media.
- I/O control methods include programmed I/O, interrupt-based I/O, DMA, and channel I/O.
- Buses require control lines, a clock, and data lines. Timing diagrams specify operational details.

Chapter 7 Conclusion

- Magnetic disk is the principal(主要的) form of durable storage.
- Disk *performance metrics*(性能度量) include seek time, rotational delay, and reliability estimates.
- Optical disks provide long-term storage for large amounts of data, although access is slow.
- Magnetic tape is also an archival medium. Recording methods are track-based, serpentine(蛇形记录), and helical scan(螺旋扫描).

Chapter 7 Conclusion

- RAID gives disk systems improved performance and reliability. RAID 3 and RAID 5 are the most common.
- Many storage systems incorporate data compression.
- Two approaches to data compression are statistical data compression and dictionary systems.
- GIF, PNG, MNG, and JPEG are used for image compression.

第七章 -1

ESSENTIAL TERMS AND CONCEPTS:

Amdahl's Law (公式含义)； Speedup 等

•I/O architectures: 4

Programmed I/O： Systems using programmed I/O devote at least one register for the exclusive use of each I/O device. The CPU continually monitors each register, waiting for data to arrive. This is called polling.

Interrupt-Driven I/O

Q: Explain how programmed I/O is different from interrupt-driven I/O; how an interrupt works and name four different types interrupt at least

DMA: How does direct memory access (DMA) work

protocol： The exact form and meaning of the signals exchanged between a sender and a receiver is called a protocol. （7.3）

•7.4.1 Rigid Disk Drives

~~**•7.8.1中的Huffman编码 书上编码过程**~~

第七章 -2

基本概念和术语复习

1、2： Amdahl's Law

3 **protocol(协议)**

5、8、12、13 输入、输出系统，**4种I/O控制方法。**

(中断控制IO，中断类型，中断响应过程)

21、22 **(硬盘相关)**

36、37、38 **RAID(性能-0、经济-5、镜像-1)**

练习题：

4、4种I/O控制方法及应用场合

5、中断响应过程

17、18 磁盘容量、访问时间计算 （$\frac{\frac{60\ \text{seconds}}{\text{disk rotation speed}} \times \frac{100\ \text{ms}}{\text{second}}}{2}$

29 赫夫曼编码

第八章 系统软件

大部分内容不考察

第九章 可选择的体系结构

只要求：**9.3 FLYNN**分类方法

一、基本概念和术语复习

4、分类依据：指令的数目和流入处理器的数据流的数目

Flynn's taxonomy considers two factors: the number of instructions and the number of data streams that flow into the processor.

二、作业：

第十章 性能度量和分析

10.2 THE BASIC COMPUTER PERFORMANCE EQUATION

公式

$$\text{CPU Time} = \frac{\text{seconds}}{\text{program}} = \frac{\text{instructions}}{\text{program}} \times \frac{\text{avg. cycles}}{\text{instruction}} \times \frac{\text{seconds}}{\text{cycle}}$$

优化方案：**CPU优化、存储器优化、I/O优化**

基本概念和术语复习

1、2

作业：