一、简答题（本大题共 7 小题，每小题 3 分，共 21 分）。

1. Name the characteristics present in a von Neumann architecture
2. What is an opcode?
3. Explain the differences between data buses, address buses, and control buses?
4. What is the difference between a byte and a word?
5. Explain the difference between memory-mapped I/O and instruction-based I/O.
6. How does direct memory access (DMA) work?
7. What are the pipeline conflicts that can cause a slowdown in the pipeline?

二、填空题（本大题共 10 空，每空 2 分，共 20 分）

1. _____bits are needed to address a memory space which has 256MB.
2. There are three basic forms of locality in memory access, they are _____, _____ and _____.
3. Given a memory of 4096 bytes consisting of several 64 Byte×8 RAM chips, and assuming byte-addressable memory,the correct way is using _____bits for chip select and _____bits for address on chip.
4. Cache is accessed by its _____, whereas main memory is accessed by its_____.
5. When a 32bit hex value 87654321 stored in a big endian byte-addressable machine from address 0, the value from byte address 0 to 7 will be _____, when stored in a little endian machine, the value will be_____.

三、判断题（本大题共 5 小题，每小题 2 分，共 10 分）

提示：正确打✓，错误打×，将其结果填写在下表中，并改正。

1	2	3	4	5

1. A branch instruction changes the flow of information by changing the PC.
2. For increasing the overall performance of a system, we have the options of CPU optimization, Memory optimization and I/O optimization.
3. Registers are storage locations within the CPU itself.
4. MARIE has a common bus scheme, which means a number of entities share thebus.
5. A fixed length instruction must have a fixed length opcode.

四、问答题（本大题共 6 小题，共 34 分）。

1. Explain what the CPU should do when an interrupt occurs. Include in your answer the method the CPU uses to detect an interrupt, how it is handled, and what happens when the interrupt has been serviced.(4 分)
2. Consider a byte-addressable computer with 24-bit addresses, a cache capable of storing a total of 64KB of data, and blocks of 32 bytes. Show the format of a 24-bit memory address for:(6 分)
   a) direct mapped
   b) associative
   c) 4-way set associative
3. What kinds of problems do you think endian-ness can cause if you wished to transfer data from a big endian machine to a little endian machine? Explain(5 分)
4. A nonpipeline system takes 100ns to process a task. The same task can be processed in a 5-stage pipeline with a clock cycle of 20ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the theoretical speedup that could be achieved with the pipeline system over a nonpipelinedsystem?.(5 分)
5. Convert the following expressions from infix to reverse Polish (postfix) notation.(6 分)
   a) X * Y + W * Z + V * U
   b) W * X + W * (U * V + Z)
   c) (W * (X + Y * (U * V)))/(U * (X + Y))
6. Suppose we have the instruction Load 500. Given that memory and register R1 contain the values below:(8 分)

Memory

100	600

400	300

500	100

600	500

700	800

R1 | 200 |

Assuming R1 is implied in the indexed addressing mode, determine the actual value loaded into the accumulator and fill in the table below:

Mode	Value Loaded into AC
Immediate	
Direct	
Indirect	
Indexed	

五、计算题（本大题共 2 小题，共 15 分）。

1. (共 7 分) Write a MARIE subroutine to subtract two numbers.
2. (共 8 分) A direct-mapped cache consists of eight blocks. Main memory contains 4K blocks of eight words each. Access time for the cache is 22ns and the time required to fill a cache slot from main memory is 300ns. (This time allows us to determine the block is missing and bring it into cache.) Assume a request is always started in parallel to both cache and to main memory (so if it is not found in cache, we do not have to add this cache search time to the memory access). If a block is missing from cache, the entire block is brought into the cache and the access is restarted. Initially, the cache is empty.
   a. Show the main memory address format that allows us to map addresses from main memory to cache. Be sure to include the fields as well as their sizes.
   b. Compute the hit ratio for a program that loops 4 times from locations 0 to 6710 in memory.
   c. Compute the effective access time for this program.