一、判断题（本大题共 10 小题，每小题 1 分，共 10 分）提示：正确打✓，错误打×，将其结果填写在下表中。

1、The Von Neumann architecture includes all of the following : a. a stored program ; b. sequential processing of instructions; c. a CPU, memory and I/O system. （ ）

2、The Principle of Equivalence of Hardware and Software says that hardware and software are basically equivalent, and implementations done via either method will run at the same speeds. （ ）

3、One million bytes can be represented as 1000K bytes. （ ）

4、Manufacturers use standards so they can market their products to a wider audience than if they came up with separate – and perhaps incompatible – specifications. （ ）

5、If Moore’s Law is to hold, Rock’s Law must fall. （ ）

6、If a computer uses hardwired control, the microprogram determines the instruction set for the machine. This instruction set can never be changed unless the architecture is redesigned. （ ）

7、MARIE has a common bus scheme, which means a number of entities share the bus. （ ）

8、As assembler is a program that accepts a symbolic language program and produces the binary machine language equivalent, resulting in a 1-to-1 correspondence between the assembly language source program and the machine language object program. （ ）

9、The core elements of an ISA include the memory model, registers, data types, instruction formats, addressing, and instruction types. （ ）

10、Both SIMD and MIMD machines have multiple processors and can operate on different pieces of data in parallel. （ ）

二、名词解释题（本大题共 8 小题，每小题 2 分，共 16 分）。

提示：解释每小题所给名词的含义，若解释正确则给分，若解释错误则无分，若解释不准确或不全面，则酌情扣分。

1. State Moore’s Law.
2. Name the three basic components of every computer.
3. What is the function of a CPU
4. ALU
5. Accumulator architectures
6. Pipelining
7. RAM and ROM
8. Direct Mapped Cache

三、填空题（本大题共 24 空，每空 1 分，共 24 分）。

1. Name the three basic components of every computer_____，_____，_____.
2. Name the four type of I/O control methods _____，_____，_____，_____。
3. Flynn's taxonomy considers two factors. They are _____ and _____.
4. Give three different types of buses _____，_____，_____.
5. List three addressing mode: _____，_____，_____.
6. Virtual memory can be implemented with different techniques, including:_____，____，___.
7. List the three fields in a set associative cache address _____，_____，_____.
8. the hardware designer must make some decisions on how the CPU should store data. This is the most basic means to differentiate ISAs. There are three choices : _____，_____，_____.

四、问答题（本大题共 3 小题，每小题 10 分，共 30 分）。

1. Suppose we have the instruction Load 500. Given that memory and register R1 contain the values below:

	Memory
100	600
…	
400	300
…	
500	100
…	
600	500
…	
700	800

200 R1

Assuming R1 is implied in the indexed addressing mode, determine the actual value loaded into the accumulator and fill in the table below:

Mode	Value Loaded into AC
Immediate	
Direct	
Indirect	
Indexed	

2. a. In a computer instruction format, the instruction length is 11 bits and the size of an address field is 4 bits. Is it possible to have:

5 2-address instructions

45 1-address instructions

32 0-address instructions

using the format? Justify your answer.

b. Assume that a computer architect has already designed 6 two-address and 24 zero

address instructions using the instruction format above. What is the maximum number of one-address instructions that can be added to the instruction set? How to organize?

3. Convert the following expressions from reverse Polish notation to infix notation.

a. W X Y Z - + *

b. U V W X Y Z + * + * +

c. X Y Z + V W - * Z + +

五、计算题（本大题共 2 小题，每小题 10 分，共 20 分）。

1. A direct-mapped cache consists of eight blocks. Main memory contains 4K blocks of eight words each. Access time for the cache is 22 ns and the time required to fill a cache slot from main memory is 300ns (this time will allow us to determine the block is missing and bring it into cache). Assume a request is always started in parallel to both cache and to main memory (so if it is not found in cache, we do not have to add this cache search time to the memory access). If a block is missing from cache, the entire block is brought into the cache and the access is restarted. Initially, the cache is empty.

   a. Show the main memory address format that allows us to map addresses from main memory to cache. Be sure to include the fields as well as their sizes.

   b. Compute the hit ratio for a program that loops 4 times from locations 0 to 6710 in memory.

2. A system implements a paged virtual address space for each process using a one level page table. The maximum size of virtual address space is 16MB. The page table for the running process includes the following valid entries (the → notation indicates that a virtual page maps to the given page frame, that is, it is located in that frame):

   Virtual page 2 →Page frame 4　　Virtual page 4 → Page frame 9

   Virtual page 1 →Page frame 2　　Virtual page 3 → Page frame 16

   Virtual page 0 →Page frame 1

   The page size is 1024 bytes and the maximum physical memory size of the machine is 2MB.

   a) How many bits are required for each virtual address?

   b) How many bits are required for each physical address?

   c) What is the maximum number of entries in a page table?

   d) To which physical address will the virtual address 152410 translate?

   e) Which virtual address will translate to physical address 102410?