DIGITAL LOGIC

数字逻辑

Registers

- A *n*-bit *register* is a set of *n* flip-flops that is capable of storing *n* bits of binary information.
- With added combinational gates, the register can perform data-processing tasks.
- A *counter* is a register that goes through a predetermined sequence of states upon the application of clock pulses.

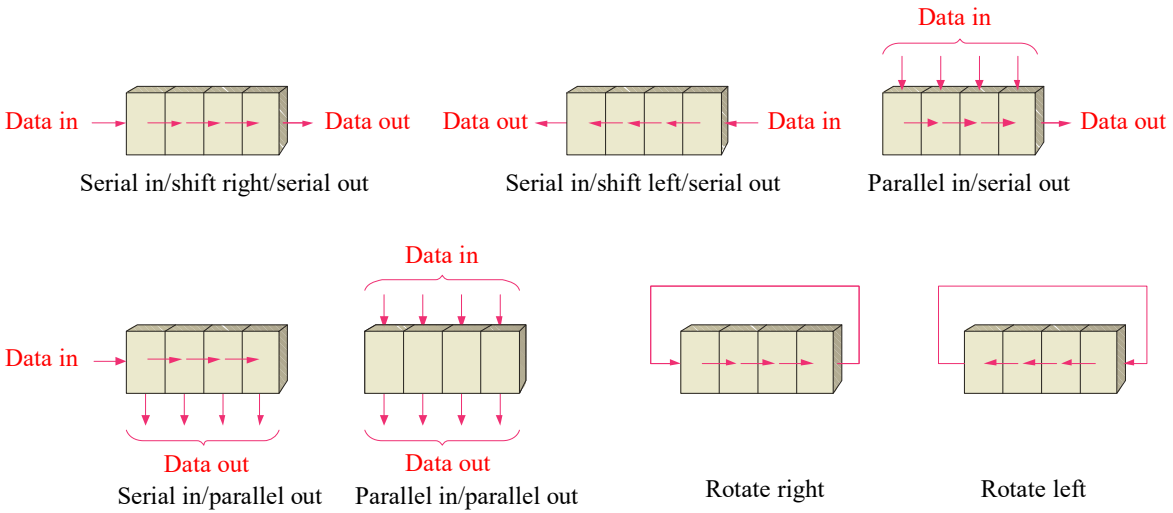
Registers Overview

- Parallel Load Register
- Shift Registers
  - Serial Load
  - Serial Addition
- Shift Register with Parallel Load
- Bidirectional Shift Register

Registers Overview

Basic Shift Register Operations

- **A shift register is an arrangement of flip-flops with important applications in storage and movement of data. Some basic data movements are illustrated here.**

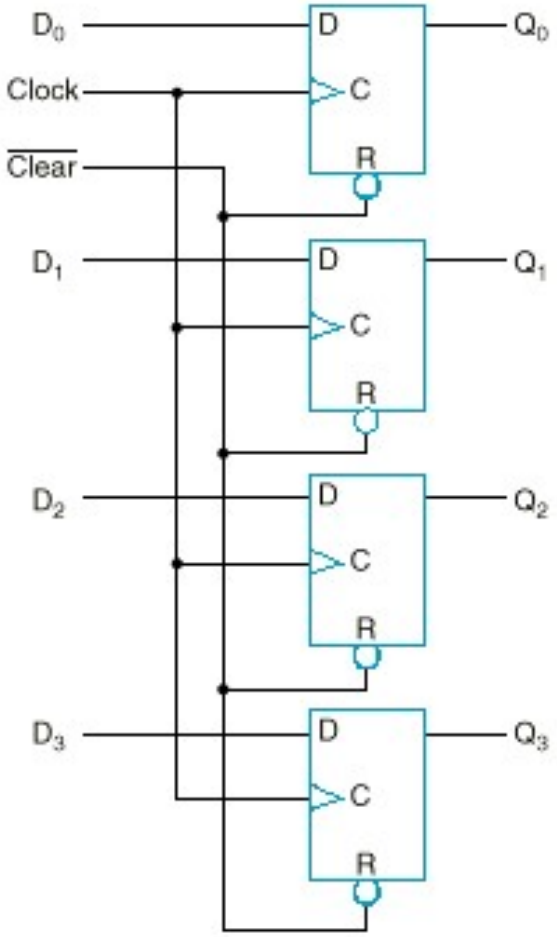


寄存器数据输入与输出类型：串入串出/串入并出/并入串出/并入并出
串行输入：每次只有一位数据送入最高/最低位触发器中。
串行输出：数据只从单一的一个触发器中获得，每次只能提取一位
并行输入：所有触发器应同时起作用（置位或复位）
并行输出：所有触发器的输出Q都应可访问。

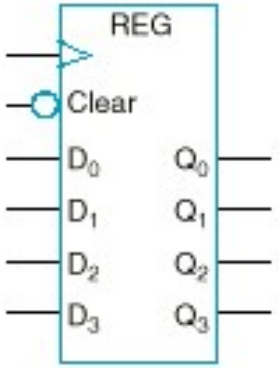
Registers

- Example (next slide) generic 4-bit register.
- The common *Clock* input triggers all flip-flops on the rising edge of each pulse, and the binary data available at the four D inputs are transferred into the 4-bit register.

Registers



(a) Logic diagram



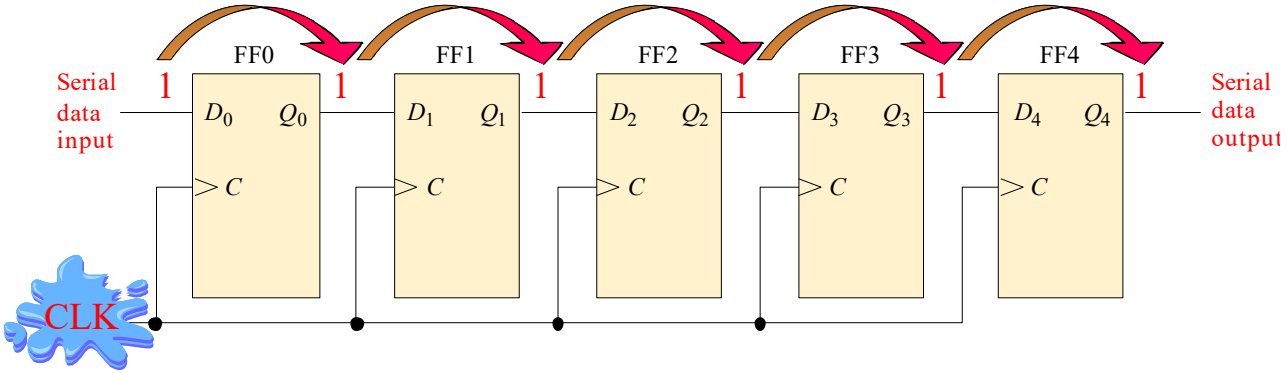
(b) Symbol

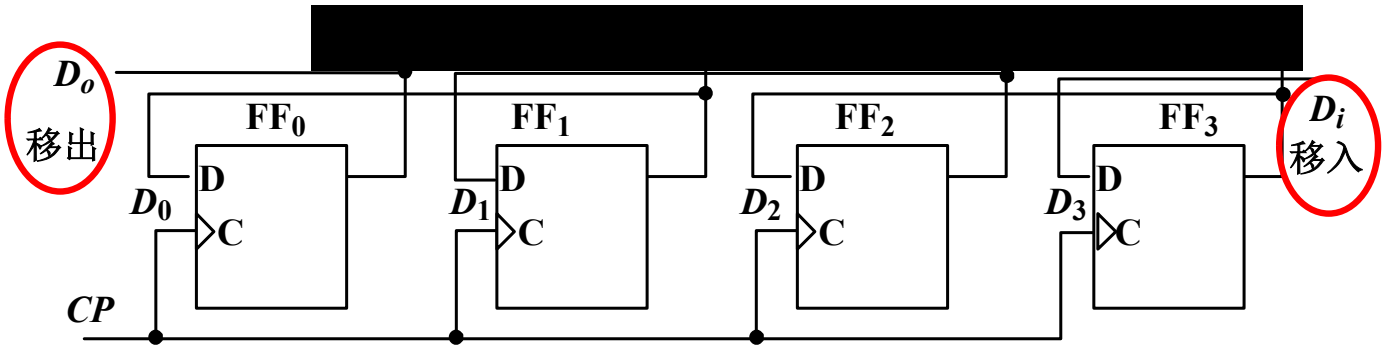
Registers

Serial-in/Serial out Shift Register

Shift registers are available in IC form or can be constructed from discrete flip-flops as is shown here with a five-bit serial-in serial-out register.

Each clock pulse will move an input bit to the next flip-flop. For example, a 1 is shown as it moves across.



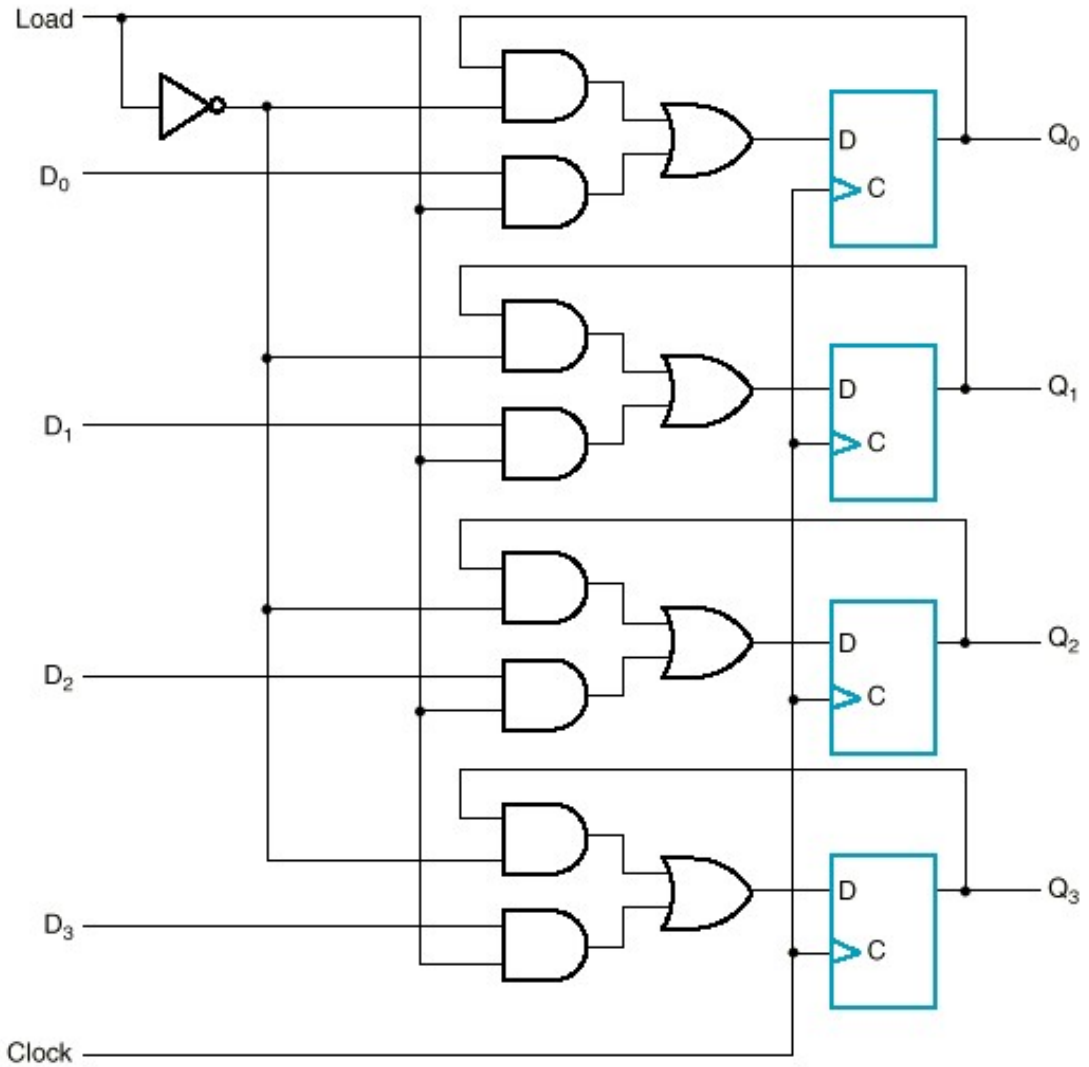


输入		现态				次态				说明
D_i	CP	Q_0^n	Q_1^n	Q_2^n	Q_3^n	Q_0^{n+1}	Q_1^{n+1}	Q_2^{n+1}	Q_3^{n+1}	
1	↑	0	0	0	0	0	0	0	1	
1	↑	1	0	0	0	0	0	1	1	连续输入
1	↑	1	1	0	0	0	1	1	1	4 个 1
1	↑	1	1	1	0	1	1	1	1	

Registers with parallel load

- Next page shows a 4-bit register with a control input *Load* that is directed through gates into the D inputs of the flip-flops.
- When *Load* is 1, the data on the four inputs is transferred into the register with the next positive transition of a clock pulse.
- When *Load* is 0, the data inputs are blocked, and the D inputs of the flip-flops are connected to their outputs.

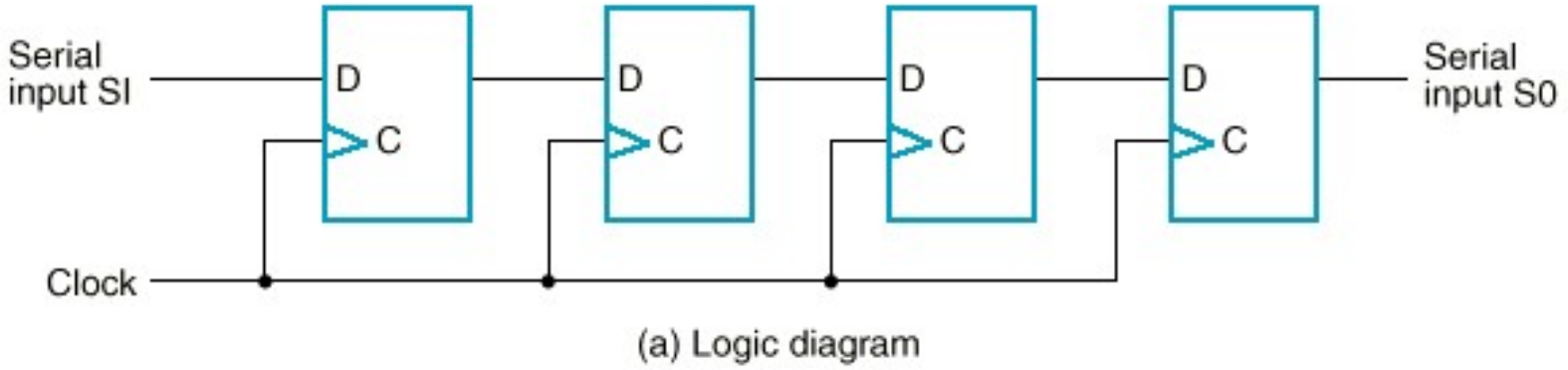
Registers



Shift Registers

- A register capable of shifting its stored bits laterally in one or both directions is called a *shift register*.
- The logical configuration of a shift register consists of a chain of flip-flops in cascade, with the output of one flip-flop connected to the input of the next FF.

Shift Registers

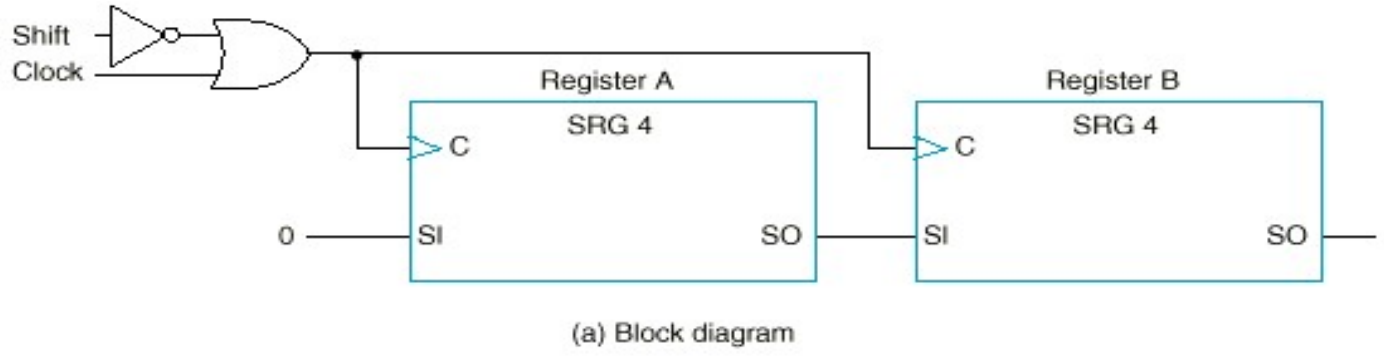


(a) Logic diagram

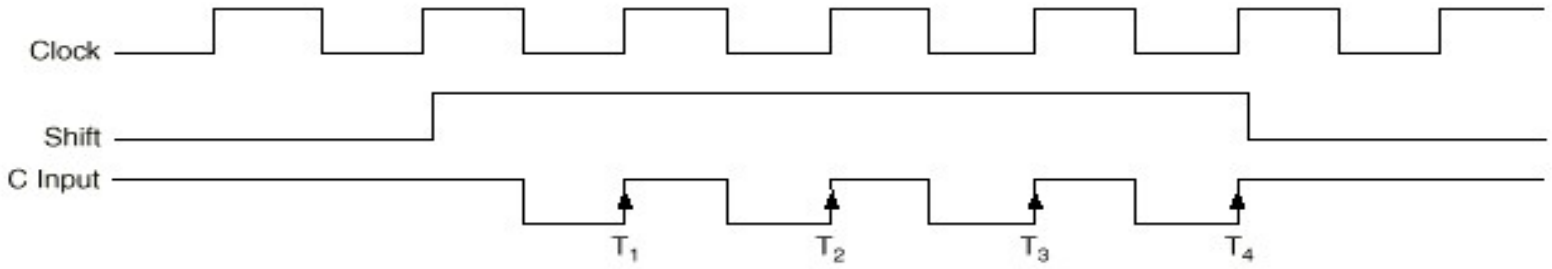
(b) Symbol

Shift Registers (cont.)

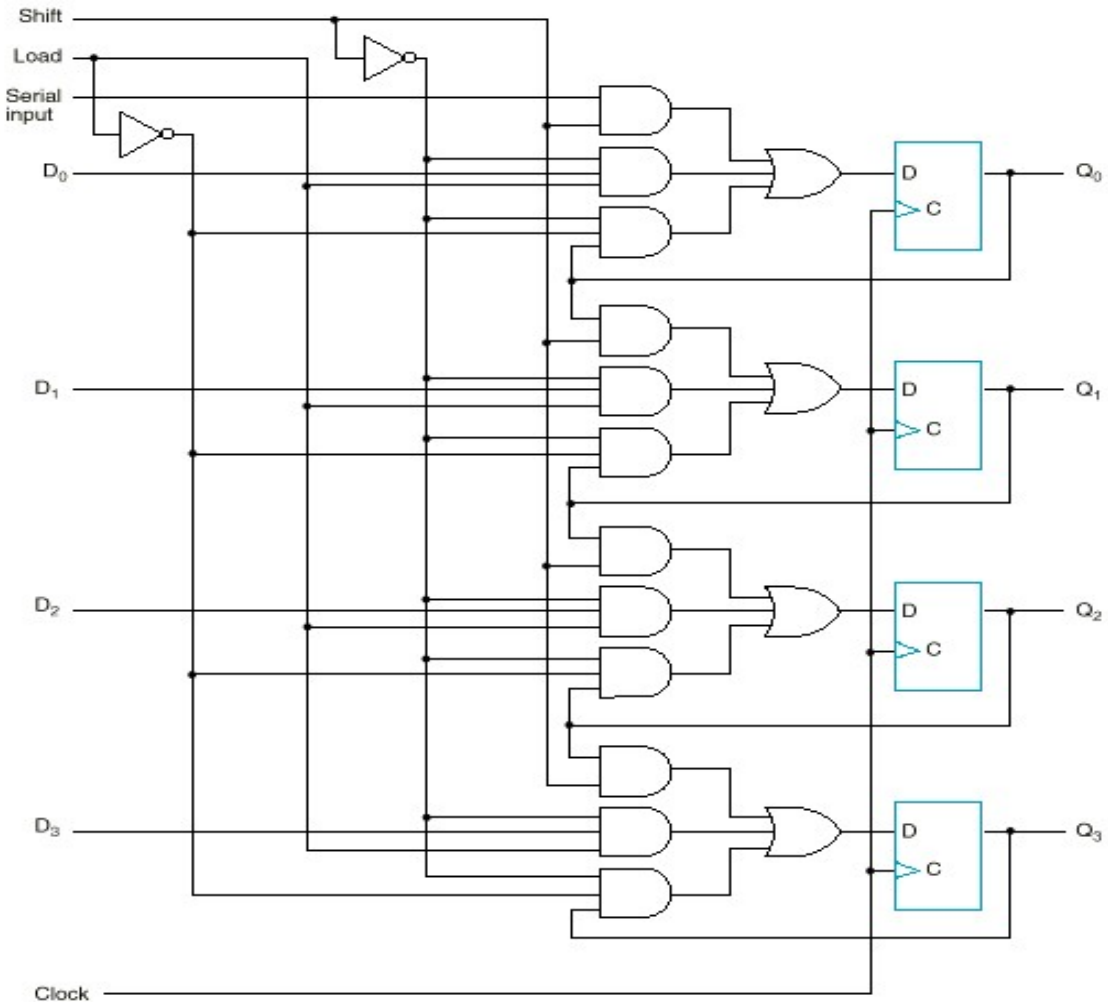
- The next figure shows how the serial transfer of information from register A to register B can be done. One clock cycle per bit of data is required.

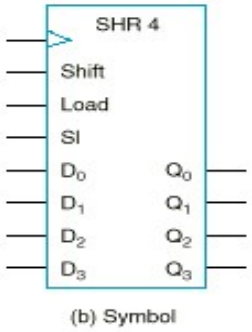


(a) Block diagram



Shift Register with parallel load





(b) Symbol

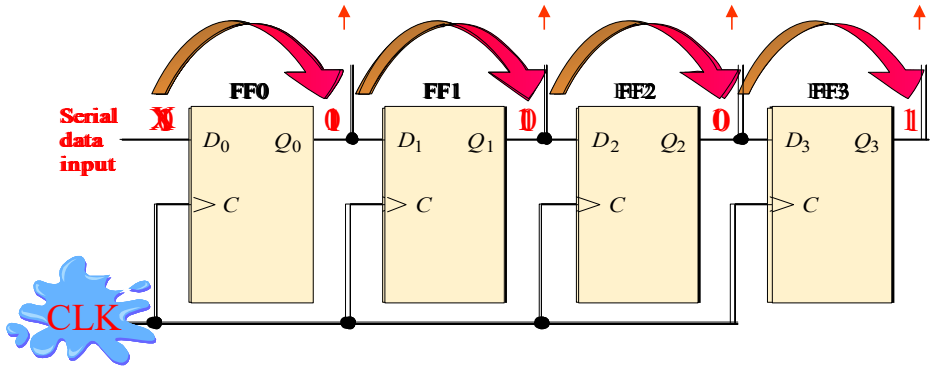
Shift	Load	Operation
0	0	Nothing
0	1	Load parallel
1	X	Shift

Shift Register

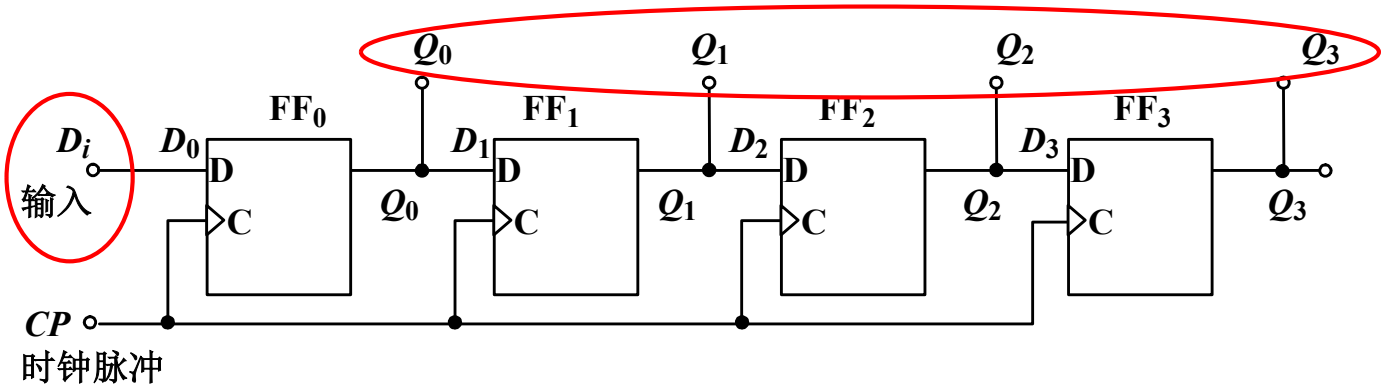
An application of shift registers is conversion of serial data to parallel form.

For example, assume the binary number 1011 is loaded sequentially, one bit at each clock pulse.

After 4 clock pulses, the data is available at the parallel output.



Shift Register



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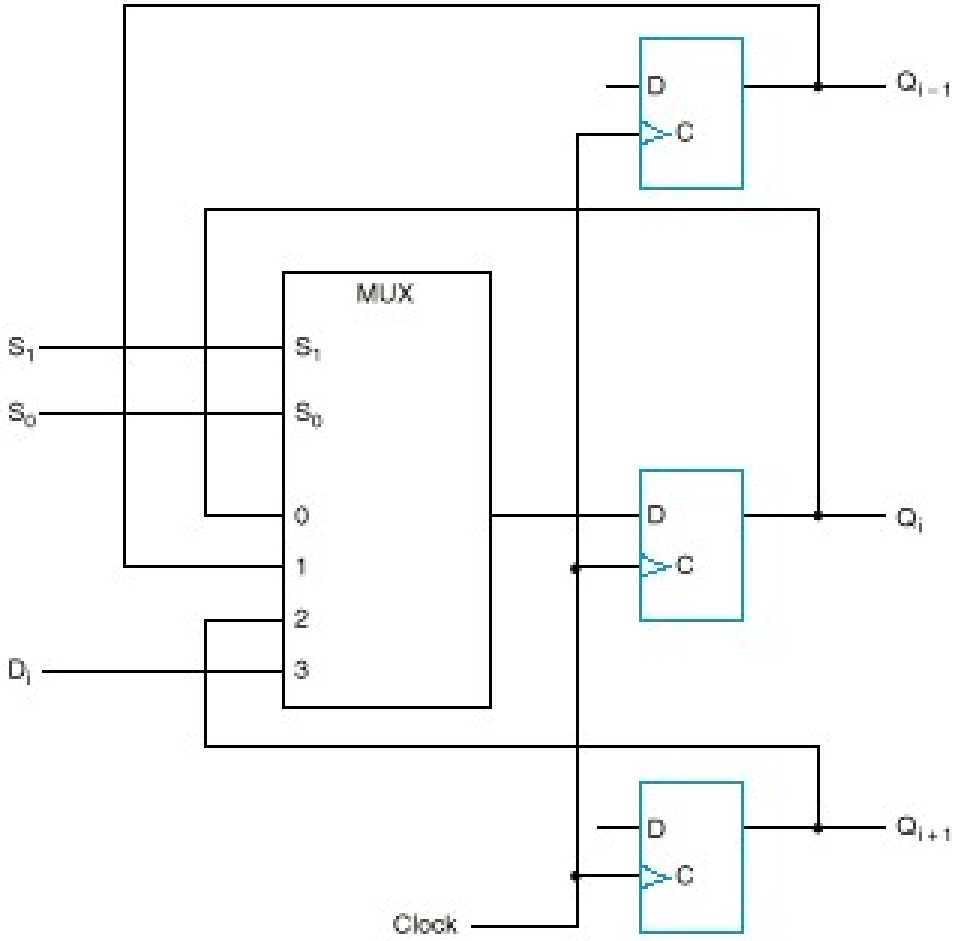
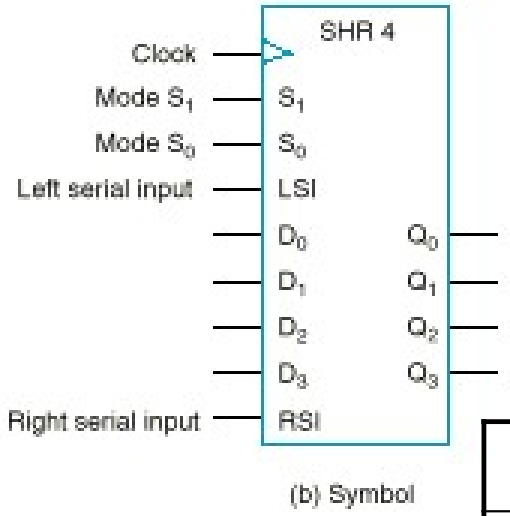
Bidirectional Shift Register



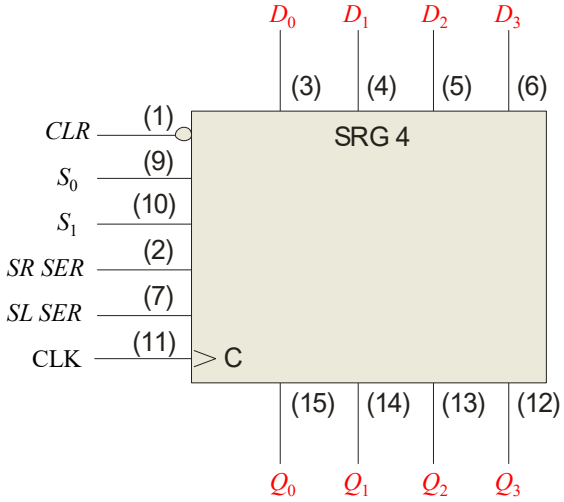


(b) Symbol

S_1S_0	Action
00	Nothing
01	Shift down
10	Shift up
11	Parallel load

Universal Shift Register

A universal shift register has both serial and parallel input and output capability. The 74HC194 is an example of a 4-bit bidirectional universal shift register.

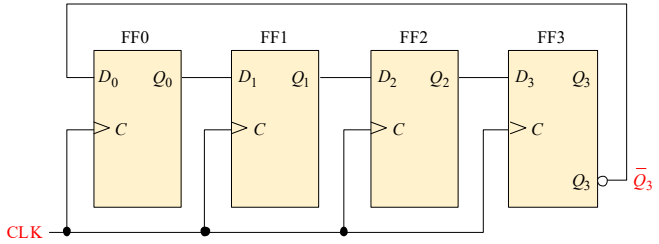


$\overline{CLR}$	S_1	S_0	CP	
0	×	×	×	异步清零
1	0	0	×	保　持
1	0	1	↑	右　移
1	1	0	↑	左　移
1	1	1	×	并行输入

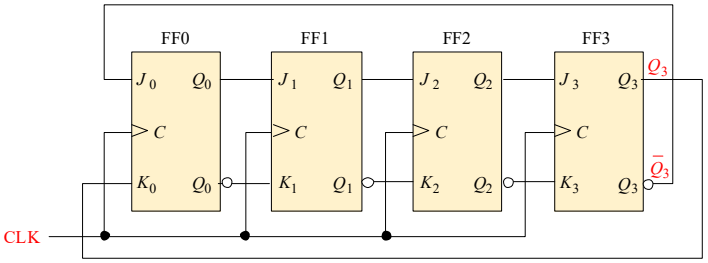
Shift Register Counters

Shift registers can form useful counters by recirculating a pattern of 0's and 1's. Two important shift register counters are the *Johnson counter* and the *ring counter*.

The Johnson counter can be made with a series of D flip-flops



… or with a series of J-K flip flops. Here Q_3 and $\overline{Q}_3$ are fed back to the J and K inputs with a "twist".



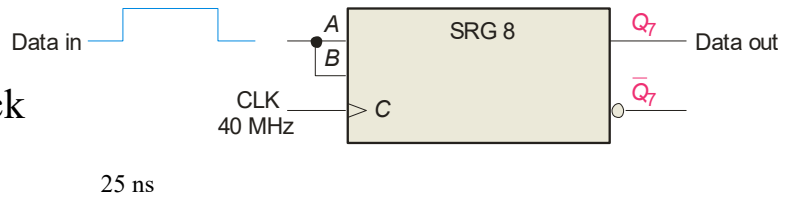
Application

Shift Register Applications

Shift registers can be used to delay a digital signal by a predetermined amount.

Example An 8-bit serial in/serial out shift register has a 40 MHz clock. What is the total delay through the register?

Solution



25 ns

The delay for each clock is 1/40 MHz = 25 ns

The total delay is
8 x 25 ns = 200 ns

= 200 ns

Serial addition using shift registers

- The two binary numbers to be added serially are stored in two shift registers.
- Bits are added one pair at a time through a **single** full-adder circuit.
- The **carry out** of the full adder is transferred into a D flip-flop. The output of the carry FF is then used as the carry input for the next pair of bits.
- The sum bit on the S output of the full adder is transferred into the result register A.

Serial vs. parallel addition

- The parallel adder is a combinational circuit, whereas the serial adder is a sequential circuit.
- The parallel adder has *n* full adders for *n*-bit operands, whereas the serial adder requires only one full adder.
- The serial circuit takes *n* clock cycles to complete an addition.
- In summary, the parallel adder in space is n times larger than the serial adder, but it is *n* times faster.
- The serial adder, although it is *n* times slower, is *n* times smaller in space.(It's a trade-off!)

Johnson Counter

Shift Register Counters

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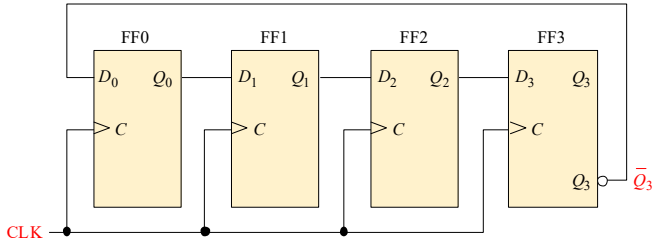

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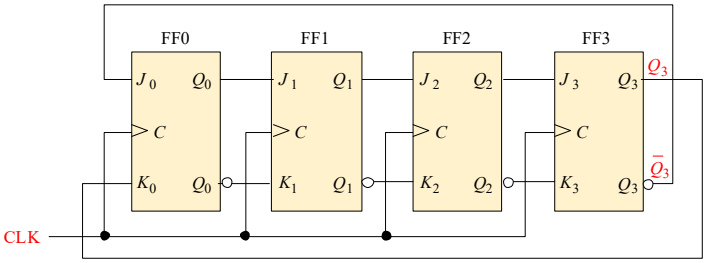
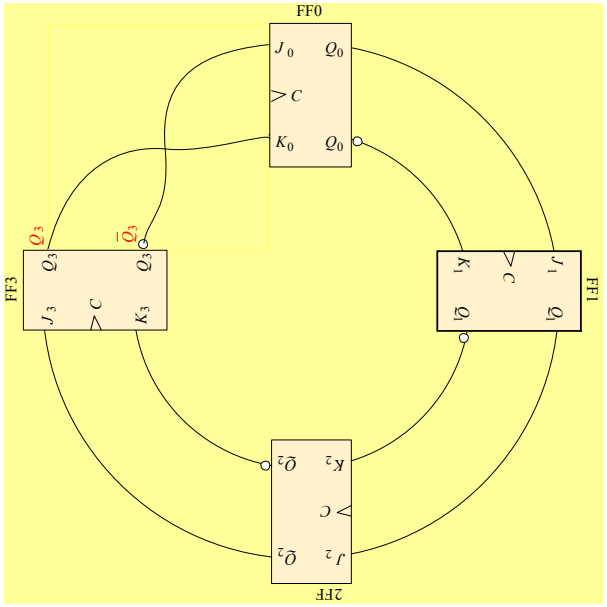
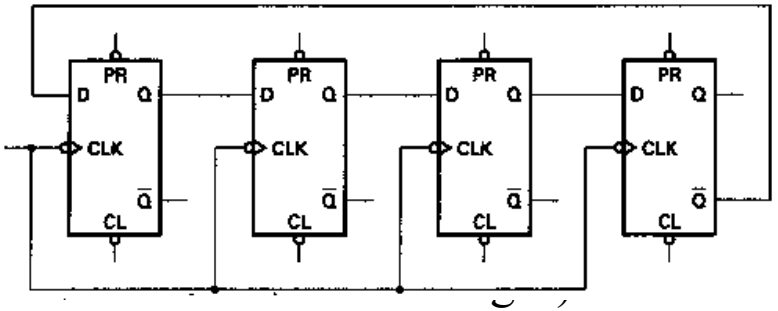




Counter Application

Johnson Counter



The Johnson counter
that changes by only
number of states (2*n*,

The first five counts for a 4-bit Johnson counter that is initially cleared are:

CLK	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1

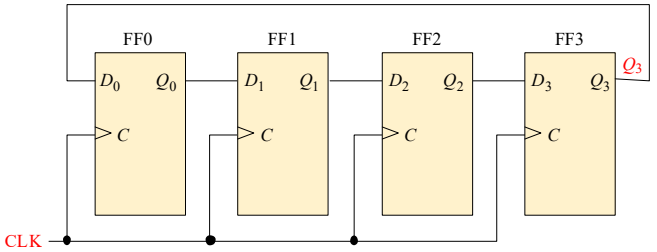
Question

What are the remaining 3 states?

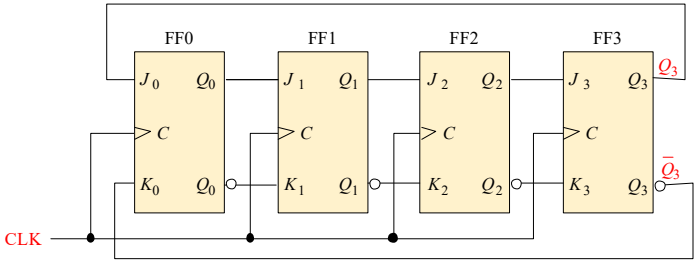
Ring Counter

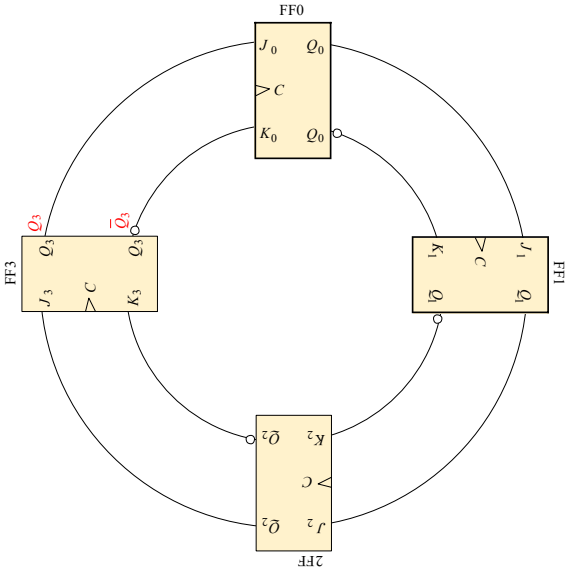
- **The ring counter can also be implemented with either D flip-flops or J-K flip-flops.**

Here is a 4-bit ring counter constructed from a series of D flip-flops. Notice the feedback.



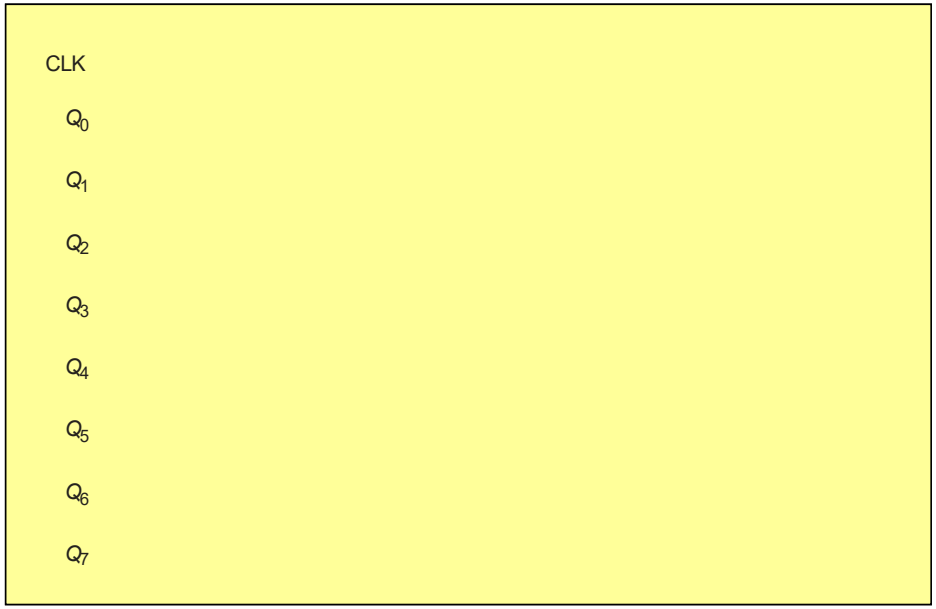
Like the Johnson counter, it can also be implemented with J-K flip flops.





Ring Counter

A common pattern for a ring counter is to load it with a single 1 or a single 0. The waveforms shown here are for an 8-bit ring counter with a single 1.



Homework

Thanks