

FEATURES

- Member of the Texas Instruments Widebus™ Family
- Operates From 2.7 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 8.5 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- All Outputs Have Equivalent 26- Ω Series Resistors, So No External Resistors Are Required
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

DESCRIPTION/ORDERING INFORMATION

This 16-bit (dual-octal) noninverting bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

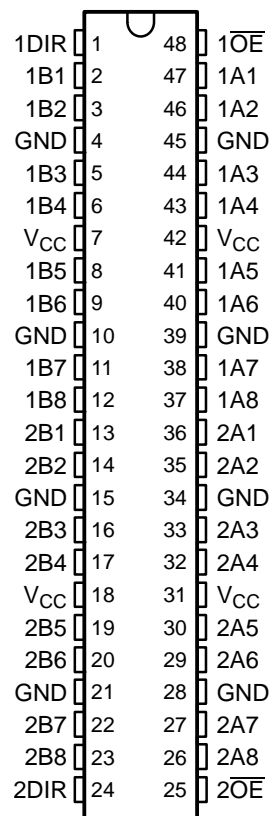
The SN74LVCR162245 is designed for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses effectively are isolated.

All outputs, which are designed to sink up to 12 mA, include 26- Ω resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended. The bus-hold circuitry is part of the input circuit and is not disabled by \overline{OE} or DIR.

DGG OR DL PACKAGE
(TOP VIEW)



ORDERING INFORMATION

| T_A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------------------|---------------|-----------------------|------------------|
| –40°C to 85°C | SSOP – DL | Tube | SN74LVCR162245DL | LVCR162245 |
| | | Tape and reel | SN74LVCR162245DLR | |
| | TSSOP – DGG | Tape and reel | SN74LVCR162245DGGR | LVCR162245 |
| | VFBGA – GQL | Tape and reel | SN74LVCR162245KR | LEP245 |
| | VFBGA – ZQL (Pb-free) | | 74LVCR162245ZQLR | |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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Widebus is a trademark of Texas Instruments.

SN74LVCR162245

16-BIT BUS TRANSCEIVER

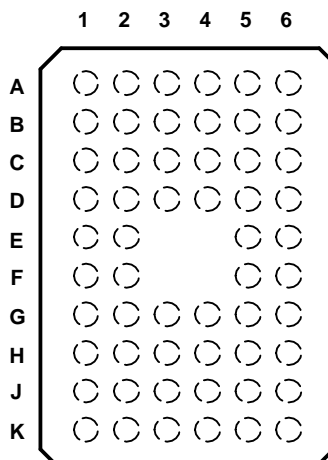
WITH 3-STATE OUTPUTS

SCES047E–AUGUST 1995–REVISED MARCH 2005

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**GQL OR ZQL PACKAGE
(TOP VIEW)**



TERMINAL ASSIGNMENTS⁽¹⁾

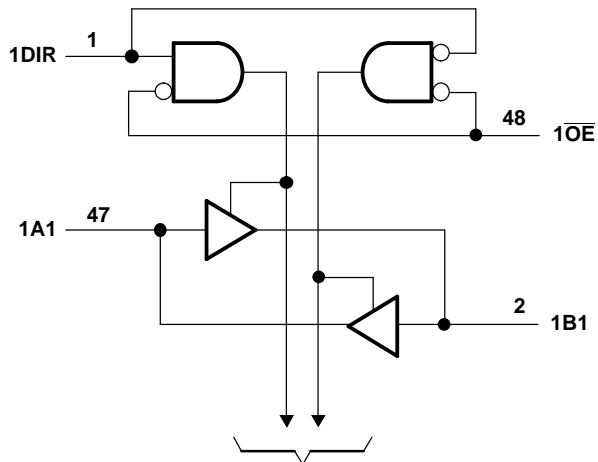
| | 1 | 2 | 3 | 4 | 5 | 6 |
|----------|------|-----|----------|----------|-----|-------------------|
| A | 1DIR | NC | NC | NC | NC | 1 \overline{OE} |
| B | 1B2 | 1B1 | GND | GND | 1A1 | 1A2 |
| C | 1B4 | 1B3 | V_{CC} | V_{CC} | 1A3 | 1A4 |
| D | 1B6 | 1B5 | GND | GND | 1A5 | 1A6 |
| E | 1B8 | 1B7 | | | 1A7 | 1A8 |
| F | 2B1 | 2B2 | | | 2A2 | 2A1 |
| G | 2B3 | 2B4 | GND | GND | 2A4 | 2A3 |
| H | 2B5 | 2B6 | V_{CC} | V_{CC} | 2A6 | 2A5 |
| J | 2B7 | 2B8 | GND | GND | 2A8 | 2A7 |
| K | 2DIR | NC | NC | NC | NC | 2 \overline{OE} |

(1) NC - No internal connection

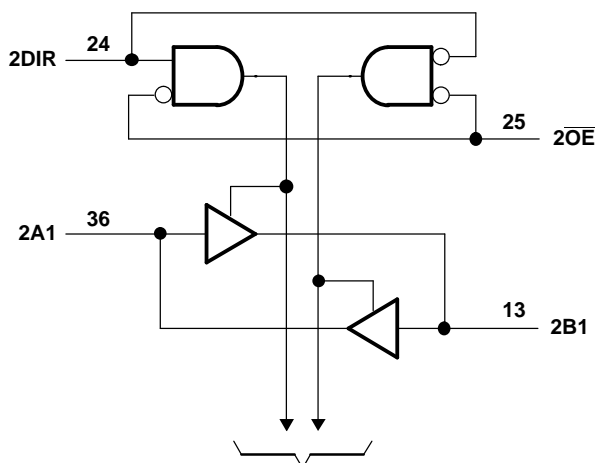
**FUNCTION TABLE
(EACH 8-BIT SECTION)**

| INPUTS | | OPERATION |
|-----------------|-----|-----------------|
| \overline{OE} | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

LOGIC DIAGRAM (POSITIVE LOGIC)



To Seven Other Channels



Pin numbers shown are for the DGG and DL packages.

SN74LVCR162245

16-BIT BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

SCES047E–AUGUST 1995–REVISED MARCH 2005

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---------------|--|---------------------------------|------|----------------|------|
| V_{CC} | Supply voltage range | | –0.5 | 4.6 | V |
| V_I | Input voltage range | Except I/O ports ⁽²⁾ | –0.5 | $V_{CC} + 4.6$ | V |
| | | I/O ports ⁽²⁾⁽³⁾ | –0.5 | $V_{CC} + 0.5$ | |
| V_O | Output voltage range ⁽²⁾⁽³⁾ | | –0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | Input clamp current | $V_I < 0$ | | –50 | mA |
| I_{OK} | Output clamp current | $V_O < 0$ or $V_O > V_{CC}$ | | ±50 | mA |
| I_O | Continuous output current | $V_O = 0$ to V_{CC} | | ±50 | mA |
| | Continuous current through V_{CC} or GND | | | ±100 | mA |
| θ_{JA} | Package thermal impedance ⁽⁴⁾ | DGG package | | 70 | °C/W |
| | | DL package | | 63 | |
| | | GQL/ZQL package | | 42 | |
| T_{stg} | Storage temperature range | | –65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

| | | | MIN | MAX | UNIT |
|---------------------|------------------------------------|---------------------------|-----|----------|------|
| V_{CC} | Supply voltage | | 2.7 | 3.6 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 2.7$ V to 3.6 V | 2 | | V |
| V_{IL} | Low-level input voltage | $V_{CC} = 2.7$ V to 3.6 V | | 0.8 | V |
| V_I | Input voltage | | 0 | V_{CC} | V |
| V_O | Output voltage | | 0 | V_{CC} | V |
| I_{OH} | High-level output current | $V_{CC} = 2.7$ V | | –8 | mA |
| | | $V_{CC} = 3$ V | | –12 | |
| I_{OL} | Low-level output current | $V_{CC} = 2.7$ V | | 8 | mA |
| | | $V_{CC} = 3$ V | | 12 | |
| $\Delta t/\Delta V$ | Input transition rise or fall rate | | | 10 | ns/V |
| T_A | Operating free-air temperature | | –40 | 85 | °C |

- (1) All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | V _{CC} ⁽¹⁾ | MIN | TYP ⁽²⁾ | MAX | UNIT |
|--------------------------------|--|---|--------------------|--------------------------------|-----------------------|--------------------|------|------|
| V _{OH} | I _{OH} = −100 μA | | | MIN to MAX | V _{CC} − 0.2 | | | V |
| | I _{OH} = −4 mA, | V _{IH} = 2 V | 2.7 V | 2.2 | | | | |
| | I _{OH} = −8 mA, | V _{IH} = 2 V | | 2 | | | | |
| | I _{OH} = −6 mA, | V _{IH} = 2 V | 3 V | 2.4 | | | | |
| | I _{OH} = −12 mA, | V _{IH} = 2 V | | 2 | | | | |
| V _{OL} | I _{OL} = 100 μA | | | MIN to MAX | | | 0.2 | V |
| | I _{OL} = 4 mA, | V _{IL} = 0.8 V | 2.7 V | | | 0.4 | | |
| | I _{OL} = 8 mA, | V _{IL} = 0.8 V | | | | 0.6 | | |
| | I _{OL} = 6 mA, | V _{IL} = 0.8 V | 3 V | | | 0.55 | | |
| | I _{OL} = 12 mA, | V _{IL} = 0.8 V | | | | 0.8 | | |
| I _I | V _I = V _{CC} or GND | | | 3.6 V | | | ±5 | μA |
| I _{I(hold)} | V _I = 0.8 V | | 3 V | 75 | | | μA | |
| | V _I = 2 V | | | −75 | | | | |
| | V _I = 0 to 3.6 V | | | 3.6 V | | | ±500 | μA |
| I _{OZ} ⁽³⁾ | V _O = 0 V or (V _{CC} to 5.5 V) | | | 3.6 V | | | ±10 | μA |
| I _{CC} | V _I = V _{CC} or GND | | I _O = 0 | 3.6 V | | | 20 | μA |
| | 3.6 V ≤ V _I ≤ 5.5 V ⁽⁴⁾ | | | | | | 20 | |
| ΔI _{CC} | One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND | | | | 2.7 V to 3.6 V | | | 500 |
| C _i | Control inputs | V _I = V _{CC} or GND | | 3.3 V | 2.5 | | | pF |
| C _{io} | A or B ports | V _O = V _{CC} or GND | | 3.3 V | 3.5 | | | pF |

(1) For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



(2) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(3) For the total leakage current in an I/O port, please consult the I_{I(hold)} specification for the input voltage condition 0 V < V_I < V_{CC}, and the I_{OZ} specification for the input voltage conditions V_I = 0 V or V_I = V_{CC} to 5.5 V. The bus-hold current, at input voltage greater than V_{CC}, is negligible.

(4) This applies in the disabled state only.

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

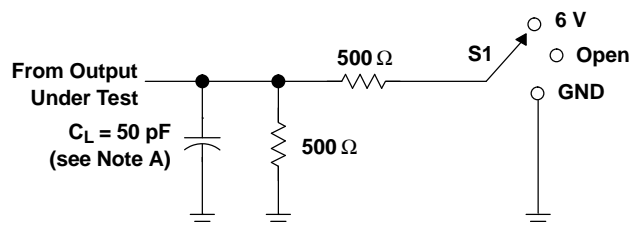
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 2.7 V | | UNIT |
|------------------|---|----------------|------------------------------------|-----|-------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| t _{pd} | A or B | B or A | 1.5 | 7.5 | 1.5 | 8.5 | ns |
| t _{en} |  | A or B | 1.5 | 9 | 1.5 | 10 | ns |
| t _{dis} |  | A or B | 1.5 | 7.5 | 1.5 | 8.5 | ns |

Operating Characteristics

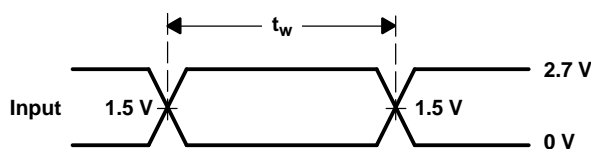
V_{CC} = 3.3 V, T_A = 25°C

| PARAMETER | | | TEST CONDITIONS | TYP | UNIT |
|-----------------|---|------------------|------------------------------------|-----|------|
| C _{pd} | Power dissipation capacitance per transceiver | Outputs enabled | C _L = 50 pF, f = 10 MHz | 20 | pF |
| | | Outputs disabled | | 2 | |

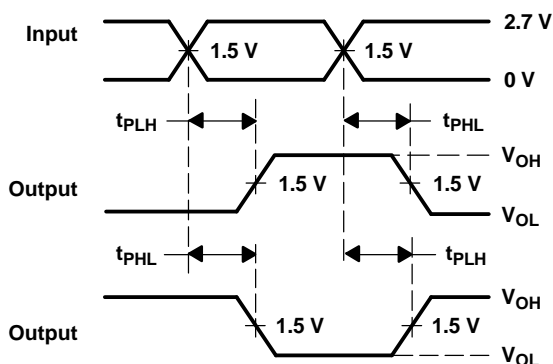
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS

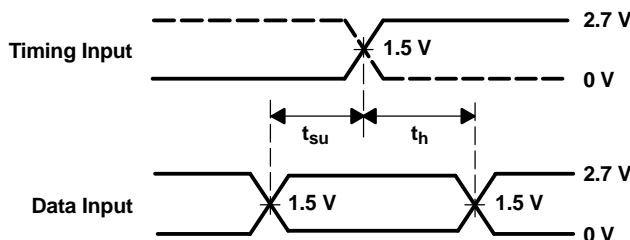


VOLTAGE WAVEFORMS
PULSE DURATION

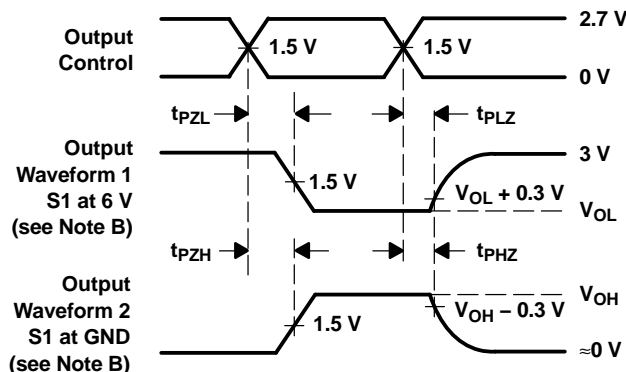


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 6 V |
| t_{PHZ}/t_{PZH} | GND |



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|--------------------|---------------|----------------------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| 74LVCR162245ZQLR | ACTIVE | BGA MICROSTAR JUNIOR | ZQL | 56 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | LEP245 | Samples |
| SN74LVCR162245DGGR | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVCR162245 | Samples |
| SN74LVCR162245DL | ACTIVE | SSOP | DL | 48 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVCR162245 | Samples |
| SN74LVCR162245DLR | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVCR162245 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|----------------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 74LVCR162245ZQLR | BGA MICROSTAR JUNIOR | ZQL | 56 | 1000 | 330.0 | 16.4 | 4.8 | 7.3 | 1.5 | 8.0 | 16.0 | Q1 |
| SN74LVCR162245DGGR | TSSOP | DGG | 48 | 2000 | 330.0 | 24.4 | 8.6 | 13.0 | 1.8 | 12.0 | 24.0 | Q1 |
| SN74LVCR162245DLR | SSOP | DL | 48 | 1000 | 330.0 | 32.4 | 11.35 | 16.2 | 3.1 | 16.0 | 32.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

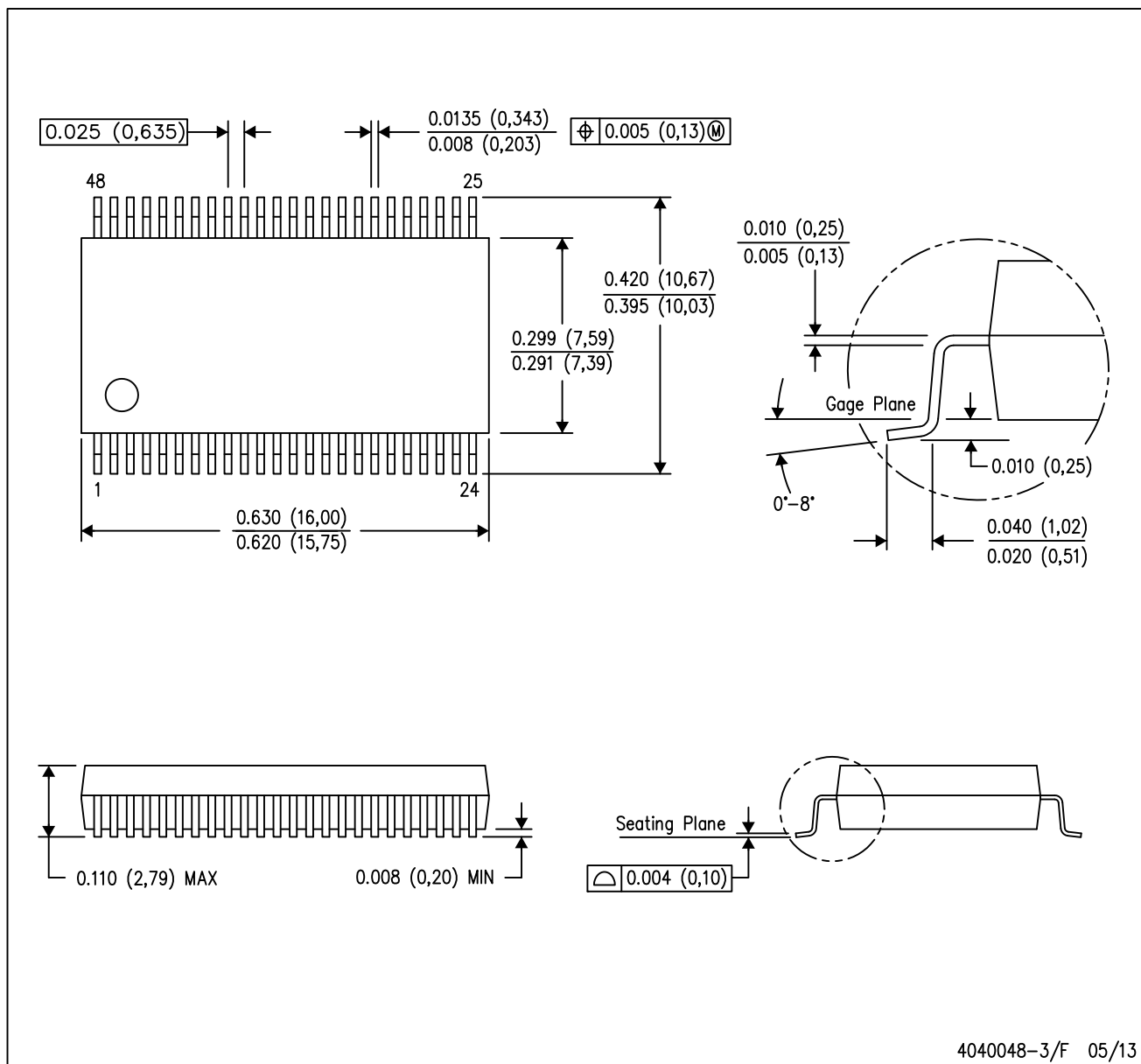


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------|----------------------|-----------------|------|------|-------------|------------|-------------|
| 74LVCR162245ZQLR | BGA MICROSTAR JUNIOR | ZQL | 56 | 1000 | 350.0 | 350.0 | 43.0 |
| SN74LVCR162245DGGR | TSSOP | DGG | 48 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LVCR162245DLR | SSOP | DL | 48 | 1000 | 367.0 | 367.0 | 55.0 |

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE

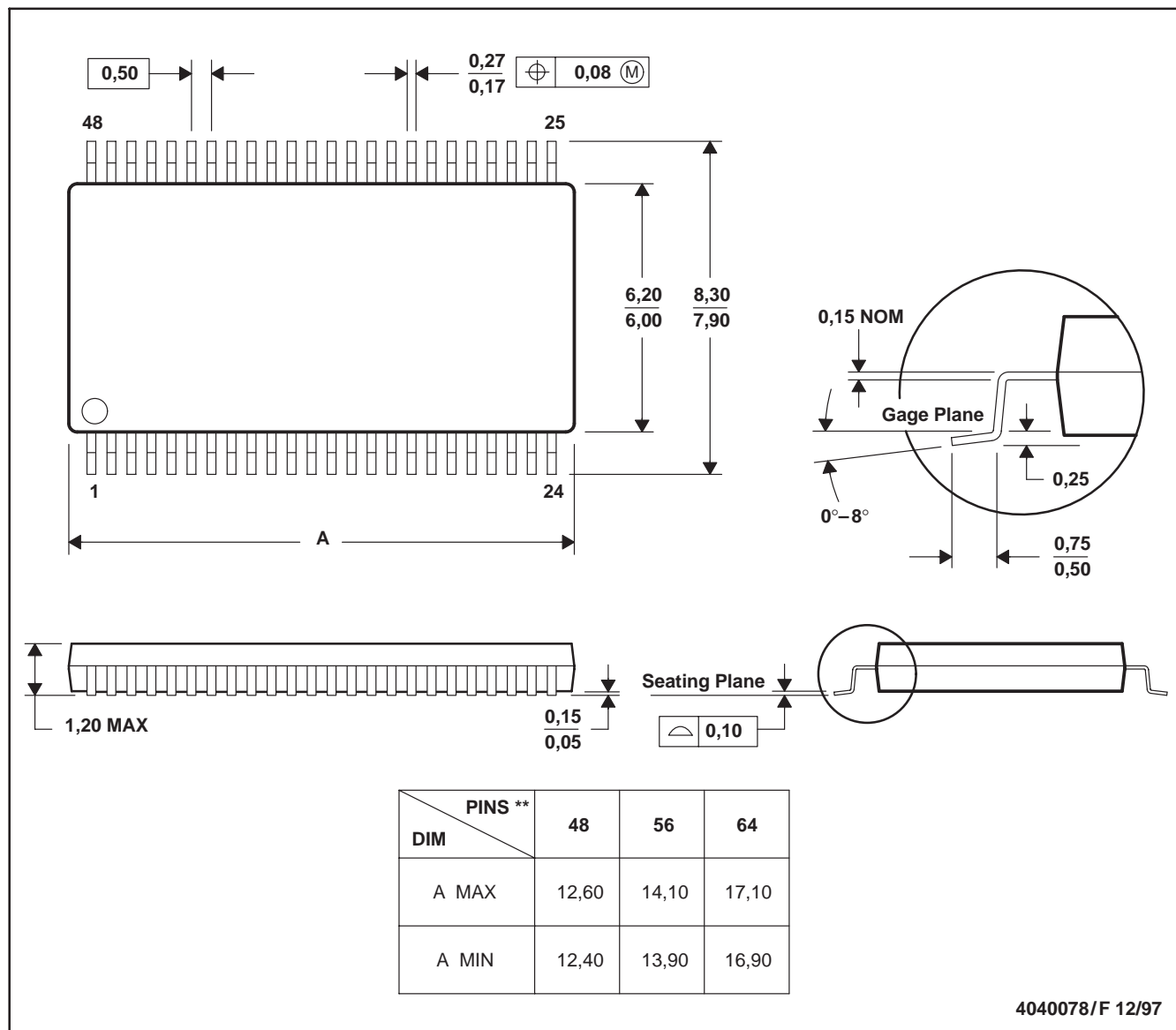


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118

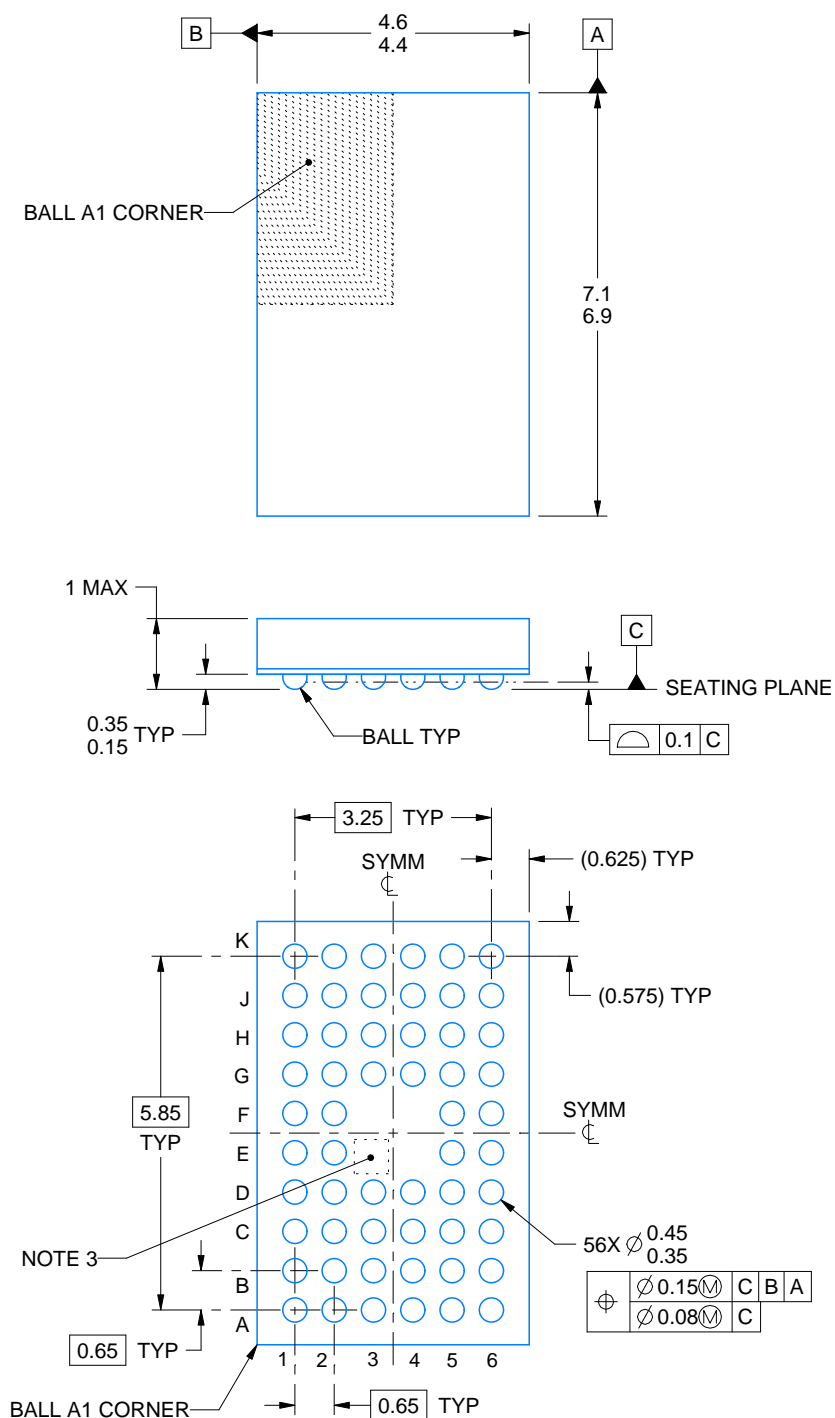
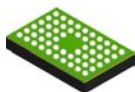
DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153



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NOTES:

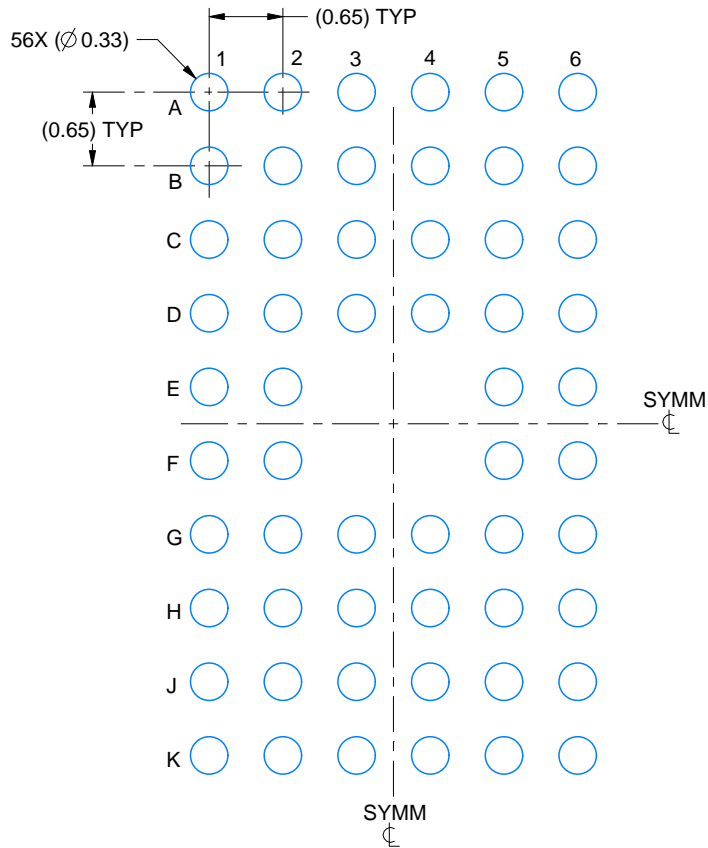
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. No metal in this area, indicates orientation.

EXAMPLE BOARD LAYOUT

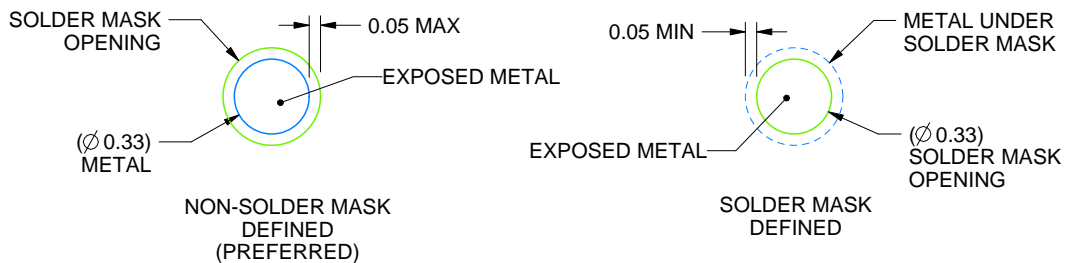
ZQL0056A

JRBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

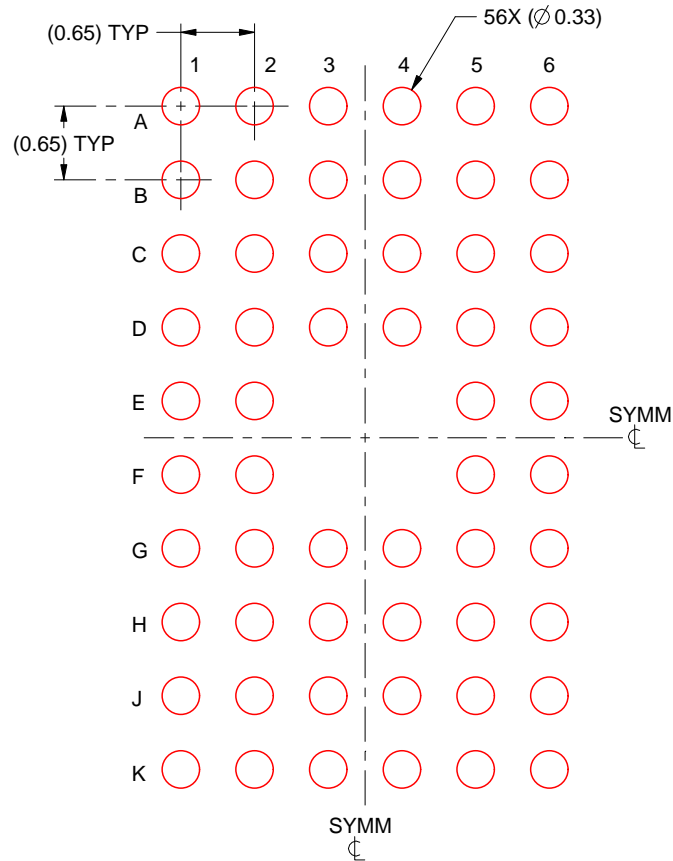
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

EXAMPLE STENCIL DESIGN

ZQL0056A

JRBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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