1. Description

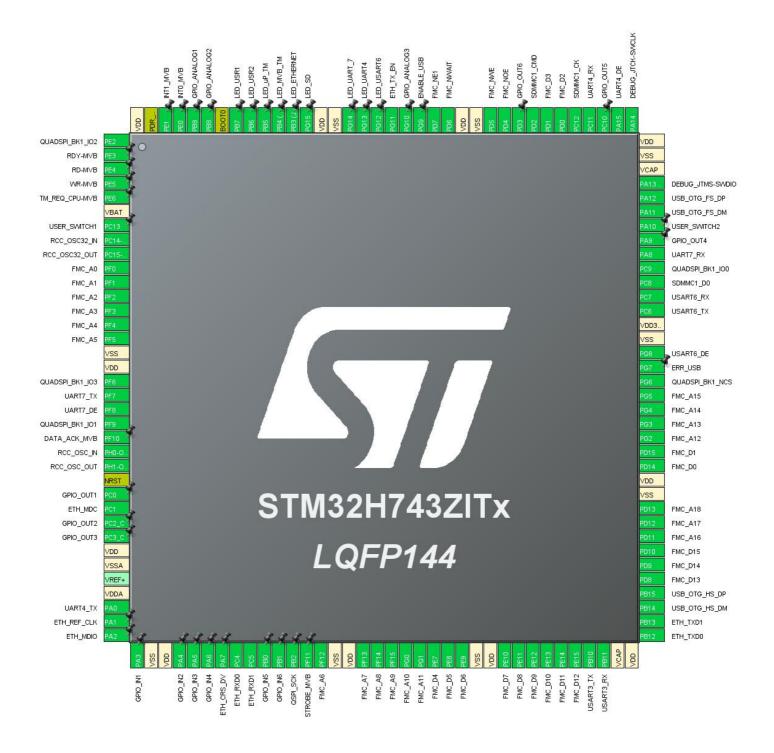
1.1. Project

Project Name	STM32 Project
Board Name	custom
Generated with:	STM32CubeMX 5.6.1
Date	07/18/2020

1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H743/753
MCU name	STM32H743ZITx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



3. Pins Configuration

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP144	(function after		Function(s)	
	reset)			
1	PE2	I/O	QUADSPI_BK1_IO2	
2	PE3 *	I/O	GPIO_Input	RDY-MVB
3	PE4 *	I/O	GPIO_Output	RD-MVB
4	PE5 *	I/O	GPIO_Output	WR-MVB
5	PE6 *	I/O	GPIO_Output	TM_REQ_CPU-MVB
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Input	USER_SWITCH1
8	PC14-OSC32_IN (OSC32_IN)	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT (OSC32_OUT)	I/O	RCC_OSC32_OUT	
10	PF0	I/O	FMC_A0	
11	PF1	I/O	FMC_A1	
12	PF2	I/O	FMC_A2	
13	PF3	I/O	FMC_A3	
14	PF4	I/O	FMC_A4	
15	PF5	I/O	FMC_A5	
16	VSS	Power		
17	VDD	Power		
18	PF6	I/O	QUADSPI_BK1_IO3	
19	PF7	I/O	UART7_TX	
20	PF8	I/O	UART7_DE	
21	PF9	I/O	QUADSPI_BK1_IO1	
22	PF10 *	I/O	GPIO_Input	DATA_ACK_MVB
23	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
24	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
25	NRST	Reset		
26	PC0 *	I/O	GPIO_Output	GPIO_OUT1
27	PC1	I/O	ETH_MDC	
28	PC2_C *	I/O	GPIO_Output	GPIO_OUT2
29	PC3_C *	I/O	GPIO_Output	GPIO_OUT3
30	VDD	Power		
31	VSSA	Power		
33	VDDA	Power		
34	PA0	I/O	UART4_TX	
35	PA1	I/O	ETH_REF_CLK	

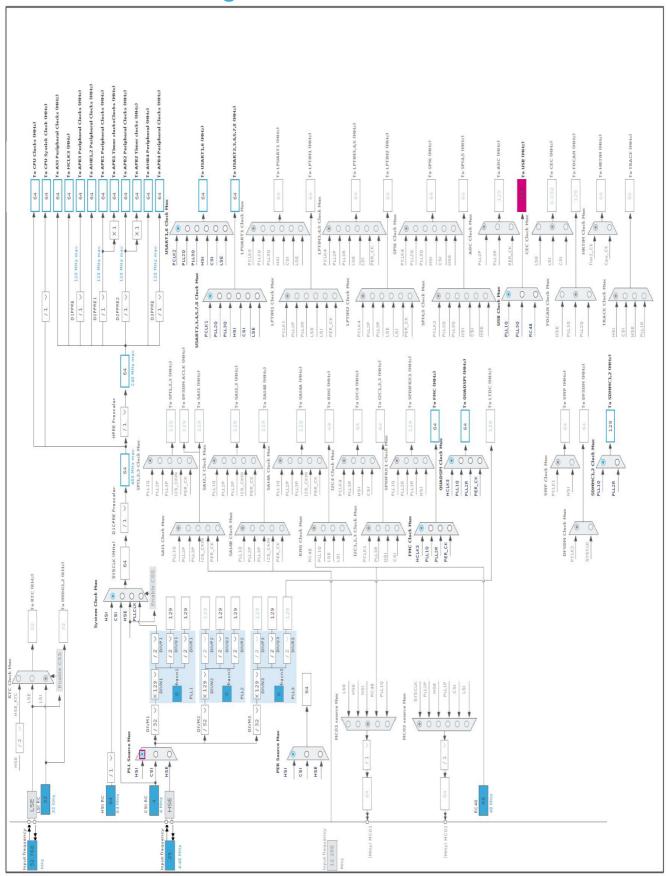
49 PF11 * I/O GPIO_Input ST 50 PF12 I/O FMC_A6 ST 51 VSS Power Power ST Power ST ST POWER POWER ST POWER POWER ST POWER POWER <t< th=""><th>GPIO_IN1 GPIO_IN2 GPIO_IN3 GPIO_IN4 GPIO_IN5 GPIO_IN6 QSPI_SCK TROBE_MVB</th></t<>	GPIO_IN1 GPIO_IN2 GPIO_IN3 GPIO_IN4 GPIO_IN5 GPIO_IN6 QSPI_SCK TROBE_MVB
PA2	GPIO_IN2 GPIO_IN3 GPIO_IN4 GPIO_IN5 GPIO_IN6 QSPI_SCK
36	GPIO_IN2 GPIO_IN3 GPIO_IN4 GPIO_IN5 GPIO_IN6 QSPI_SCK
37	GPIO_IN2 GPIO_IN3 GPIO_IN4 GPIO_IN5 GPIO_IN6 QSPI_SCK
38	GPIO_IN2 GPIO_IN3 GPIO_IN4 GPIO_IN5 GPIO_IN6 QSPI_SCK
A0	GPIO_IN3 GPIO_IN4 GPIO_IN5 GPIO_IN6 QSPI_SCK
A1	GPIO_IN3 GPIO_IN4 GPIO_IN5 GPIO_IN6 QSPI_SCK
Mathematical Page Math	GPIO_IN5 GPIO_IN6 QSPI_SCK
Harmonia Harmonia	GPIO_IN5 GPIO_IN6 QSPI_SCK
A44	GPIO_IN6 QSPI_SCK
A5	GPIO_IN6 QSPI_SCK
46 PB0 * I/O GPIO_Input 47 PB1 * I/O GPIO_Input 48 PB2 I/O QUADSPI_CLK 49 PF11 * I/O GPIO_Input ST 50 PF12 I/O FMC_A6 51 VSS Power 52 VDD Power 53 PF13 I/O FMC_A7 54 PF14 I/O FMC_A8 55 PF15 I/O FMC_A9 56 PG0 I/O FMC_A10 57 PG1 I/O FMC_A11 58 PE7 I/O FMC_D4 59 PE8 I/O FMC_D5 60 PE9 I/O FMC_D6 61 VSS Power 62 VDD Power	GPIO_IN6 QSPI_SCK
Heat	GPIO_IN6 QSPI_SCK
48 PB2 I/O QUADSPI_CLK 49 PF11 * I/O GPIO_Input S* 50 PF12 I/O FMC_A6 S* 51 VSS Power Power S* 52 VDD Power Power PMC_A7 PMC_A7 PMC_A7 PMC_A8 PMC_A8 PMC_A9 PMC_A9 PMC_A9 PMC_A10 PMC_A10 PMC_A10 PMC_A11 PMC_A11 PMC_A11 PMC_A11 PMC_A11 PMC_D4 PMC_D4 PMC_D5 PMC_D5 PMC_D5 PMC_D6	QSPI_SCK
49 PF11 * I/O GPIO_Input ST 50 PF12 I/O FMC_A6 51 VSS Power 52 VDD Power 53 PF13 I/O FMC_A7 54 PF14 I/O FMC_A8 55 PF15 I/O FMC_A9 56 PG0 I/O FMC_A10 57 PG1 I/O FMC_A11 58 PE7 I/O FMC_D4 59 PE8 I/O FMC_D5 60 PE9 I/O FMC_D6 61 VSS Power 62 VDD Power	
50 PF12 I/O FMC_A6 51 VSS Power 52 VDD Power 53 PF13 I/O FMC_A7 54 PF14 I/O FMC_A8 55 PF15 I/O FMC_A9 56 PG0 I/O FMC_A10 57 PG1 I/O FMC_A11 58 PE7 I/O FMC_D4 59 PE8 I/O FMC_D5 60 PE9 I/O FMC_D6 61 VSS Power 62 VDD Power	TROBE_MVB
51 VSS Power 52 VDD Power 53 PF13 I/O FMC_A7 54 PF14 I/O FMC_A8 55 PF15 I/O FMC_A9 56 PG0 I/O FMC_A10 57 PG1 I/O FMC_A11 58 PE7 I/O FMC_D4 59 PE8 I/O FMC_D5 60 PE9 I/O FMC_D6 61 VSS Power 62 VDD Power	
52 VDD Power 53 PF13 I/O FMC_A7 54 PF14 I/O FMC_A8 55 PF15 I/O FMC_A9 56 PG0 I/O FMC_A10 57 PG1 I/O FMC_A11 58 PE7 I/O FMC_D4 59 PE8 I/O FMC_D5 60 PE9 I/O FMC_D6 61 VSS Power 62 VDD Power	
53 PF13 I/O FMC_A7 54 PF14 I/O FMC_A8 55 PF15 I/O FMC_A9 56 PG0 I/O FMC_A10 57 PG1 I/O FMC_A11 58 PE7 I/O FMC_D4 59 PE8 I/O FMC_D5 60 PE9 I/O FMC_D6 61 VSS Power 62 VDD Power	
54 PF14 I/O FMC_A8 55 PF15 I/O FMC_A9 56 PG0 I/O FMC_A10 57 PG1 I/O FMC_A11 58 PE7 I/O FMC_D4 59 PE8 I/O FMC_D5 60 PE9 I/O FMC_D6 61 VSS Power 62 VDD Power	
55 PF15 I/O FMC_A9 56 PG0 I/O FMC_A10 57 PG1 I/O FMC_A11 58 PE7 I/O FMC_D4 59 PE8 I/O FMC_D5 60 PE9 I/O FMC_D6 61 VSS Power 62 VDD Power	
56 PG0 I/O FMC_A10 57 PG1 I/O FMC_A11 58 PE7 I/O FMC_D4 59 PE8 I/O FMC_D5 60 PE9 I/O FMC_D6 61 VSS Power 62 VDD Power	
57 PG1 I/O FMC_A11 58 PE7 I/O FMC_D4 59 PE8 I/O FMC_D5 60 PE9 I/O FMC_D6 61 VSS Power 62 VDD Power	
58 PE7 I/O FMC_D4 59 PE8 I/O FMC_D5 60 PE9 I/O FMC_D6 61 VSS Power 62 VDD Power	
59 PE8 I/O FMC_D5 60 PE9 I/O FMC_D6 61 VSS Power 62 VDD Power	
60 PE9 I/O FMC_D6 61 VSS Power 62 VDD Power	
61 VSS Power 62 VDD Power	
62 VDD Power	
63 PE10 I/O FMC_D7	
64 PE11 I/O FMC_D8	
65 PE12 I/O FMC_D9	
66 PE13 I/O FMC_D10	
67 PE14 I/O FMC_D11	
68 PE15 I/O FMC_D12	
69 PB10 I/O USART3_TX	
70 PB11 I/O USART3_RX	
71 VCAP Power	
72 VDD Power	
73 PB12 I/O ETH_TXD0	
74 PB13 I/O ETH_TXD1	

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP144	(function after		Function(s)	
	reset)			
75	PB14	I/O	USB_OTG_HS_DM	
76	PB15	I/O	USB_OTG_HS_DP	
77	PD8	I/O	FMC_D13	
78	PD9	I/O	FMC_D14	
79	PD10	I/O	FMC_D15	
80	PD11	I/O	FMC_A16	
81	PD12	I/O	FMC_A17	
82	PD13	I/O	FMC_A18	
83	VSS	Power	,o_,o	
84	VDD	Power		
85	PD14	I/O	FMC_D0	
86	PD15	I/O	FMC_D1	
87	PG2	I/O	FMC_A12	
88	PG3	I/O	FMC_A13	
89	PG4	I/O	FMC_A14	
90	PG5	I/O	FMC_A15	
91	PG6	I/O	QUADSPI_BK1_NCS	
92	PG7 *	I/O	GPIO_Input	ERR_USB
93	PG8	I/O	USART6_DE	
94	VSS	Power	00/11/10_22	
95	VDD33_USB	Power		
96	PC6	I/O	USART6_TX	
97	PC7	I/O	USART6_RX	
98	PC8	I/O	SDMMC1_D0	
99	PC9	I/O	QUADSPI_BK1_IO0	
100	PA8	I/O	UART7_RX	
101	PA9 *	I/O	GPIO_Output	GPIO_OUT4
102	PA10 *	I/O	GPIO_Input	USER_SWITCH2
103	PA11	I/O	USB_OTG_FS_DM	
104	PA12	I/O	USB_OTG_FS_DP	
105	PA13 (JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
106	VCAP	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14 (JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
110	PA15 (JTDI)	I/O	UART4_DE	
111	PC10 *	I/O	GPIO_Output	GPIO_OUT5
112	PC11	I/O	UART4_RX	-
113	PC12	I/O	SDMMC1_CK	
	•	•		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
111	,	I/O	FMC D2	
114	PD0		FMC_D2	
115	PD1	1/0	FMC_D3	
116	PD2 PD3 *	1/0	SDMMC1_CMD	CDIO OLITO
117		1/0	GPIO_Output	GPIO_OUT6
118	PD4	1/0	FMC_NOE	
119	PD5	1/0	FMC_NWE	
120	VSS	Power		
121	VDD	Power	FMO NIMAT	
122	PD6	1/0	FMC_NWAIT	
123	PD7	1/0	FMC_NE1	55. 555
124	PG9 *	1/0	GPIO_Output	ENABLE_USB
125	PG10 *	I/O	GPIO_Analog	GPIO_ANALOG3
126	PG11	I/O	ETH_TX_EN	
127	PG12 *	I/O	GPIO_Output	LED_USART6
128	PG13 *	I/O	GPIO_Output	LED_UART4
129	PG14 *	I/O	GPIO_Output	LED_UART_7
130	VSS	Power		
131	VDD	Power		
132	PG15 *	I/O	GPIO_Output	LED_SD
133	PB3 (JTDO/TRACESWO) *	I/O	GPIO_Output	LED_ETHERNET
134	PB4 (NJTRST) *	I/O	GPIO_Output	LED_MVB_TM
135	PB5 *	I/O	GPIO_Output	LED_uP_TM
136	PB6 *	I/O	GPIO_Output	LED_USR2
137	PB7 *	I/O	GPIO_Output	LED_USR1
138	BOOT0	Boot		
139	PB8 *	I/O	GPIO_Analog	GPIO_ANALOG2
140	PB9 *	I/O	GPIO_Analog	GPIO_ANALOG1
141	PE0 *	I/O	GPIO_Input	INT0_MVB
142	PE1 *	I/O	GPIO_Input	INT1_MVB
143	PDR_ON	Reset		
144	VDD	Power		

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



Page 7

5. Software Project

5.1. Project Settings

Name	Value	
Project Name	STM32 Project	
Project Folder	/mnt/Shared/GitHub/Repos/TesisCESE/STM32 Project	
Toolchain / IDE	EWARM V8.32	
Firmware Package Name and Version	STM32Cube FW_H7 V1.7.0	

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H743/753
MCU	STM32H743ZITx
Datasheet	DS12110_Rev5

6.2. Parameter Selection

Temperature	25
IVAA	3.0

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

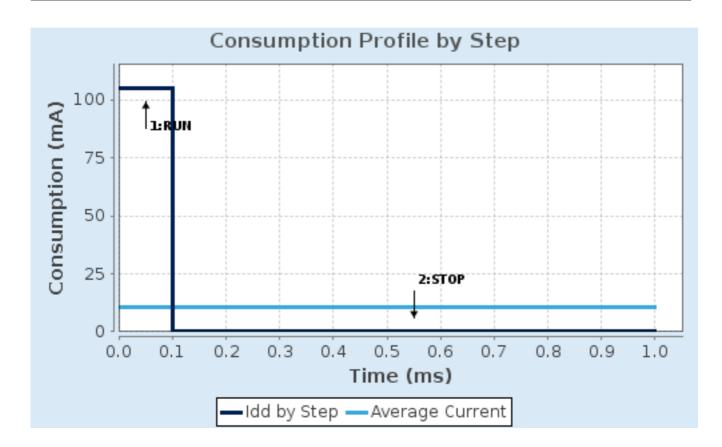
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS1: Scale1-High	SVOS5: System-Scale5
D1 Mode	DRUN/CRUN	DSTANDBY
D2 Mode	DSTANDBY	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	FLASH A	NA
CPU Frequency	400 MHz	0 Hz
Clock Configuration	HSE BYP PLL Flash-ON	Flash-LP
	Cache-ON	
Clock Source Frequency	25 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	105 mA	170 μΑ
Duration	0.1 ms	0.9 ms
DMIPS	856.0	0.0
Ta Max	111.14	124.98
Category	In DS Table	In DS Table

6.5. RESULTS

Sequence Time	1 ms	Average Current	10.65 mA
Battery Life	2 days, 10 hours	Average DMIPS	856.0 DMIPS

6.6. Chart



7. IPs and Middleware Configuration 7.1. DEBUG

Debug: Serial Wire

7.2. ETH

Mode: RMII

7.2.1. Parameter Settings:

General: Ethernet Configuration:

Warning The ETH can work only when RAM is pointing at 0x24000000

Note PHY Driver must be configured from the LwIP 'Platform Settings' top right tab

Ethernet MAC Address 00:80:E1:00:00:00

Tx Descriptor Length 4

First Tx Descriptor Address 0x30040060 *

Rx Descriptor Length 4

First Rx Descriptor Address 0x30040000 *
Rx Buffers Address 0x30040200 *

Rx Buffers Length 1524

7.3. FMC

NOR Flash/PSRAM/SRAM/ROM/LCD 1

Chip Select: NE1

Memory type: SRAM

Address: 19 bits

Data: 16 bits

Wait: Asynchronous 7.3.1. NOR/PSRAM 1:

NOR/PSRAM control:

Memory type SRAM

Bank 1 NOR/PSRAM 1

Write operation Disabled
Write FIFO Enabled
Extended mode Disabled
Wait signal polarity Low polarity

NOR/PSRAM timing:

Address setup time in HCLK clock cycles 15

Data setup time in HCLK clock cycles 255

Bus turn around time in HCLK clock cycles 15

7.3.2. Bank Mapping:

Mapping parameters:

FMC bank mapping Default mapping

7.4. GPIO

7.5. QUADSPI

QuadSPI Mode: Bank1 with Quad SPI Lines

7.5.1. Parameter Settings:

General Parameters:

Clock Prescaler 255
Fifo Threshold 1

Sample Shifting No Sample Shifting

Flash Size 1

 Chip Select High Time
 1 Cycle

 Clock Mode
 Low

 Flash ID
 Flash ID 1

 Dual Flash
 Disabled

7.6. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.6.1. Parameter Settings:

SupplySource PWR_LDO_SUPPLY

RCC Parameters:

TIM Prescaler Selection Disabled
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000
CSI Calibration Value 16

HSI Calibration Value 32

System Parameters:

VDD voltage (V) 3.3

Flash Latency(WS) 0 WS (1 CPU cycle)

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 3

PLL range Parameters:

PLL1 clock Input range Between 2 and 4 MHz
PLL1 clock Output range Wide VCO range

7.7. SDMMC1

Mode: SD 1 bit

7.7.1. Parameter Settings:

SDMMC parameters:

Clock transition on which the bit capture is made Rising transition

SDMMC Clock output enable when the bus is idle

Disable the power save for the clock

SDMMC hardware flow control

The hardware control flow is disabled

SDMMC clock divide factor 0
Is external transceiver present ? no

7.8. SYS

Timebase Source: SysTick

7.9. UART4

Mode: Asynchronous

mode: Hardware Flow Control (RS485)

7.9.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable
ClockPrescaler clock /1

Fifo Mode FIFO mode disable

Txfifo Threshold 1 eighth full configuration

Rxfifo Threshold 1 eighth full configuration

Polarity High
Assertion Time 0
Deassertion Time 0

Advanced Features:

Auto Baudrate Disable TX Pin Active Level Inversion Disable RX Pin Active Level Inversion Disable Disable **Data Inversion** Disable TX and RX Pins Swapping Overrun Enable DMA on RX Error Enable MSB First Disable

7.10. UART7

Mode: Asynchronous

mode: Hardware Flow Control (RS485)

7.10.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable
ClockPrescaler clock /1

Fifo Mode FIFO mode disable

Txfifo Threshold 1 eighth full configuration

Rxfifo Threshold 1 eighth full configuration

Polarity High
Assertion Time 0
Deassertion Time 0

Advanced Features:

Auto Baudrate Disable TX Pin Active Level Inversion Disable **RX Pin Active Level Inversion** Disable Disable Data Inversion TX and RX Pins Swapping Disable Enable Overrun DMA on RX Error Enable MSB First Disable

7.11. USART3

Mode: Asynchronous

7.11.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable
ClockPrescaler clock /1
Fifo Mode Disable

Txfifo Threshold 1 eighth full configuration
Rxfifo Threshold 1 eighth full configuration

Advanced Features:

Auto Baudrate Disable TX Pin Active Level Inversion Disable **RX Pin Active Level Inversion** Disable Disable **Data Inversion** TX and RX Pins Swapping Disable Enable Overrun DMA on RX Error Enable MSB First Disable

7.12. USART6

Mode: Asynchronous

mode: Hardware Flow Control (RS485)

7.12.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable
ClockPrescaler clock /1
Fifo Mode Disable

Txfifo Threshold 1 eighth full configuration Rxfifo Threshold 1 eighth full configuration

Polarity High
Assertion Time 0
Deassertion Time 0

Advanced Features:

Auto Baudrate Disable TX Pin Active Level Inversion Disable **RX Pin Active Level Inversion** Disable Data Inversion Disable Disable TX and RX Pins Swapping Overrun Enable DMA on RX Error Enable MSB First Disable

7.13. USB_OTG_FS

Mode: Device_Only

7.13.1. Parameter Settings:

Speed Full Speed 12MBit/s

Enable internal IP DMA Disabled
Low power Disabled
Battery charging Disabled

Link Power Management Disabled
Use dedicated end point 1 interrupt Disabled
VBUS sensing Disabled
Signal start of frame Disabled

7.14. USB_OTG_HS

Internal FS Phy: Host_Only 7.14.1. Parameter Settings:

Speed Host Full Speed 12MBit/s

Enable internal IP DMA Disabled

Physical interface Internal Phy

Signal start of frame Disabled

^{*} User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DEBUG	PA13 (JTMS/SWDI O)	DEBUG_JTMS- SWDIO	n/a	n/a	n/a	
	PA14 (JTCK/SWC LK)	DEBUG_JTCK- SWCLK	n/a	n/a	n/a	
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB12	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	Low	
FMC	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD11	FMC_A16	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD12	FMC_A17	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD13	FMC_A18	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG2	FMC_A12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG3	FMC_A13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG4	FMC_A14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG5	FMC_A15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD4	FMC_NOE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD5	FMC_NWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD6	FMC_NWAIT	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD7	FMC_NE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
QUADSPI	PE2	QUADSPI_BK1_I		No pull-up and no pull-down	Low	
		O2				
	PF6	QUADSPI_BK1_I O3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF9	QUADSPI_BK1_I O1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB2	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	QSPI_SCK
	PG6	QUADSPI_BK1_ NCS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC9	QUADSPI_BK1_I O0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
RCC	PC14- OSC32_IN (OSC32_IN)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15- OSC32_OU T	RCC_OSC32_O UT	n/a	n/a	n/a	
	PH0- OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1- OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SDMMC1	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
UART4	PA0	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA15 (JTDI)	UART4_DE	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC11	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART7	PF7	UART7_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF8	UART7_DE	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA8	UART7_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART3	PB10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART6	PG8	USART6_DE	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC6	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USB_OTG_ FS	PA11	USB_OTG_FS_ DM	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA12	USB_OTG_FS_ DP	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USB_OTG_ HS	PB14	USB_OTG_HS_ DM	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB15	USB_OTG_HS_ DP	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PE3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	RDY-MVB
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RD-MVB
	PE5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	WR-MVB
	PE6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TM_REQ_CPU-MVB
	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USER_SWITCH1
	PF10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DATA_ACK_MVB
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO_OUT1
	PC2_C	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO_OUT2
	PC3_C	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO_OUT3
	PA3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	GPIO_IN1
	PA4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	GPIO_IN2
	PA5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	GPIO_IN3
	PA6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	GPIO_IN4
	PB0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	GPIO_IN5
	PB1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	GPIO_IN6
	PF11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	STROBE_MVB
	PG7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ERR_USB
	PA9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO_OUT4
	PA10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USER_SWITCH2
	PC10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO_OUT5
	PD3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO_OUT6
	PG9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ENABLE_USB

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PG10	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	GPIO_ANALOG3
	PG12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_USART6
	PG13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_UART4
	PG14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_UART_7
	PG15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_SD
	PB3 (JTDO/TRA CESWO)	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_ETHERNET
	PB4 (NJTRST)	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_MVB_TM
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_uP_TM
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_USR2
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_USR1
	PB8	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	GPIO_ANALOG2
	PB9	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	GPIO_ANALOG1
	PE0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	INT0_MVB
	PE1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	INT1_MVB

8.2. DMA configuration

DMA request	Stream	Direction	Priority
MEMTOMEM	DMA1_Stream0	Memory To Memory	Low

MEMTOMEM: DMA1_Stream0 DMA request Settings:

Mode: Normal

Use fifo: Enable *

FIFO Threshold: Full

Src Memory Increment: Enable *

Dst Memormy Increment: Enable *

Src Memory Data Width: Byte
Dst Memormy Data Width: Byte
Src Memory Burst Size: Single
Dst Memormy Burst Size: Single

8.3. BDMA configuration

nothing configured in DMA service

8.4. MDMA configuration

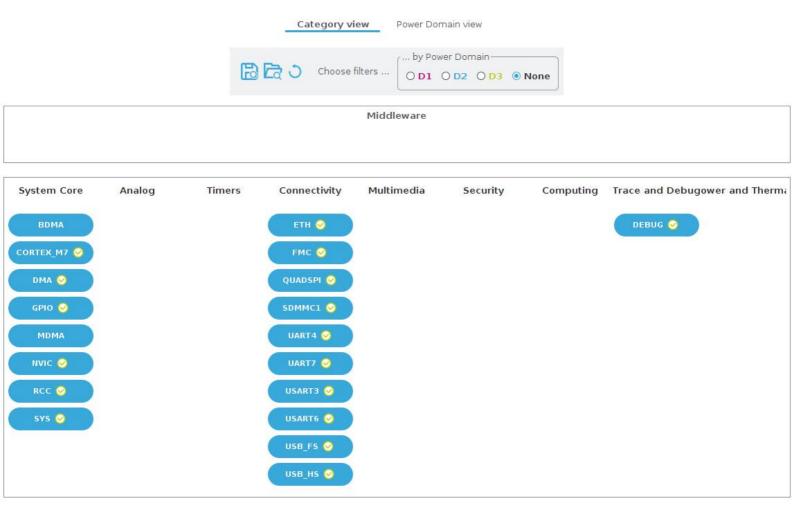
nothing configured in DMA service

8.5. NVIC configuration

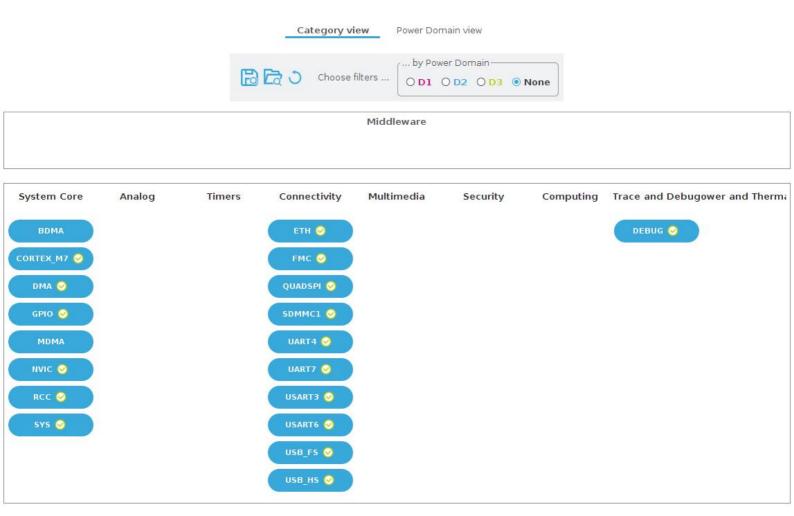
Interrupt Table	Enable	Preenmption Priority	SubPriority		
Non maskable interrupt	true	0	0		
Hard fault interrupt	true	0	0		
Memory management fault	true	0	0		
Pre-fetch fault, memory access fault	true	0	0		
Undefined instruction or illegal state	true	0	0		
System service call via SWI instruction	true	0	0		
Debug monitor	true	0	0		
Pendable request for system service	true	0	0		
System tick timer	true	0	0		
PVD and AVD interrupts through EXTI line 16		unused			
Flash global interrupt		unused			
RCC global interrupt		unused			
DMA1 stream0 global interrupt		unused			
USART3 global interrupt	unused				
SDMMC1 global interrupt	unused				
UART4 global interrupt	unused				
Ethernet global interrupt	unused unused unused				
Ethernet wake-up interrupt through EXTI line 86					
USART6 global interrupt					
USB On The Go HS End Point 1 Out global interrupt		unused			
USB On The Go HS End Point 1 In global interrupt		unused			
USB On The Go HS global interrupt	unused unused				
FPU global interrupt					
UART7 global interrupt	unused				
QUADSPI global interrupt	unused				
USB On The Go FS End Point 1 Out global interrupt	unused				
USB On The Go FS End Point 1 In global interrupt		unused			
USB On The Go FS global interrupt		unused			
HSEM1 global interrupt		unused			

* User modified value

9. Predefined Views - Category view : Current



10. Predefined Views - Category view : Without filters



11. Predefined Views - Power Domain view

Category view



Power Domain view

12. Software Pack Report