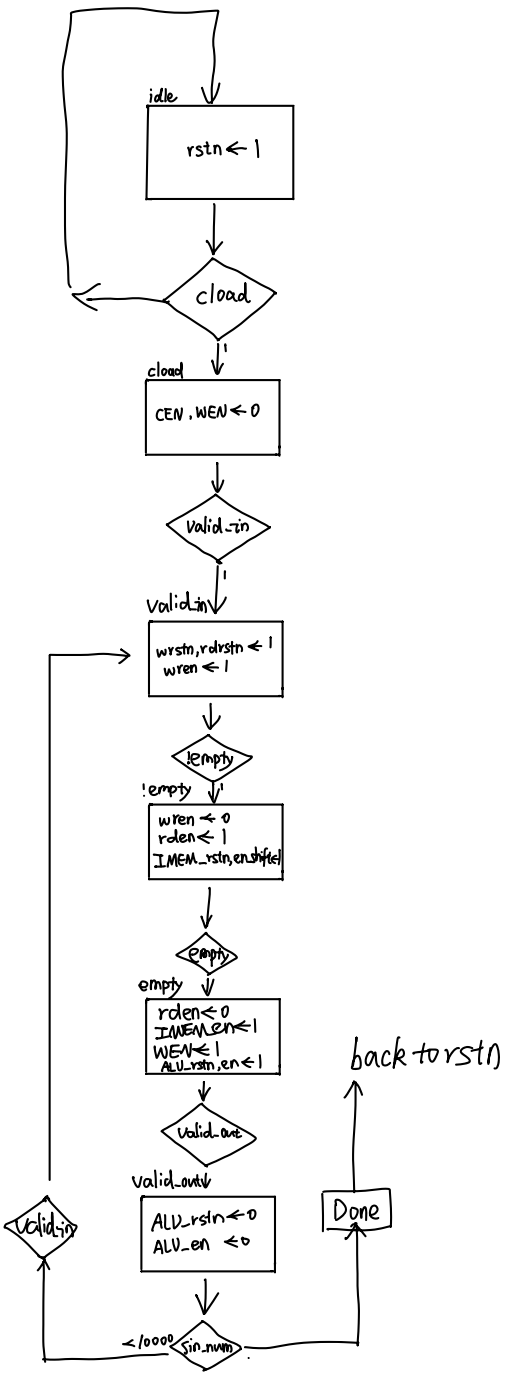
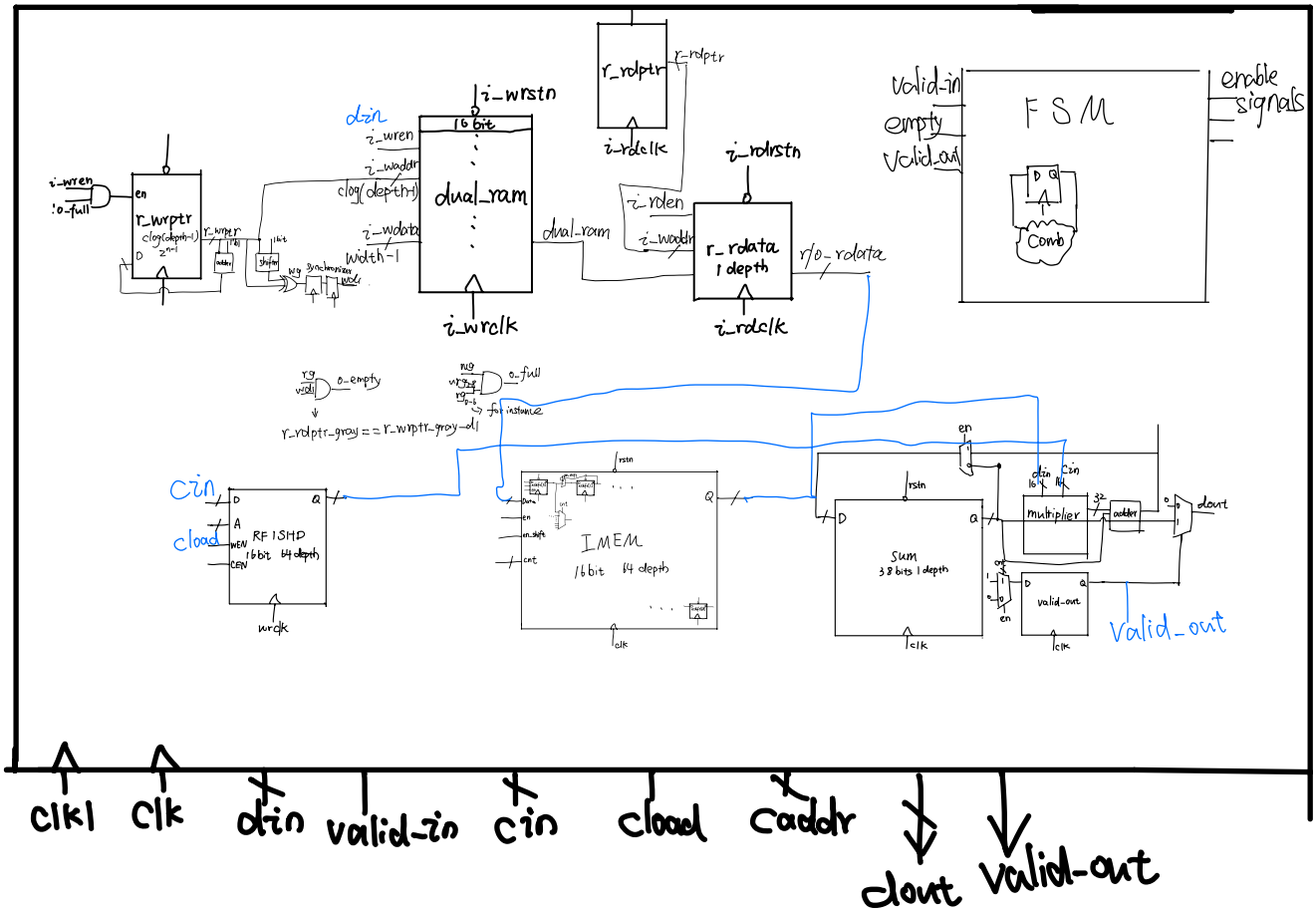
S0 : idle S1 : cload S2 : valid_in S3 : !empty S4 : empty

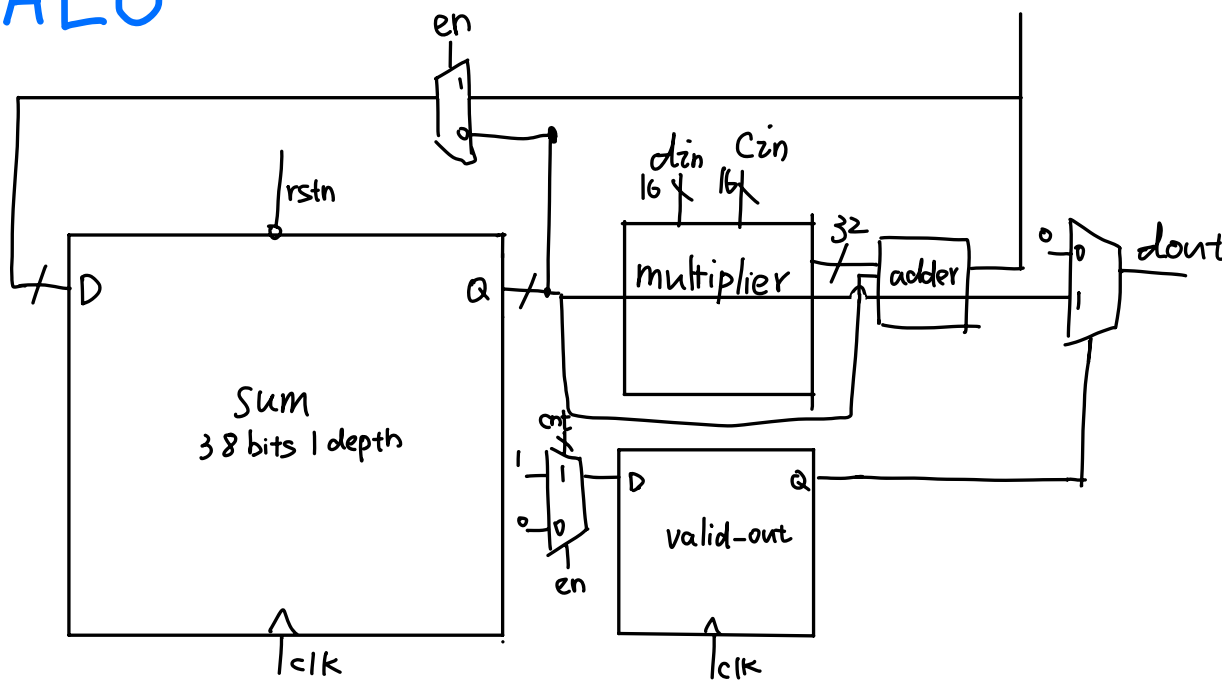
S5 : valid_out default : S0



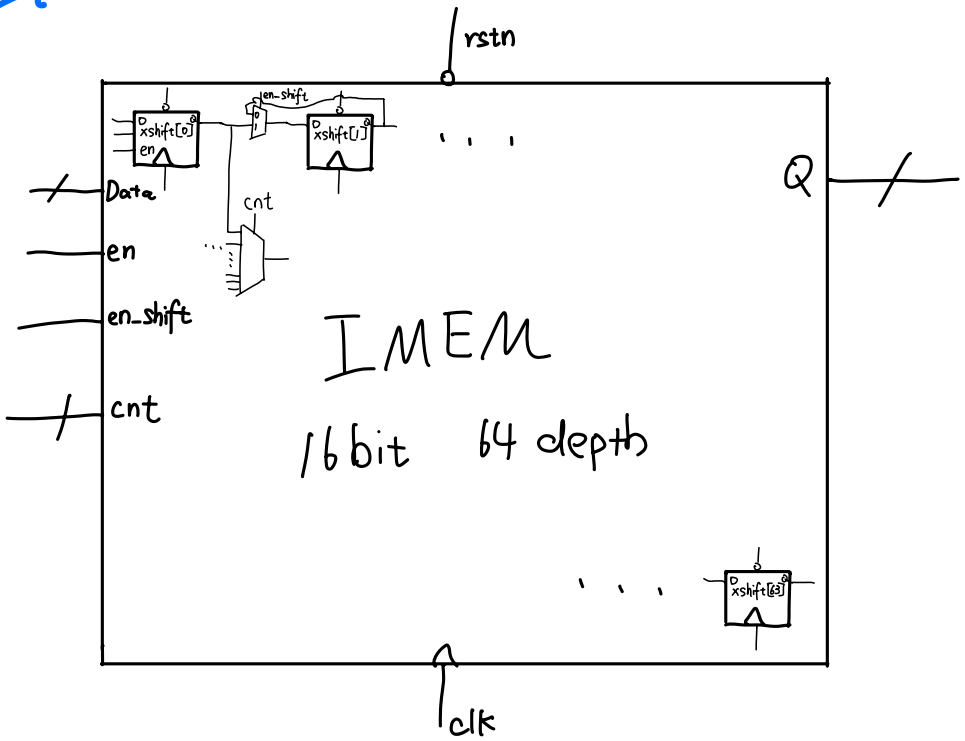


r_wrptr
clog(depth-1)
i_wren
o_full
en
r_wrptr
dual_ram
16 bit
i_wrstn
i_wren
i_waddr
clog(depth-1)
i_wdata
width-1
i_wrclk
dual_ram
r_rdptr
r_rdptr
i_rdclk
i_rdrstn
i_rden
i_waddr
r_rdata
1 depth
r/o_rdata
i_rdclk
valid_in
empty
valid_out
FSM
enable signals
Comb
o_empty
r_rdptr_gray == r_wrptr_gray_d1
o_full
for instance
cin
cload
RF 1SHD
16bit 64 depth
wrclk
IMEM
16bit 64 depth
clk
en
rstn
Sum
38 bits 1 depth
clk
multiplier
adder
dout
valid_out
clk
Valid_out
clk1
clk
din
valid-in
cin
cload
caddr
dout
valid-out

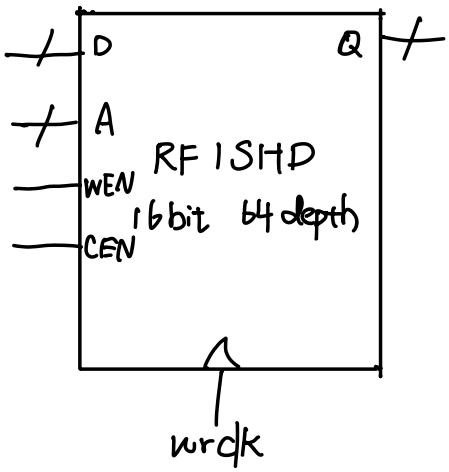
ALU


en
rstn
din
Cin
16
16
32
multiplier
adder
dout
D
Q
Sum
38 bits 1 depth
cnt
valid-out
en
clk
clk

IMEM

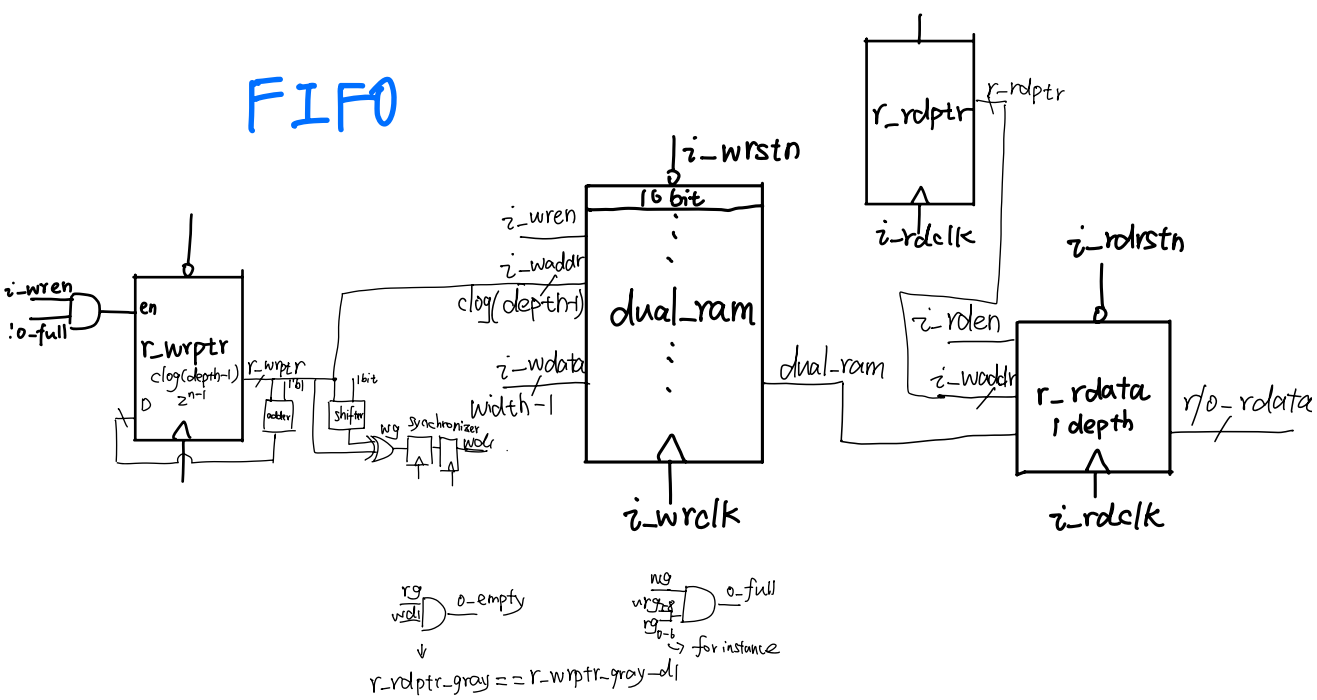

rstn
en_shift
xshift[0]
xshift[1]
xshift[63]
en
Data
cnt
Q
en
en_shift
cnt
IMEM
16bit 64 depth
clk

SRAM



D for data input

A for address

CEN	WEN	
0	0	write
0	1	read
1	~	

FIFO