Elektronik

Active Components

EITA10

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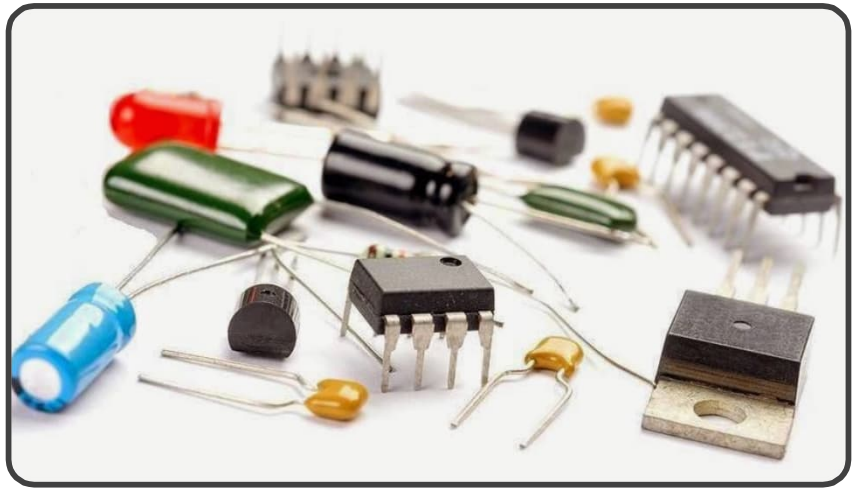
April 2025

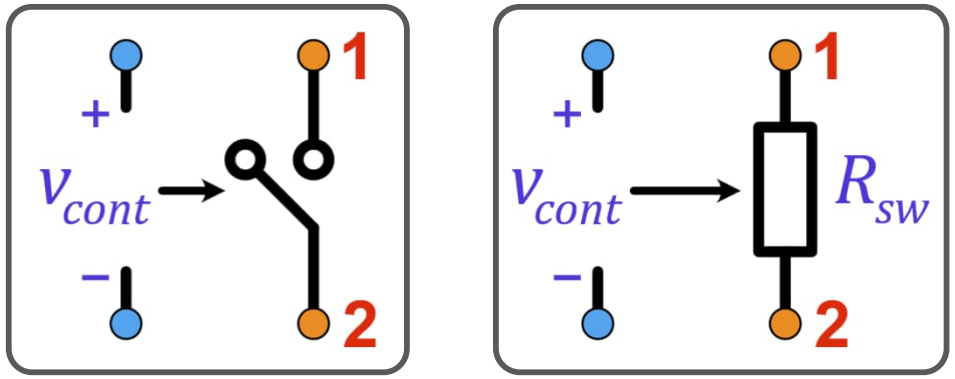
Active and Passive Components

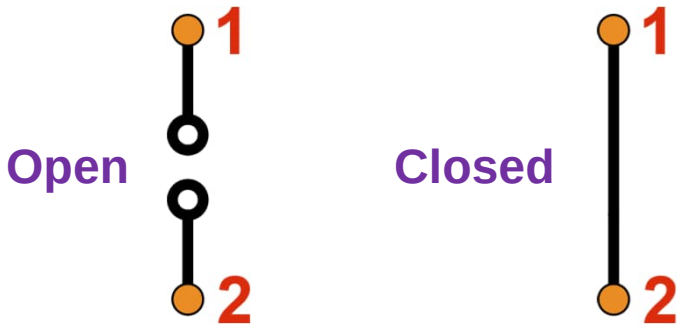
- **Passive components**
  - Resistors, capacitors, inductors, etc.
  - Do not need to be activated (always working)
  - Wide linear range
- **Active components**
  - Diodes, transistors, ICs, LEDs, etc.
  - Must be activated.
  - Multiple modes of operation
  - Control current flow and voltage distribution
  - Generally nonlinear



An Ideal Electronically-Controlled Switch

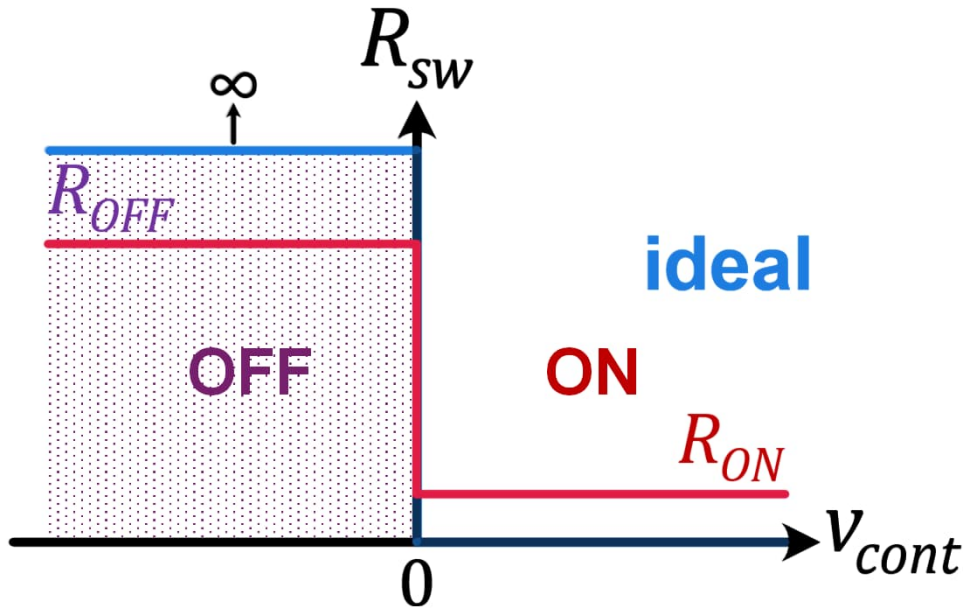
- A two-state device
- Having four terminals
- The **resistance** between 1 and 2 is controlled by the voltage applied to the Gate.
- **OFF state:**
  - $v_{cont} < 0 \Rightarrow R_{sw} \rightarrow \infty$
  - Open, perfect isolation between 1 and 2
- **ON state:**
  - $v_{cont} \geq 0 \Rightarrow R_{sw} = 0$
  - Closed, short-circuit between 1 and 2





Realistic Switch

- Finite OFF-resistance (R_{OFF})
- Imperfect ON-resistance (R_{ON})
  - Voltage drop
  - Power loss and noise generation
- **Threshold** voltage (V_t)



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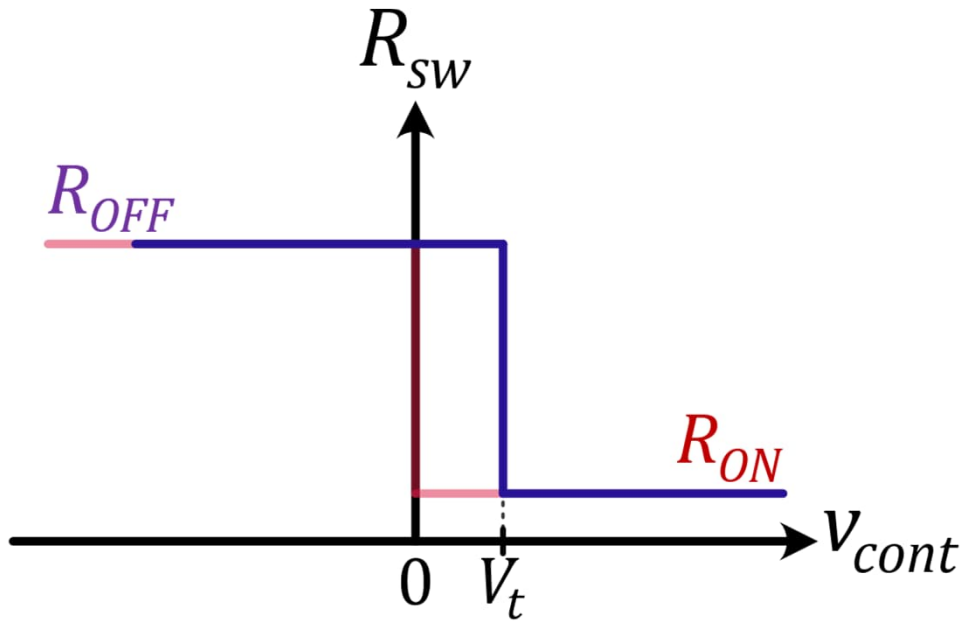

$$R_{sw} = \begin{cases} R_{OFF} & ; v_{cont} < V_t \\ R_{ON} & ; v_{cont} \geq V_t \end{cases}$$

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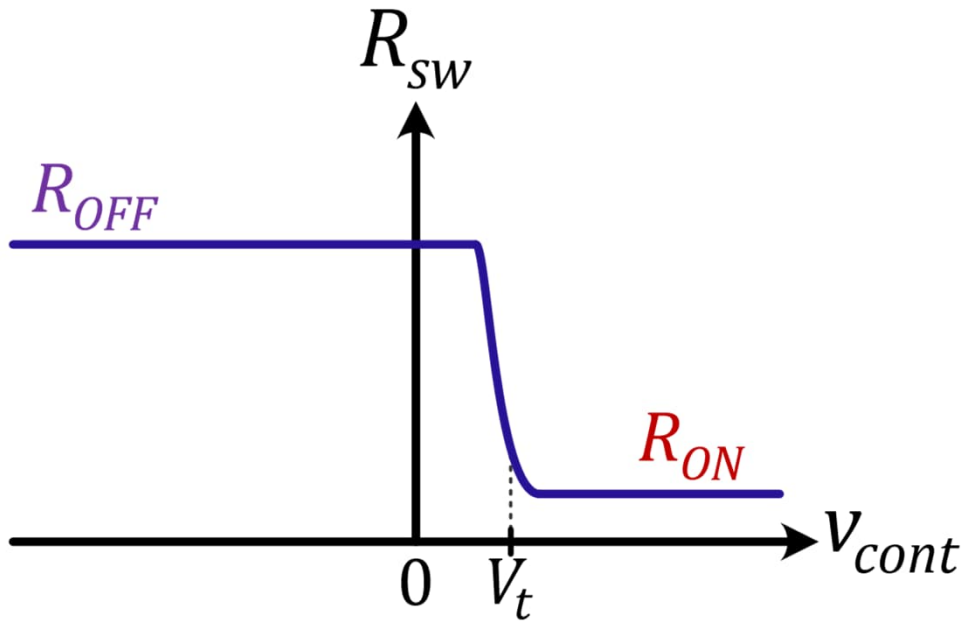

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  - Voltage drop
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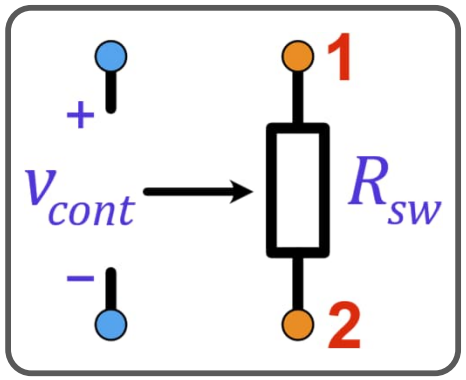
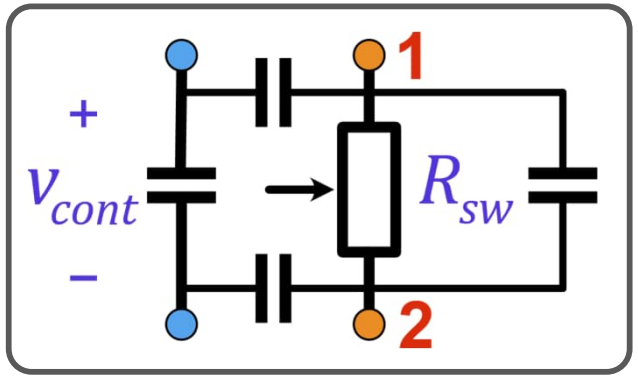
- **Threshold** voltage (V_t)
- **Gradual transition** from OFF to ON
- Parasitic capacitances
- Equivalent high-frequency RC-circuit
  - Delay ($\tau = RC$)
  - Limited sampling frequency (f_s)

Low-Frequency Model

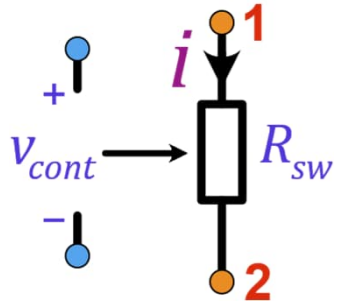


High-Frequency Model

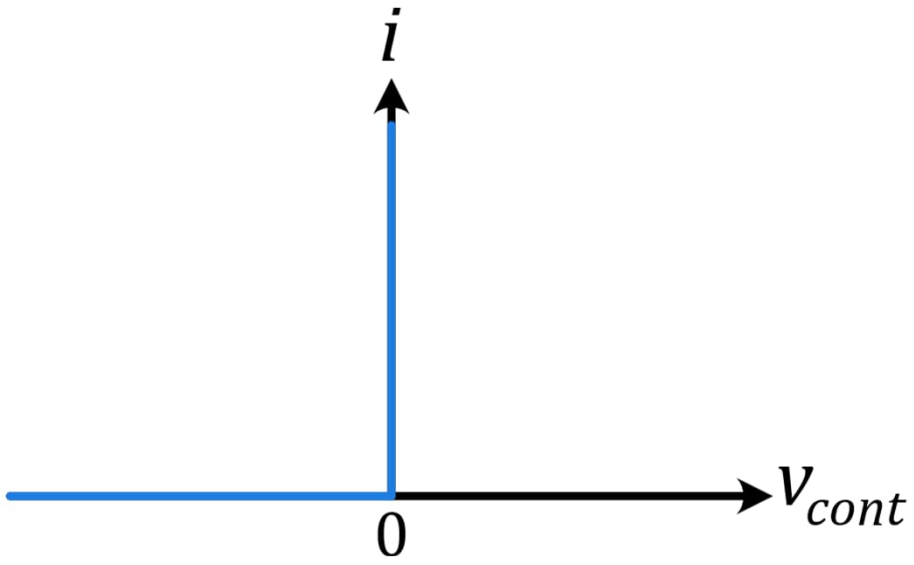


$i - v$ Characteristic of a Switch

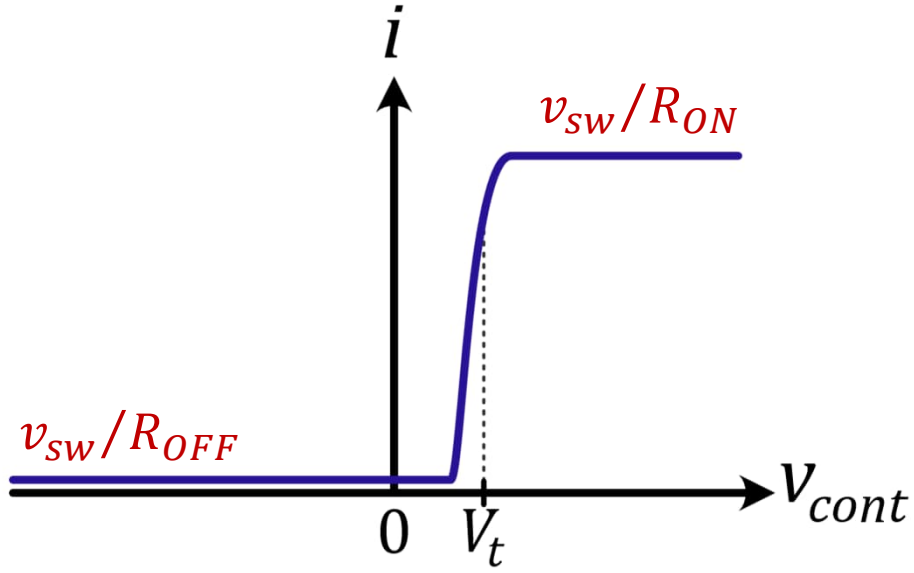
- For a constant $v_{sw} = v_1 - v_2$



$$i = \frac{v_{sw}}{R_{sw}}$$



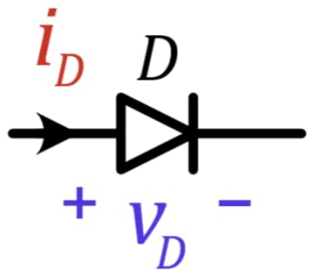
ideal

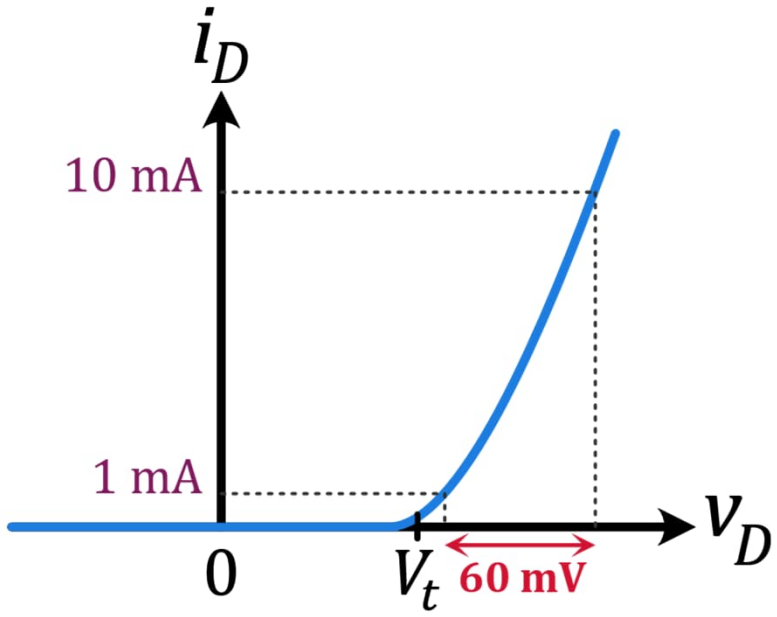


Practical

Diode, a Self-Controlled Switch

- The control voltage is the same as the voltage across the device ($v_{cont} = v_D$).
- **ON state**
  - $v_D \geq V_t \approx 0.7\ V$
  - v_D remains **almost constant**, no matter what current flows! (~60 mV per decade)
  - $R_{ON} \approx \frac{25\ mV}{I_D}$ (at room temperature)
- **OFF state**
  - $v_D < V_t$
  - $R_{OFF} \approx$ 100 to 1000 MΩ



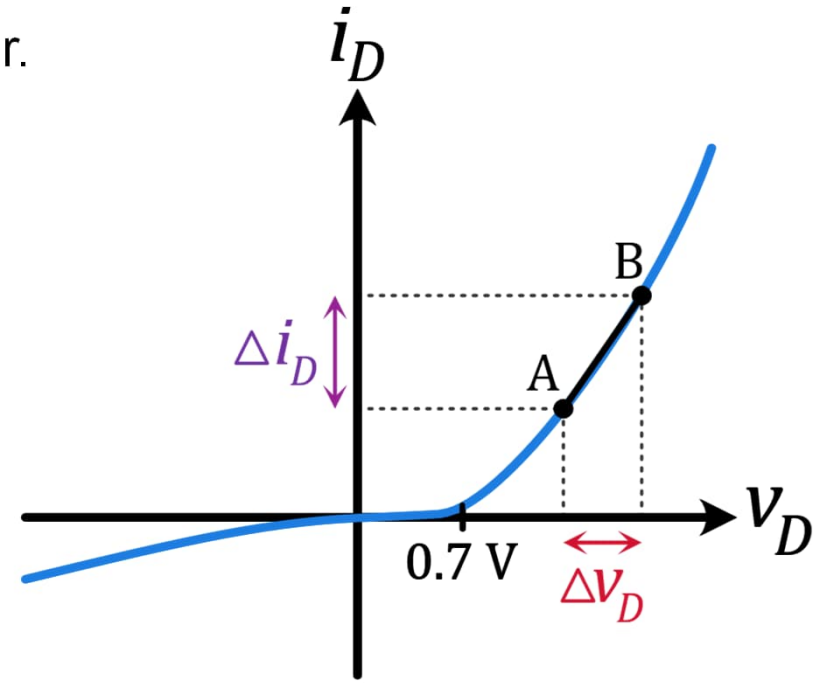


Pause and Ponder 1

A group of students have measured and plotted the $\boldsymbol{i - v}$ characteristic diagram of a diode. Can you help them calculate the values of $\boldsymbol{R_{ON}}$ and $\boldsymbol{R_{OFF}}$?

- By definition, $R_D = \frac{v_D}{i_D}$; however, diode is nonlinear.
- Linearization in a region of operation:

$$R_D = \frac{\Delta v_D}{\Delta i_D}$$



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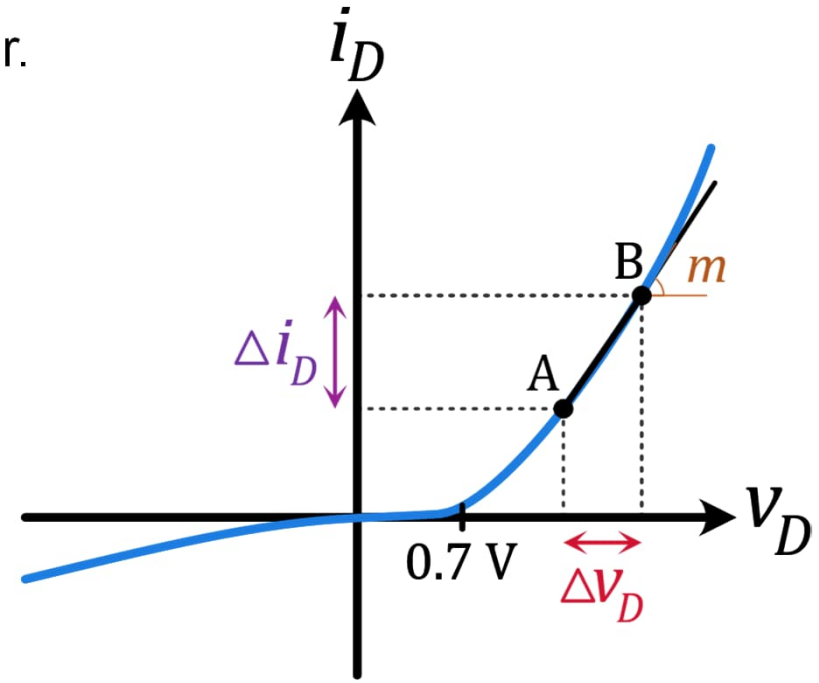
- Linearization in a region of operation:

$$R_D = \frac{\Delta v_D}{\Delta i_D}$$

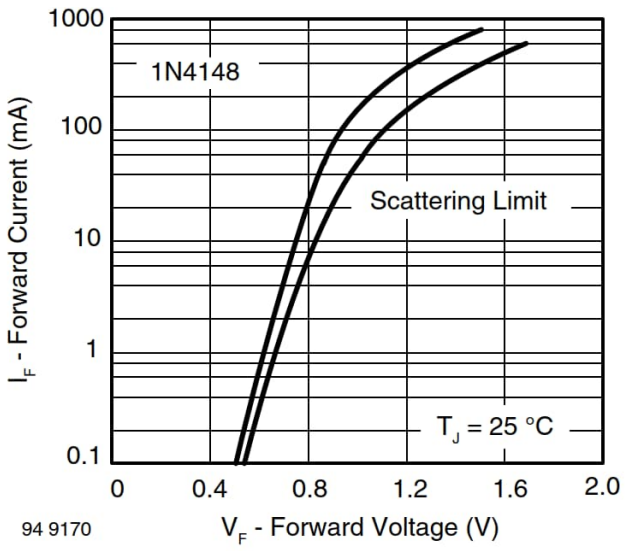
- Linearization at a certain point:

$$R_D = \left(\frac{di_D}{dv_D}\right)^{-1}$$

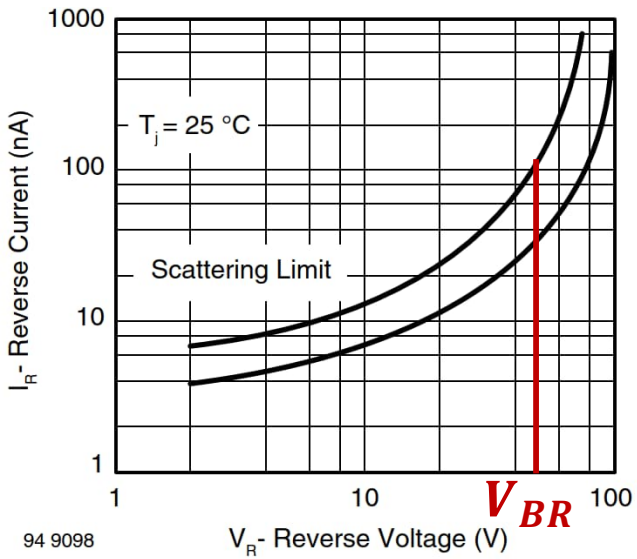


1N4148, a Commercial Diode

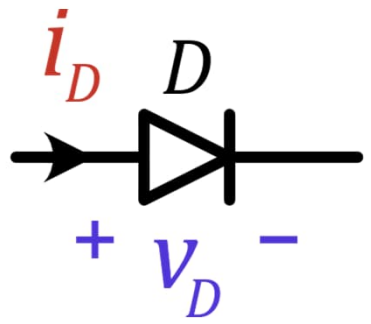
ON State $v_D \geq V_t$
(Forward Bias)



OFF State $v_D \geq V_t$
(Reverse Bias)



Anode **Cathode**



- Logarithmic scale to highlight **subthreshold** ($0 < v_D < V_t$) current

- Breakdown voltage (V_{BR}) = 75 V
- Sharp increase in reverse current

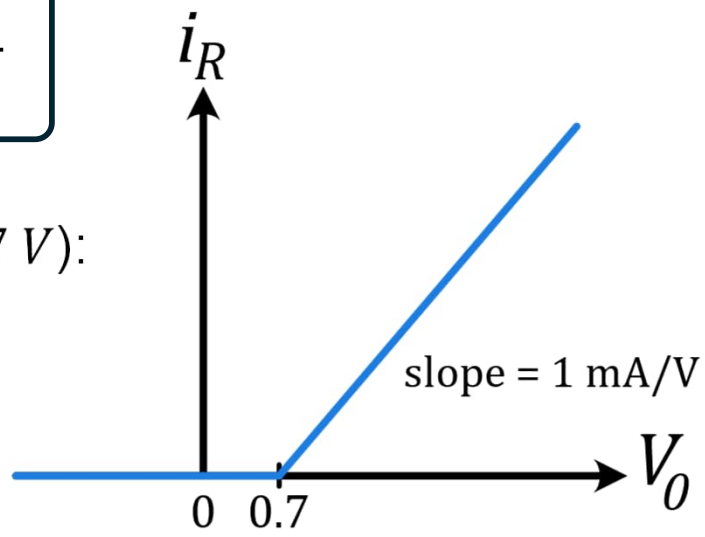
Diode Circuits – Example 1

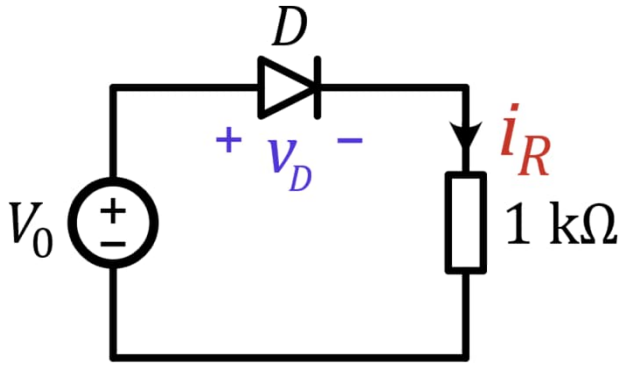
- Complete the table below. ($V_t = 0.7\ V, V_{BR} = 75\ V$)
- When diode conducts ($v_D \geq 0.7\ V$):

$$i_R = \frac{V_0 - v_D}{R} \approx \frac{V_0 - 0.7}{1000}$$

- When diode is OFF ($v_D < 0.7\ V$):

$$i_R = i_D = 0$$

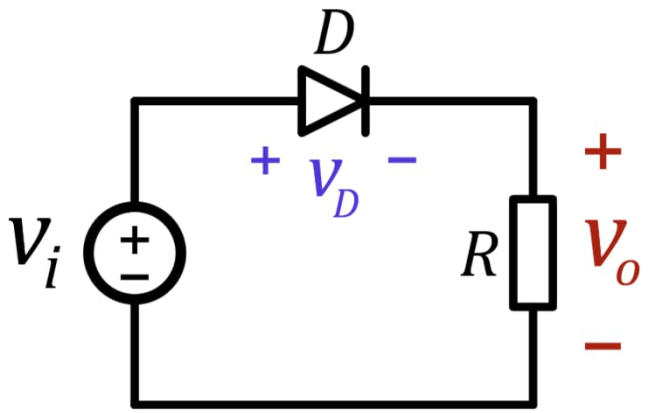


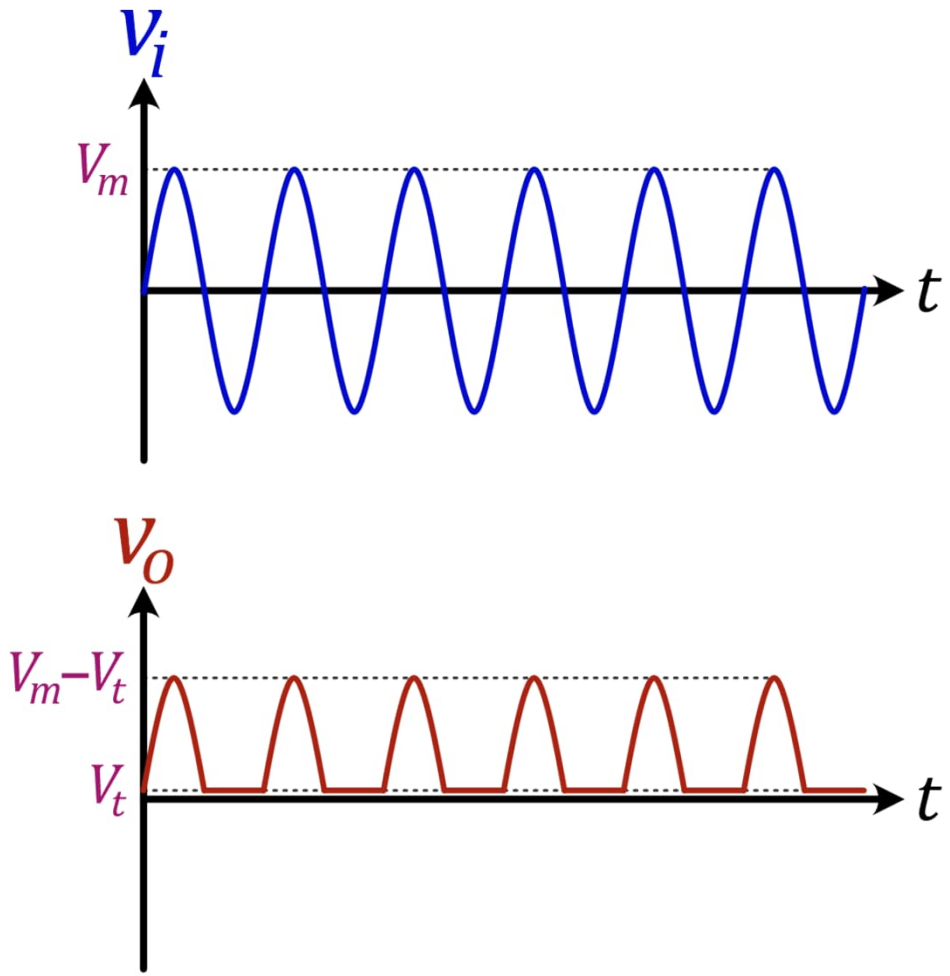


$V_0(V)$	$i_R(\mathrm{mA})$
10	9.3
5	4.3
2	1.3
0.7	0
0	0
-5	0

Diode Circuits – Example 3 (Rectifier)

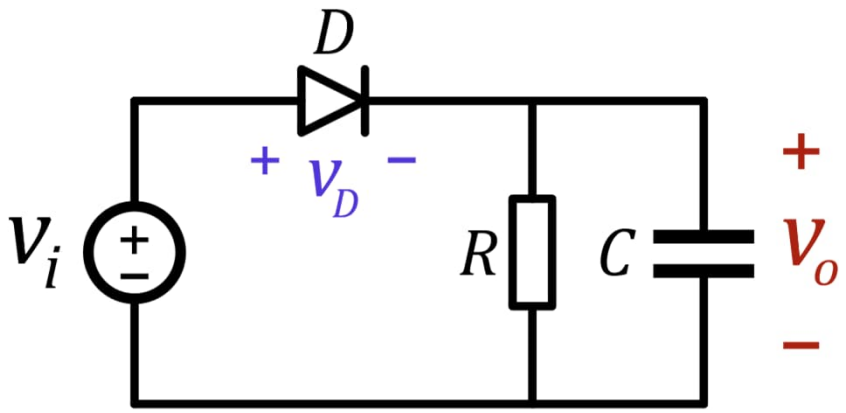
- Draw the output voltage when feeding in a sinusoidal voltage ($V_m \gg V_t$).

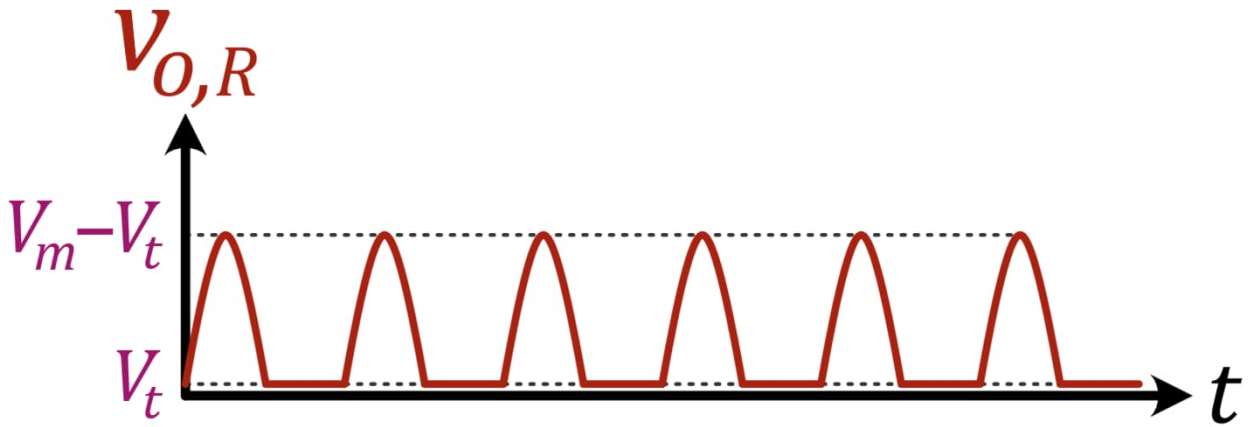




Diode Circuits – Example 2 (Filtered Rectifier)

- Draw the output voltage when feeding in a sinusoidal voltage ($V_m \gg V_t$).





- Diode is ON if: $v_i - v_o \geq V_t$
- In the beginning: $v_o(0) = 0$ V

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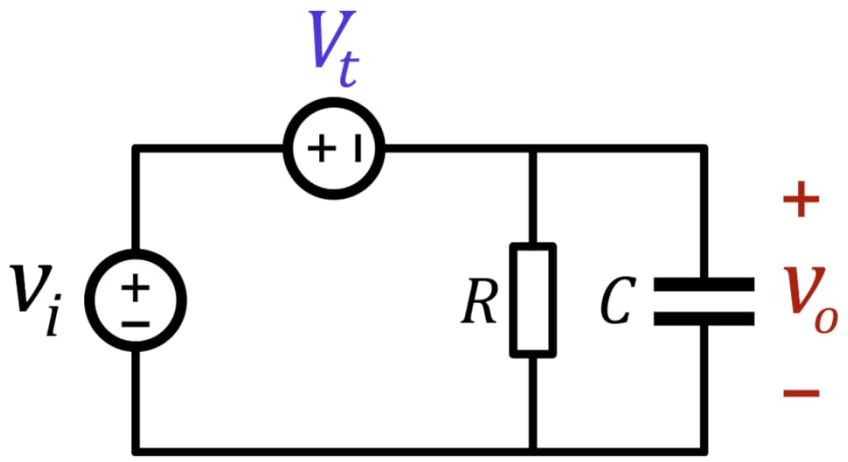

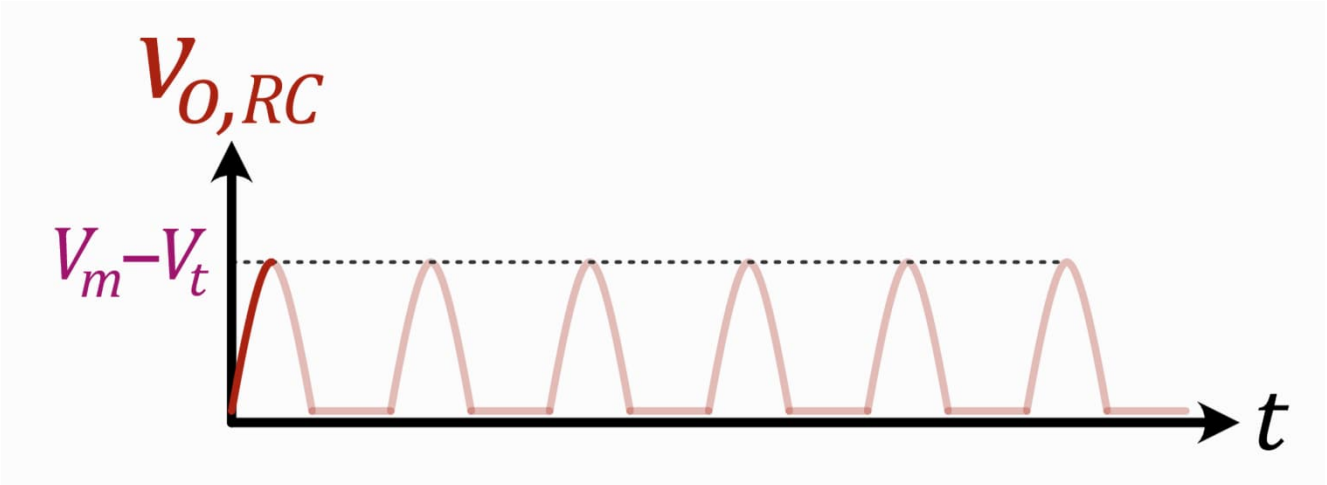

- Diode is ON if: $v_i - v_o \geq V_t$
- In the beginning: $v_o(0) = 0$ V
- The capacitor is charged up to $V_m - V_t$
- v_o follows v_i

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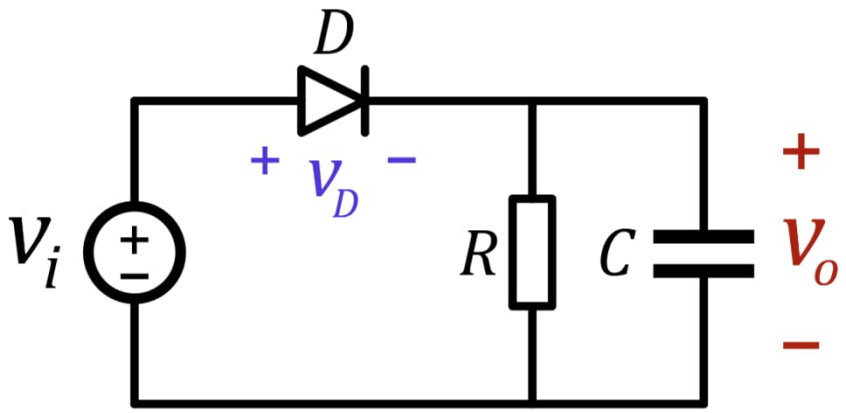

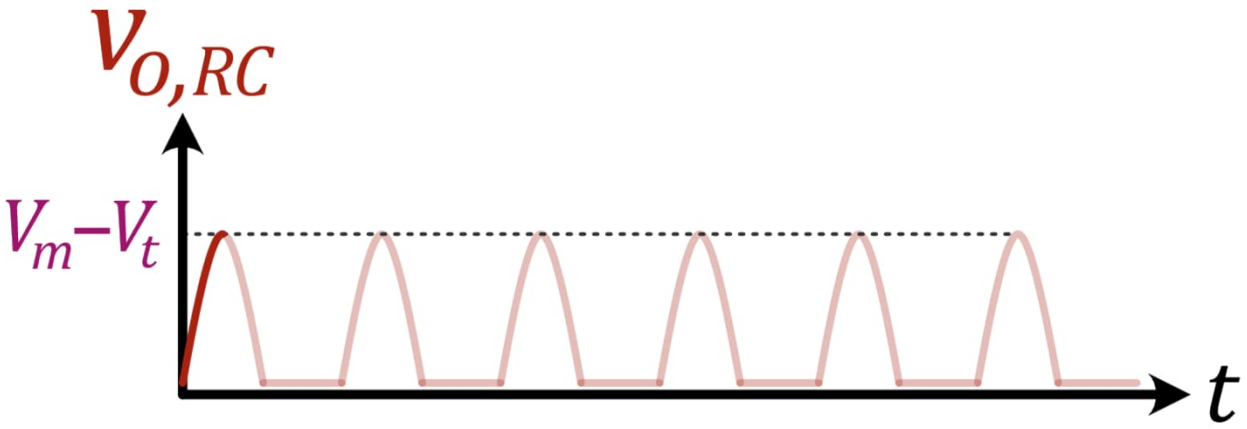

- Then v_i goes down
- $v_i < v_o$ → Diode is turned off

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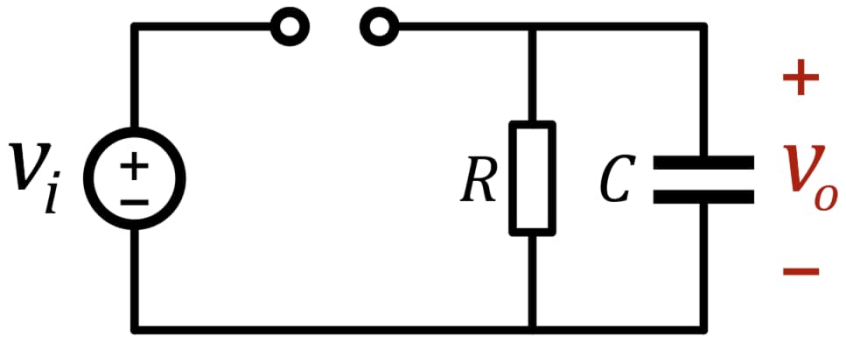
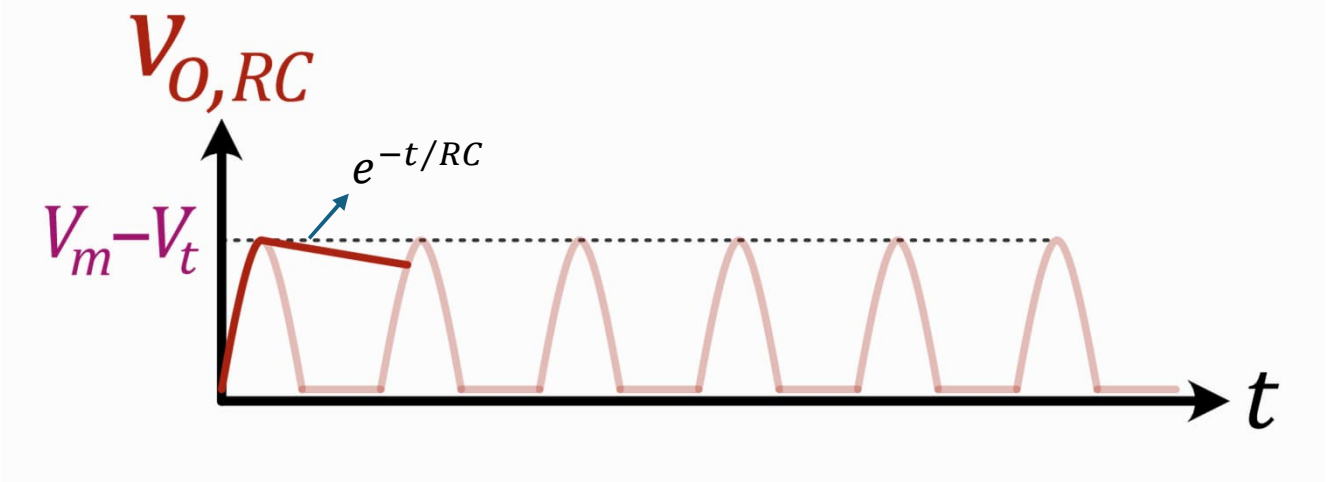
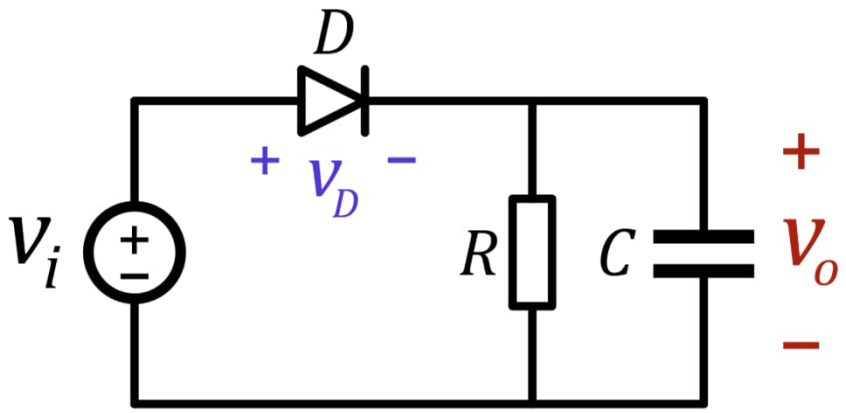


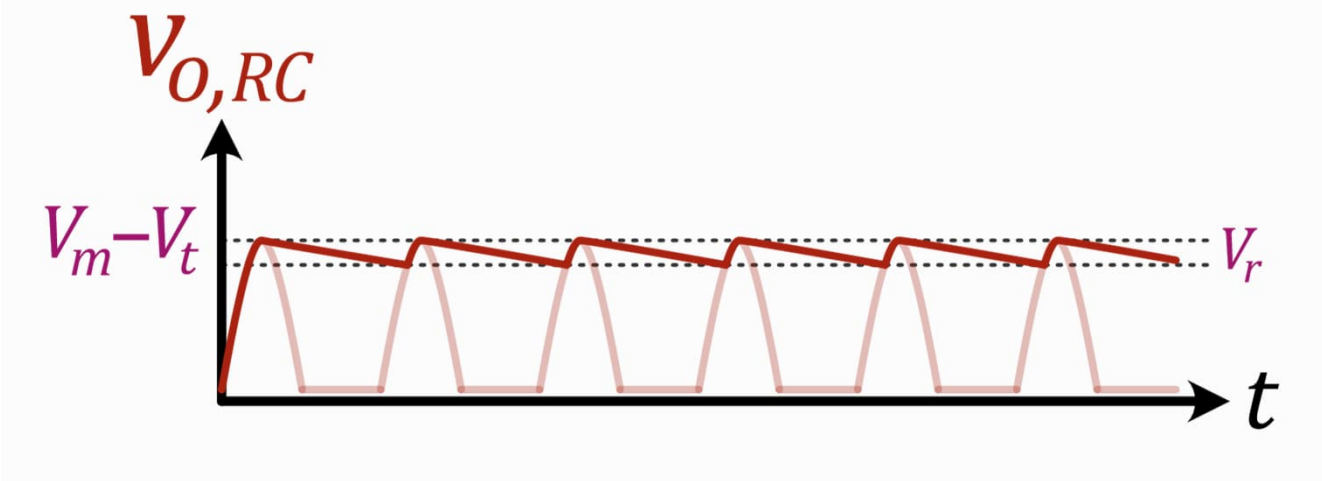


- Then v_i goes down
- $v_i < v_o$ → Diode is turned off
- The capacitor is partially discharged by R
- v_o drops with a large time constant

Diode Circuits – Example 2 (Filtered Rectifier)

- Draw the output voltage when feeding in a sinusoidal voltage ($V_m \gg V_t$).





- Afterwards, the capacitor is charged and discharged repeatedly.
- A simple **AC-to-DC converter**
- Output ripple (V_r) is inversely proportional to the filter's capacitance (C).

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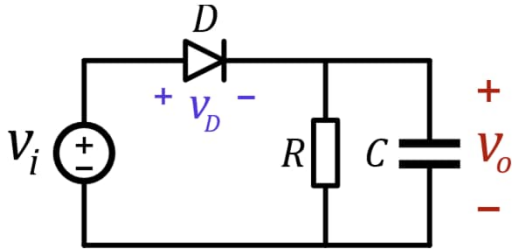

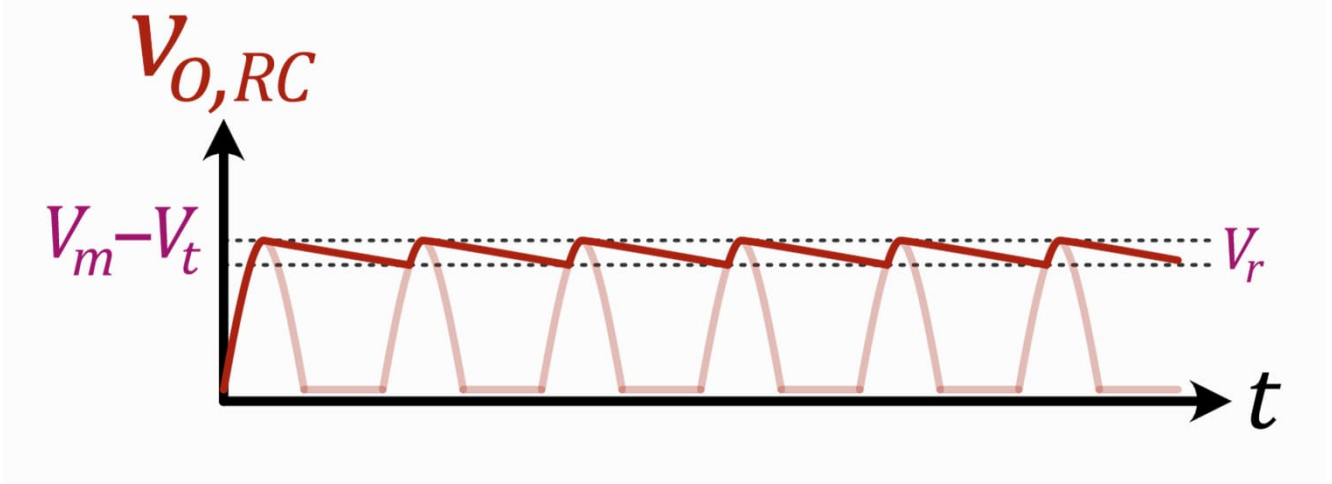

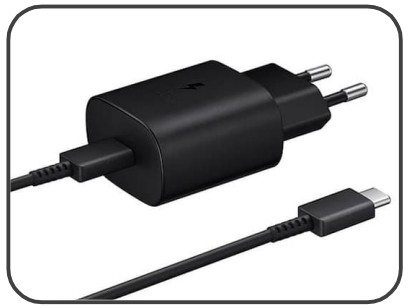

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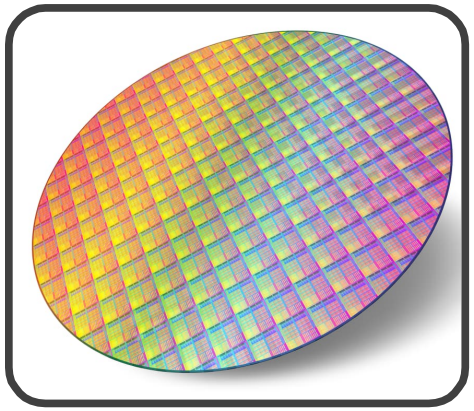
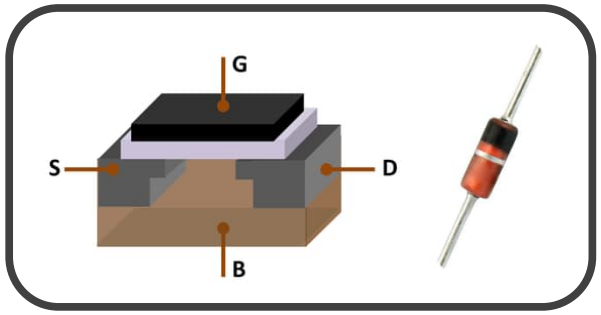
How is a Diode Fabricated?

Silicon

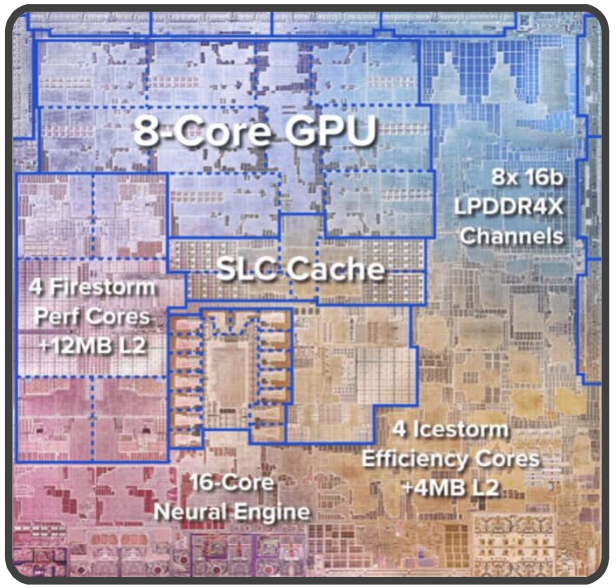
Germanium

Silicon Wafer





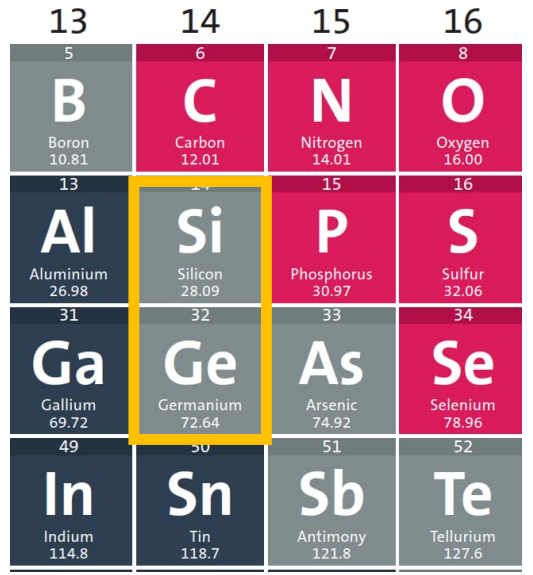
Apple M1 CPU

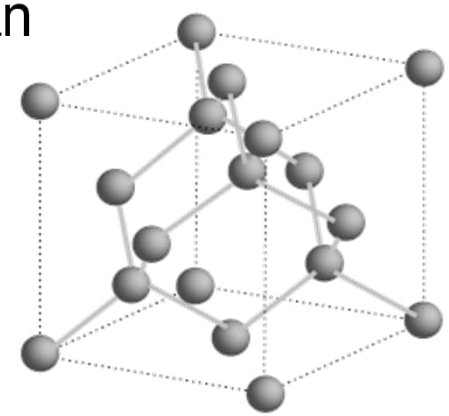


5 nm CMOS

Raw Material: Silicon

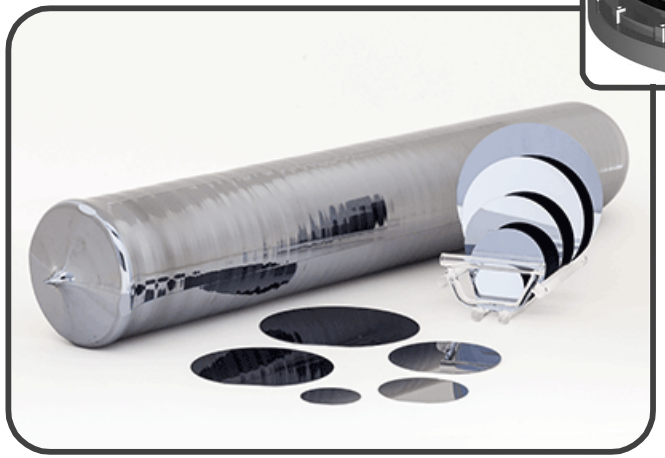
- Active devices, including diodes, are made of **semiconductors**.
- Mostly Silicon (Si) and Germanium (Ge)
- Diamond cubic crystal structure
- $\sim 5 \times 10^{22} \mathrm{atom/cm^3}$
- At temperature higher than 0 °K, electrons can jump from valence energy band to the conduction band.
- Therefore, the material shows lower resistance.





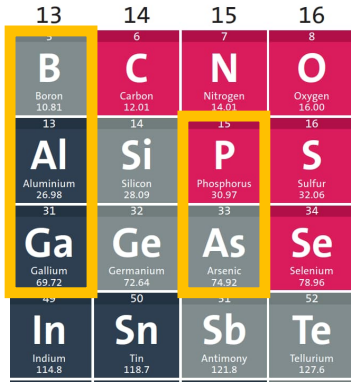
Electronic-Grade Silicon

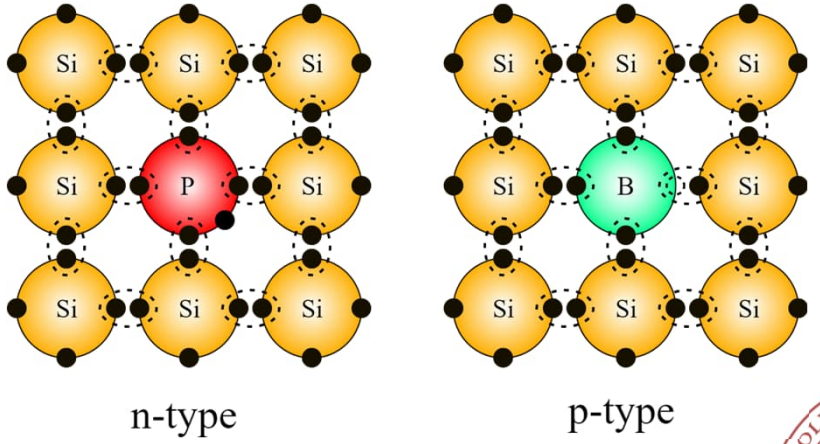
- Mechanical refinement to 98% (metallurgical grade)
- Thermo-chemical purification to **> 99.9999%**
- Controlled concentrations of impurities and dopants
- Si ingot is sliced into **wafers**
  - Diameter ~ 30 cm
  - Thickness ~ 200 to 300 µm
- Precise surface finish and dimensions



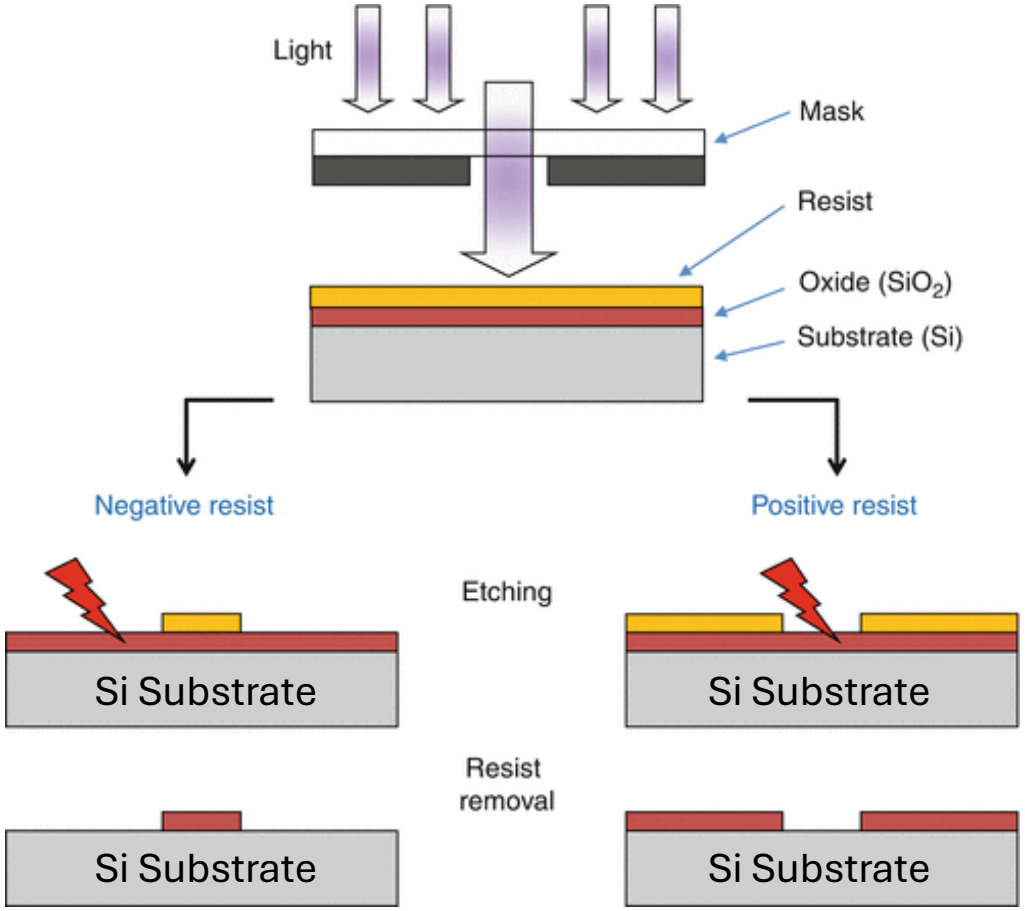
Doping and Selective Patterning

- **Dopants** (atoms from Group 13 or 15) are introduced into the silicon lattice.
- Adjust the resistivity of Si
- **Dopped Si:**
  - **N-type:** additional electrons, by implanting P or As
  - **P-type:** electron deficit, by implanting B, Al, or Ga
- **Photolithography:** selective patterning of the wafer's surface to be implanted by N/P dopants.

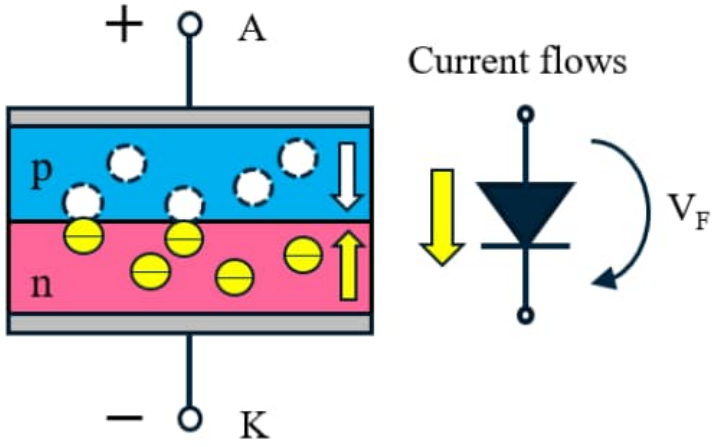


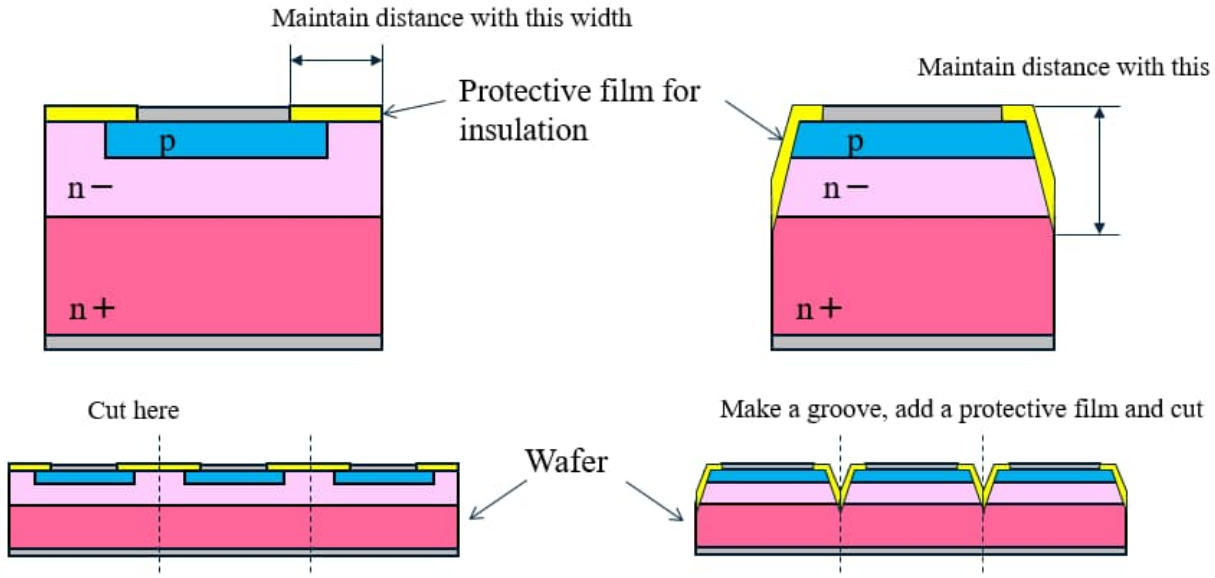


Photolithography

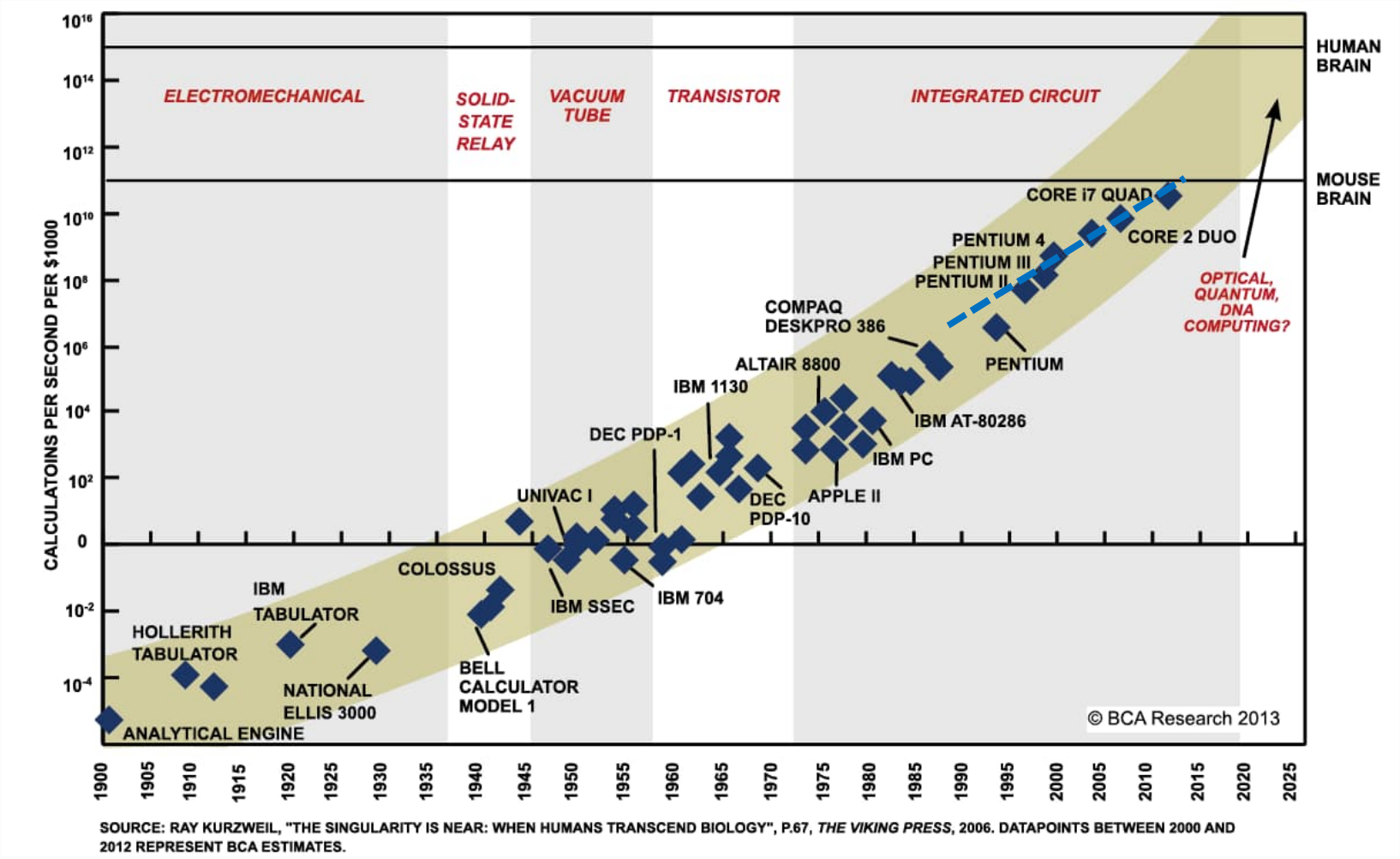


A diode: P-N Junction



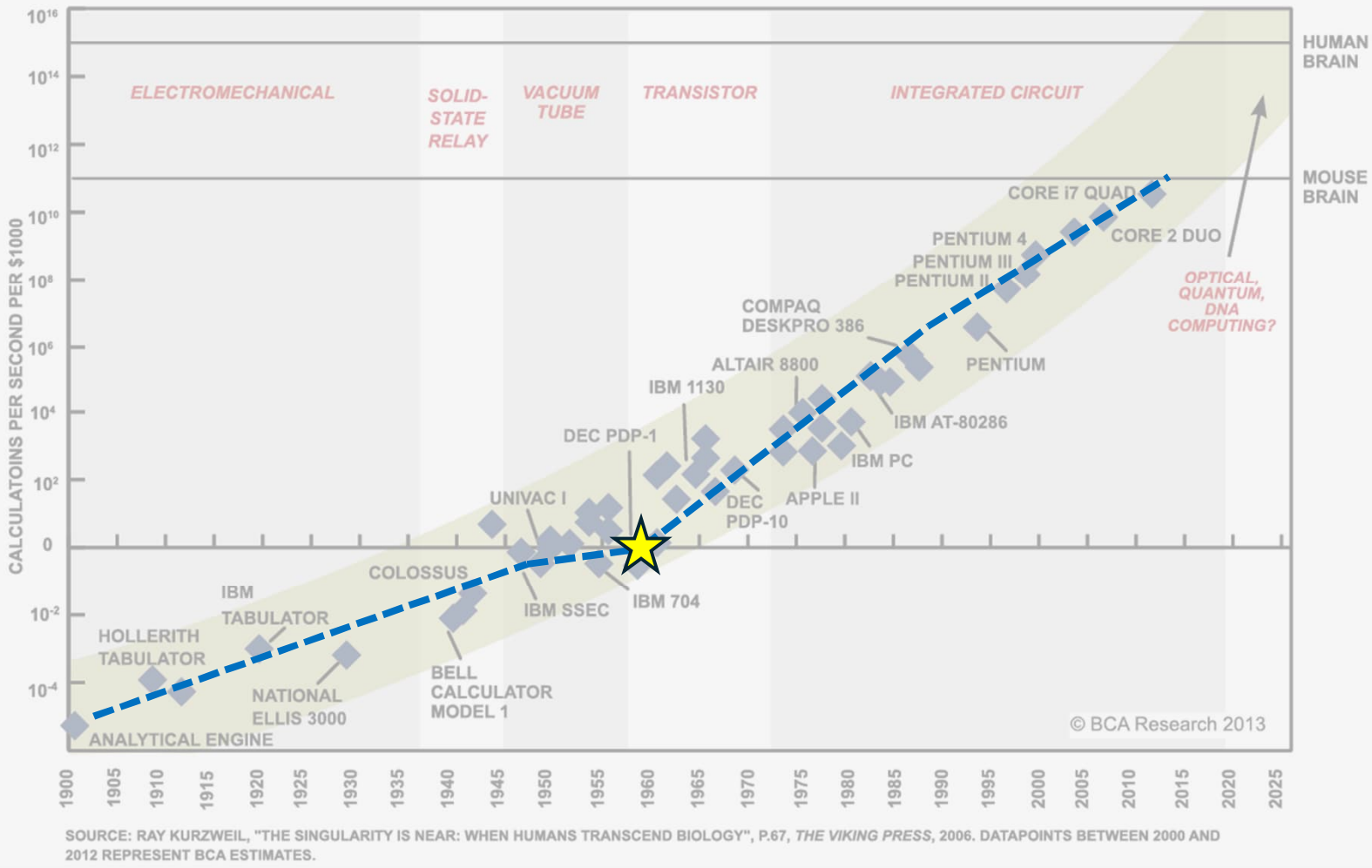


Magic of Electronic Miniaturization



SOURCE: RAY KURZWEIL, "THE SINGULARITY IS NEAR: WHEN HUMANS TRANSCEND BIOLOGY", P.67, *THE VIKING PRESS*, 2006. DATAPOINTS BETWEEN 2000 AND 2012 REPRESENT BCA ESTIMATES.

Magic of Electronic Miniaturization



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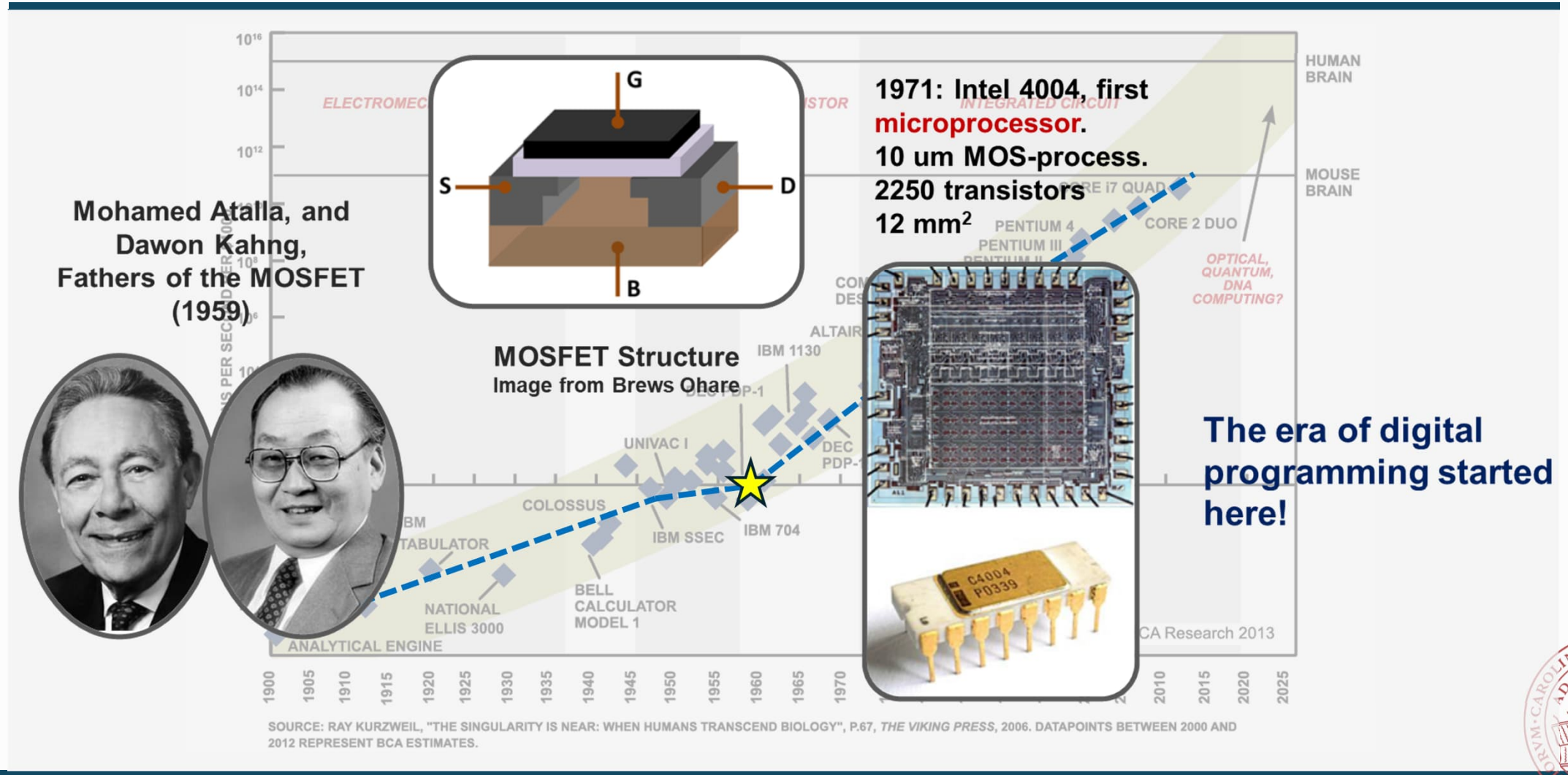
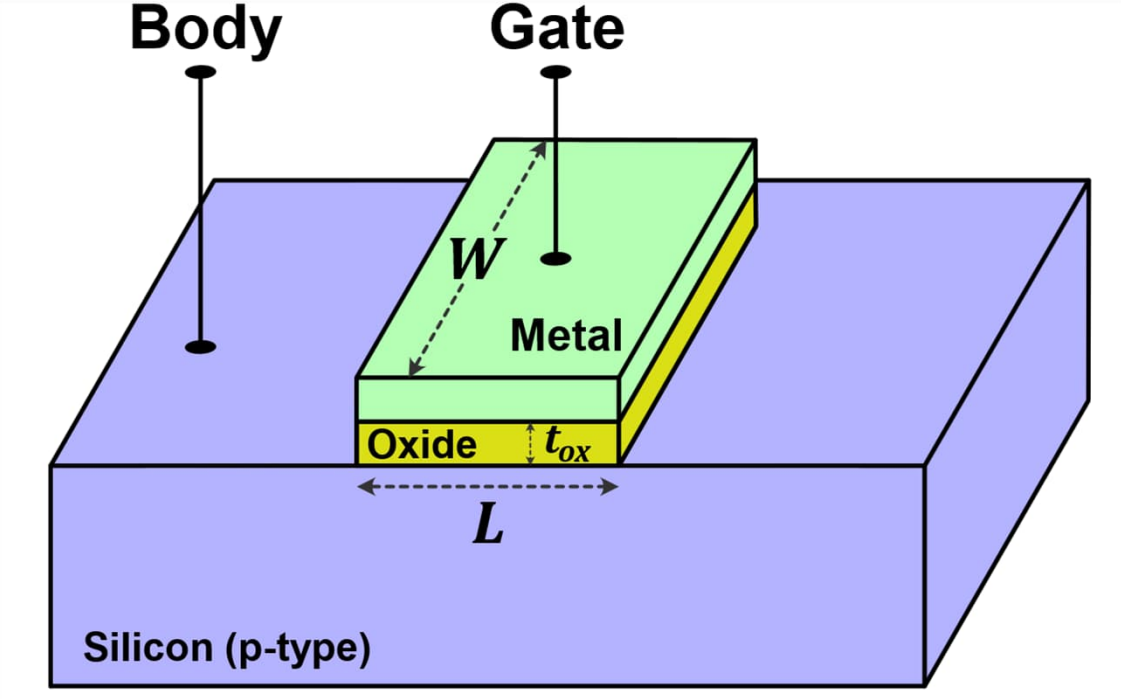
Magic of Electronic Miniaturization



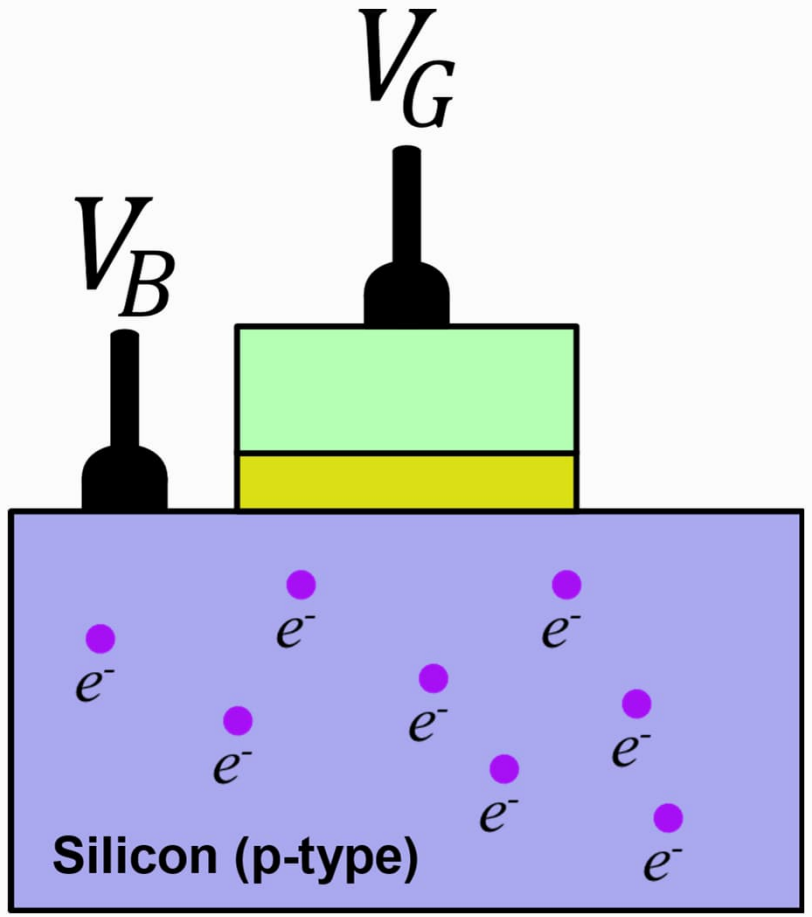
Metal-Oxide-Semiconductor (MOS) Structure

- A structure similar to a capacitor (MOSCAP)
- **Metal:** conductor, polysilicon
- **Oxide:** very thin layer (2~5 nm)
- **Silicon:** a thick layer (2~3 μm)
  - For NMOS: P-type body
  - For PMOS: N-type body



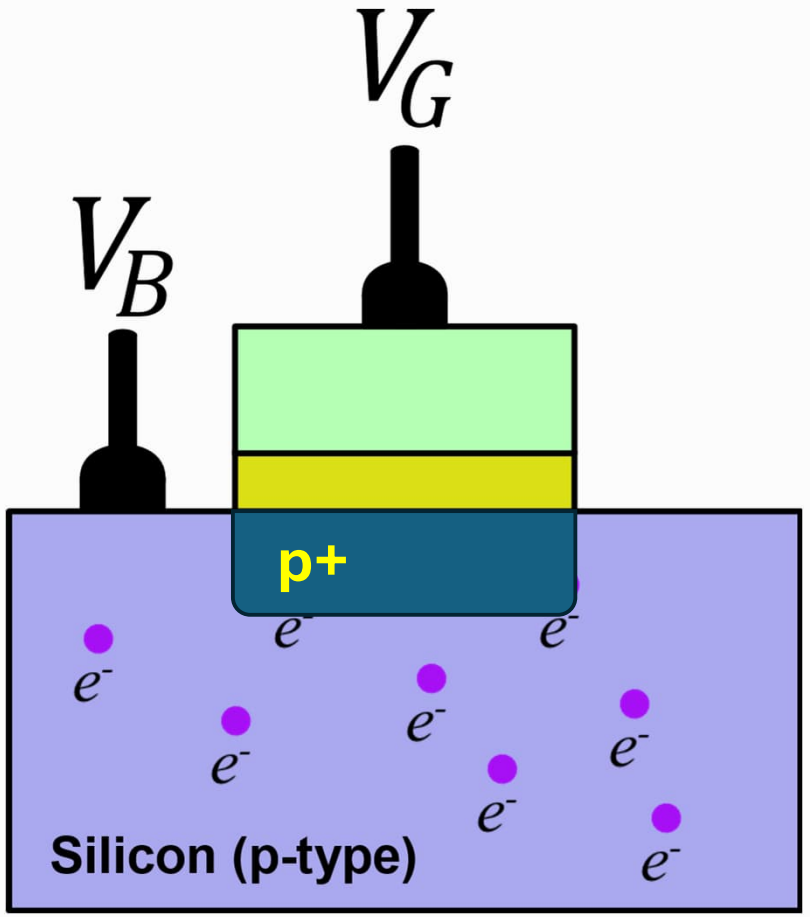
Metal-Oxide-Semiconductor (MOS) Structure

- Two terminals: **Gate** and **Body**
- Body is normally connected to GND ($V_B = 0$)
- Gate voltage (V_G) controls the **local concentration of electrons** underneath the oxide-silicon interface.



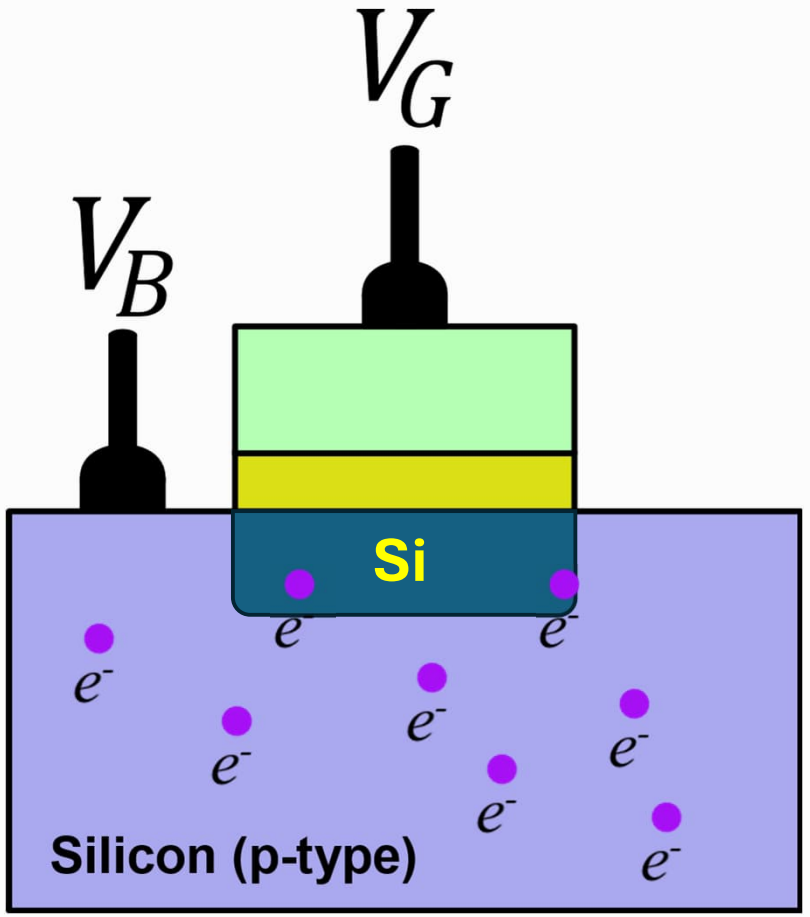
Accumulation

- $V_B = 0$
- $V_G < 0$
- More deficit of electrons underneath the gate oxide
- Silicon become more p-type (p+)



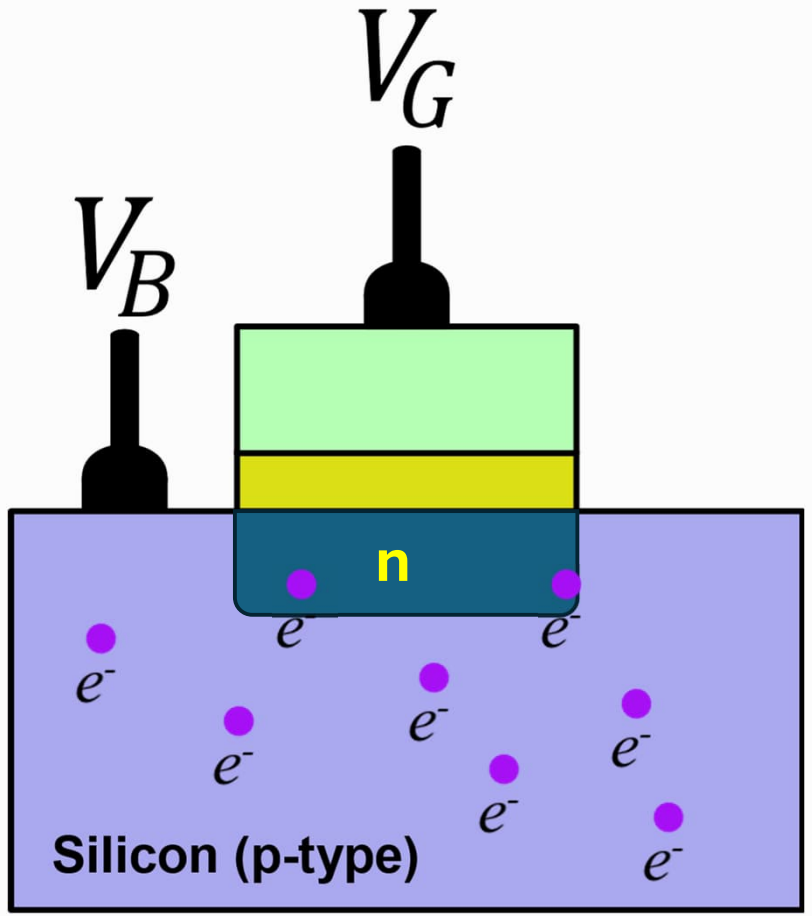
Depletion

- $V_B = 0$
- $0 < V_G < V_t$
- Less deficit of electrons underneath the gate oxide
- Not enough to make it N-type
- Behaves like undopped silicon



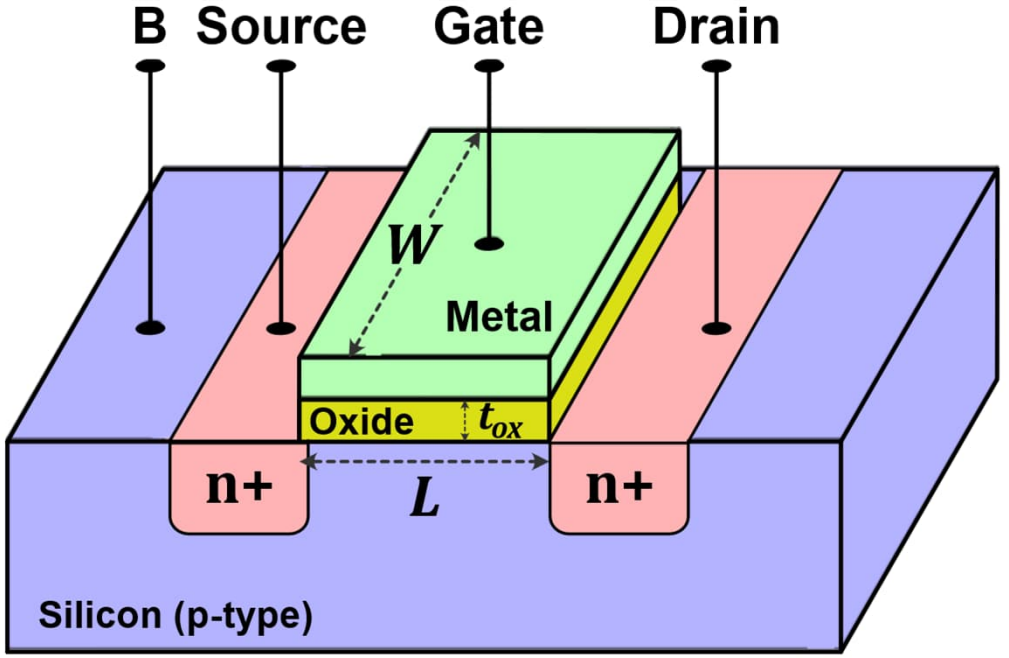
Inversion

- $V_B = 0$
- $V_t < V_G$
- **Excess** electrons underneath the gate oxide
- Locally N-type Si, a thin layer within the body (channel)



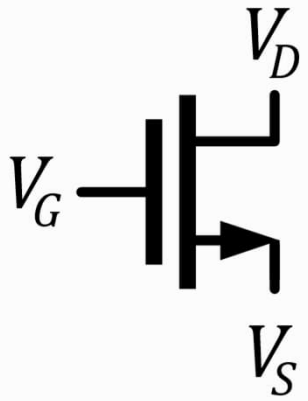
MOS Field-Effect Transistor (MOSFET)

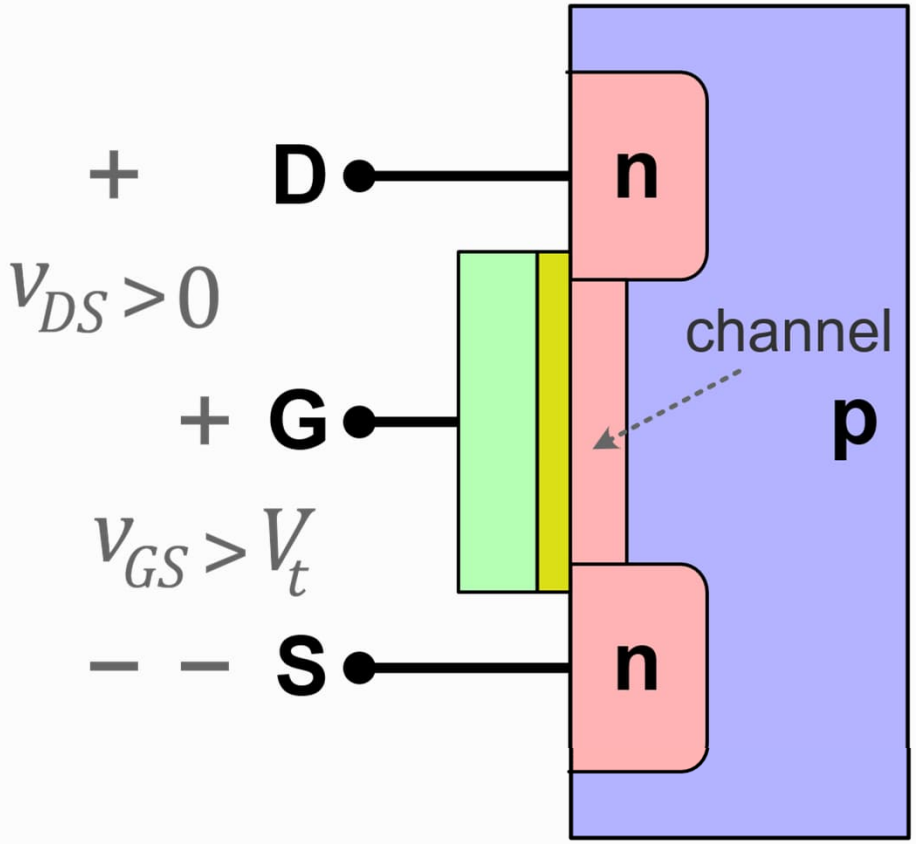
- We created a voltage-controlled material
- The resistivity of the channel is controlled by V_G → variable resistance (R_{ds})
- By implanting two n-type regions on the sides of the channel (with some overlap with the gate), a switch is constructed.
- **Source (S)** and **Drain (D)** terminals.



MOS Field-Effect Transistor (MOSFET)

- When $v_{GS} > V_t$ channel is formed next to the source.
- When $v_{DS} > 0$, electrons can flow from S to D through the channel.
- Schematic symbol of NMOS

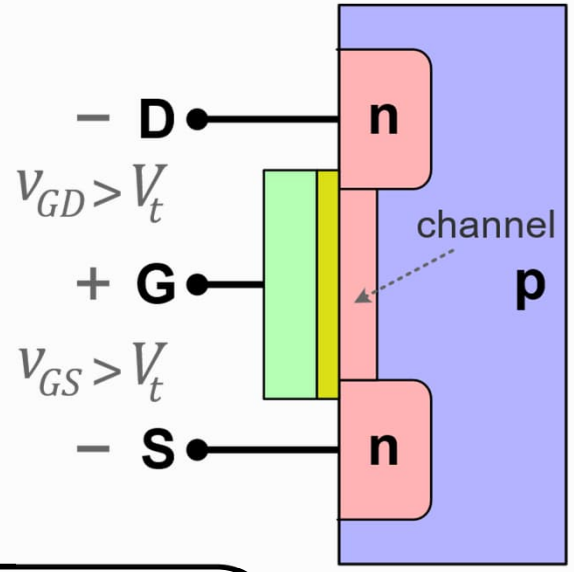


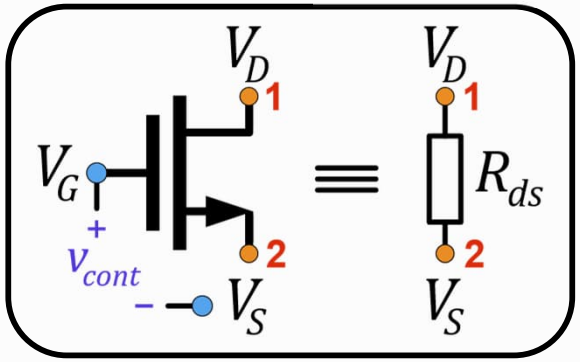


MOSFET as a Switch (Deep-Triode Region)

- $v_{GS} > V_t$ → Channel formation
- $v_{DS} \approx 0$ → Uniform channel
- Switch's performance depends on:
  - Material properties: $K_n \triangleq \frac{1}{2}\left(\frac{W}{L}\right)\mu_n C_{ox}$
  - Electron mobility: μ_n
  - Gate-oxide capacitance per area: $C_{ox} \triangleq \frac{\varepsilon_{ox}}{t_{ox}}$
  - Overdrive voltage: $v_{ov} \triangleq v_{GS} - V_t$

$$R_{ds} = \frac{1}{2K_n v_{ov}}$$

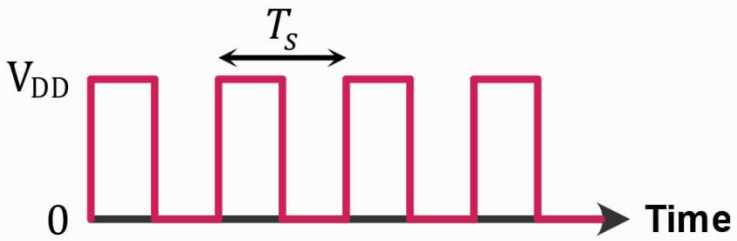


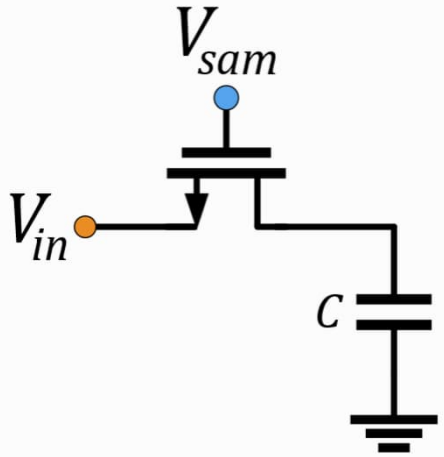


Pause and Ponder 1

- Derive an expression for the maximum achievable sampling frequency in an N-bit ADC.

$$\begin{cases} R_{ds} = \dfrac{1}{2K_n v_{ov}} \\ \tau = R_{ds}C \\ f_{s,max} = \dfrac{1}{2N(\ln 2)\tau} \end{cases} \Rightarrow \boxed{f_{s,max} = \frac{K_n v_{ov}}{N(\ln 2)C}}$$



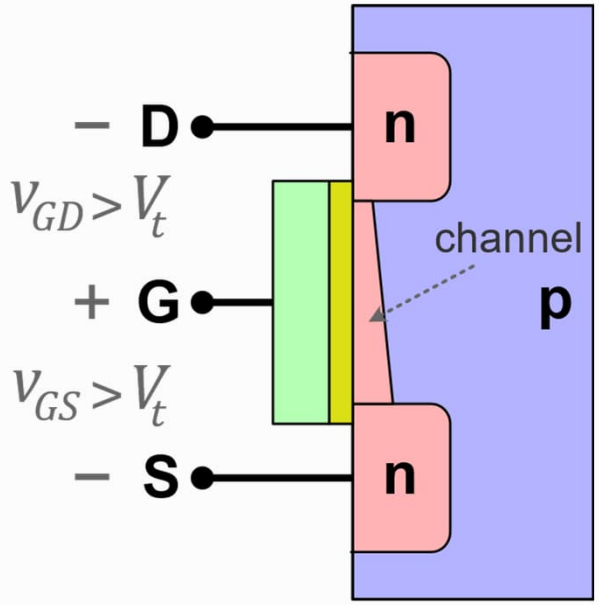


- By halving the channel length (L), how does the maximum sampling frequency increase?

$$f_{s,max} = \frac{\mu_n}{N(\ln 2)} \cdot \frac{C_{ox}}{C} \cdot \frac{W}{L} v_{ov} \Rightarrow$$ It is doubled. Really?!

Linear (Triode) Region of Operation

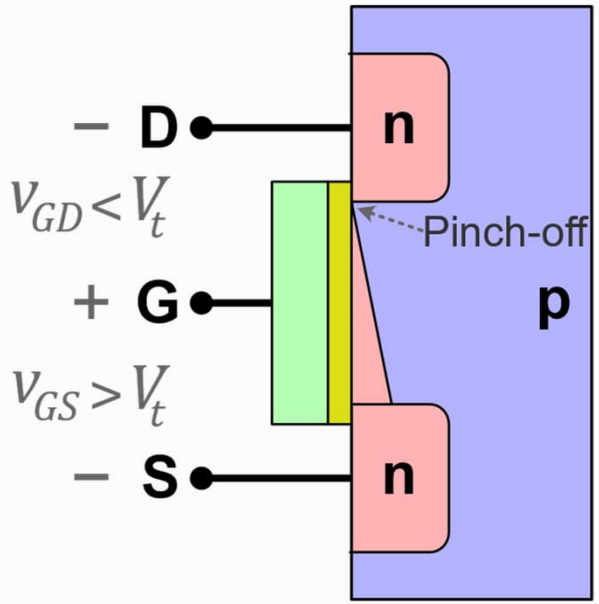
- $v_{GS} > V_t$ → Channel formation
- $0 < v_{DS} < (v_{GS} - V_t)$ → Non-uniform channel
- The transistor is symmetrical
  - No physical difference between S and D
- Increasing v_{DS} → Lowering $v_{GD} = v_{GB\ (at\ D)}$
- Lower Inversion at D → Higher channel resistance → Lower current



$$i_D = K_n(2v_{ov}v_{DS} - v_{DS}^2)$$

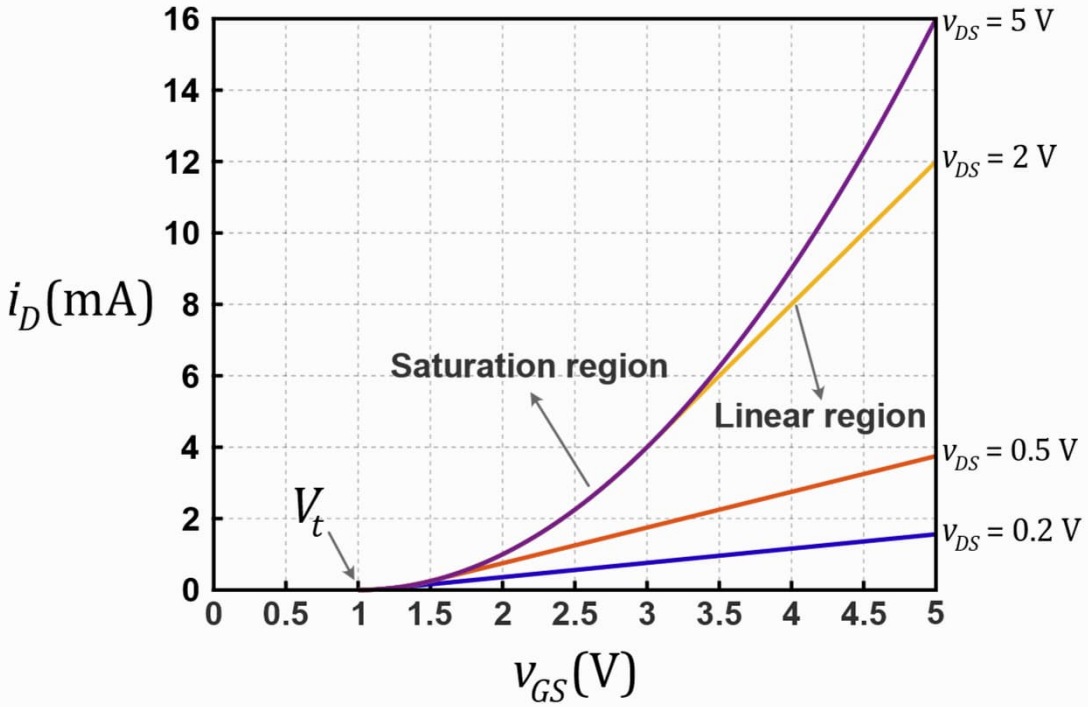
Saturation Region

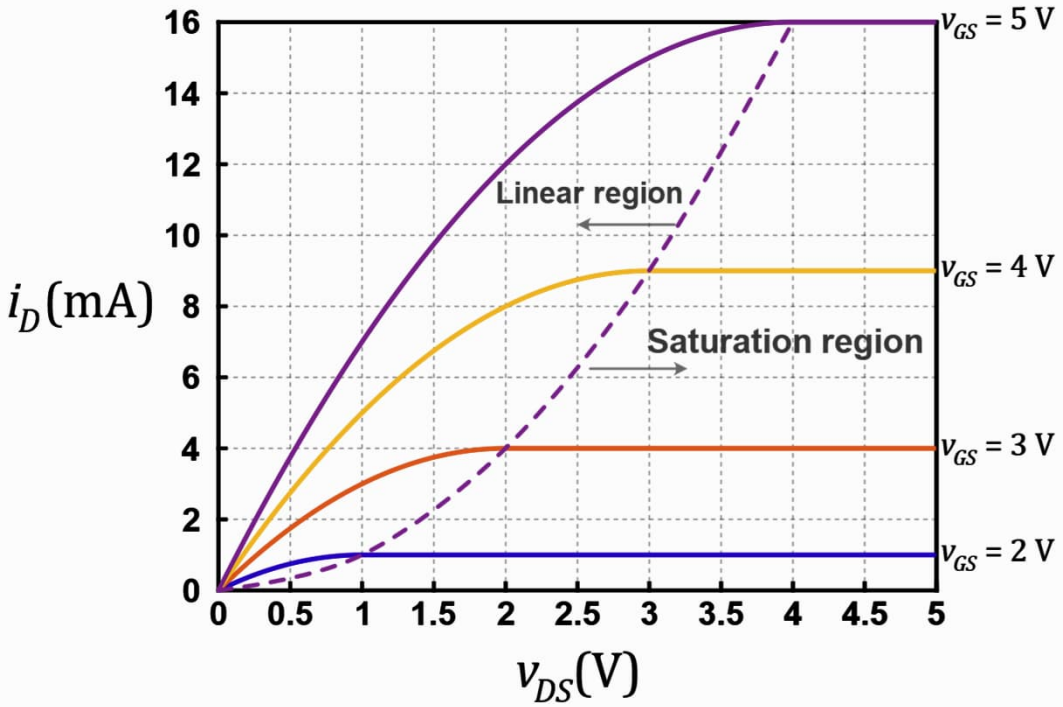
- $v_{GS} > V_t$ → Channel formation
- $(v_{GS} - V_t) < v_{DS}$ → Pinched-off channel
- The channel width is reduced to zero at D
- Increasing v_{DS} → Ideally, no effect on i_D anymore!
- Suitable operating region for analog amplification



$$i_D = K_n v_{ov}^2$$

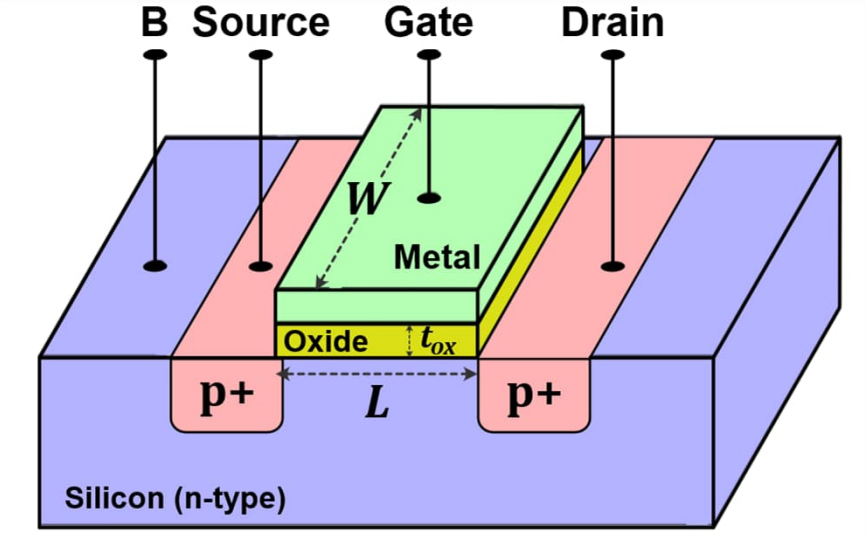
$i - v$ Characteristics of an NMOS Transistor

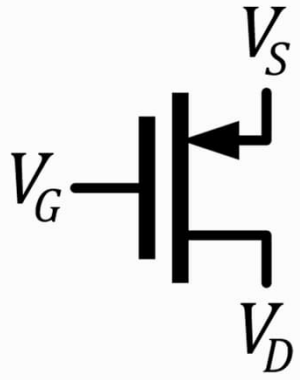




PMOS: MOS in N-Type Substrate

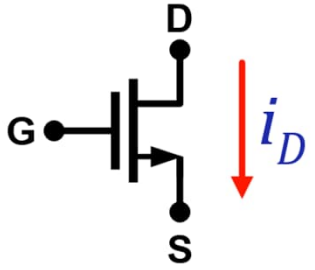
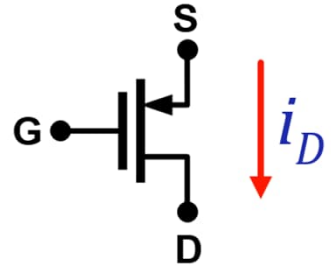
- When $v_{GS} < V_t < 0$, a low-resistance p-type channel is formed.
- A negative v_{DS} create a current (i_D) flowing from S to D.
- The same equations describe i_D as a function of v_{GS} and v_{DS}.





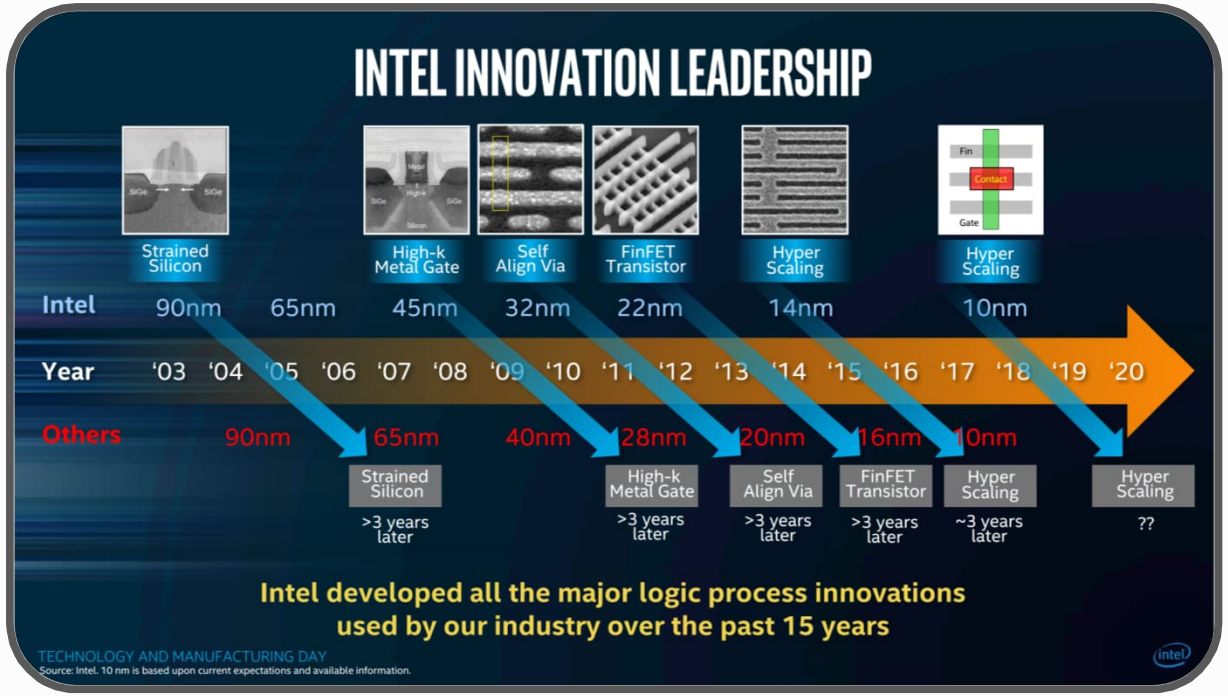
Complementary MOS (CMOS) Technology

- Both NMOS and PMOS devices are integrated on the same chip.
- NMOS switch is activated by logical 1 ($0 < V_t < v_{GS}$).
- PMOS switch is activated by logical 0 ($v_{GS} < V_t < 0$).

	NMOS	PMOS
Kretssymbol		
$\mu \approx$	$675\,\mathrm{cm^2V^{-1}s^{-1}}$	$240\,\mathrm{cm^2V^{-1}s^{-1}}$
$\kappa \approx$	$115\,\mu\mathrm{AV^{-2}}$	$40\,\mu\mathrm{AV^{-2}}$
$V_t \approx$	$+0.5\,\mathrm{V}$	$-0.6\,\mathrm{V}$
Subtröskel (strypt område)	$v_{GS} \leq V_t$, $v_{DS} \geq 0$, $i_D = 0$	$v_{GS} \geq V_t$, $v_{DS} \leq 0$, $i_D = 0$
Linjärt område	$v_{GS} \geq V_t$, $0 \leq v_{DS} \leq v_{GS} - V_t$, $i_D = K(2(v_{GS} - V_t)v_{DS} - v_{DS}^2)$	$v_{GS} \leq V_t$, $0 \geq v_{DS} \geq v_{GS} - V_t$, $i_D = K(2(v_{GS} - V_t)v_{DS} - v_{DS}^2)$
Mättnads-område	$v_{GS} \geq V_t$, $v_{DS} \geq v_{GS} - V_t$, $i_D = K(v_{GS} - V_t)^2$	$v_{GS} \leq V_t$, $v_{DS} \leq v_{GS} - V_t$, $i_D = K(v_{GS} - V_t)^2$
v_{DS}, v_{GS}	Vanligtvis positiva	Vanligtvis negativa

CMOS Process Nodes

- **Feature size:** Represents the minimum gate length (L_{min}) achievable in a given CMOS technology generation.
- **Process Node:** Identified by the feature size
- Steady **miniaturization** over decades
- Approaching quantum physics (atomic-scale) limits



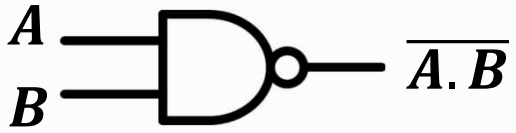
Digital Logic Operators and Gates

- Boolean logic condition: True and False
- In binary digital systems:
  - Logical “1” = True, corresponds to high voltage level (close enough to the supply voltage, V_{DD})
  - Logical “0” = False, corresponds to low voltage level (close enough to the GND voltage, 0 V)
- Fundamental digital logic operators and gates:
  - **NOT, NAND, NOR**
  - **Digital gate:** electronic implementation of an operator

NOT

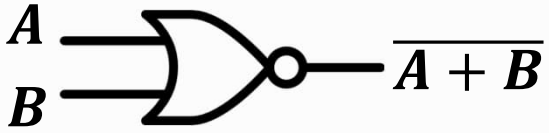
A	$\overline{A}$
0	1
1	0

NAND



A	B	$\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

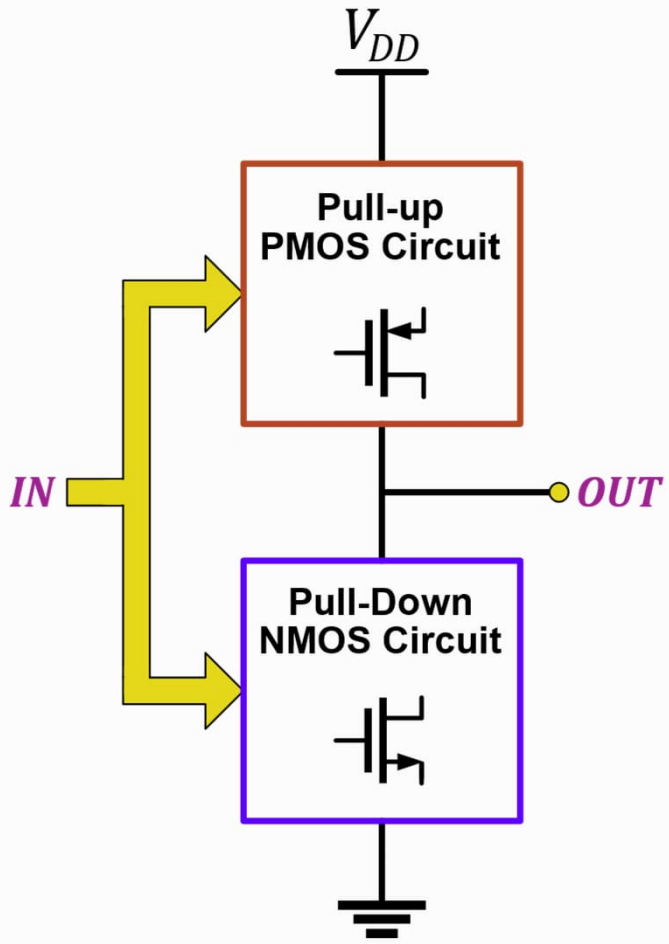
NOR



A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

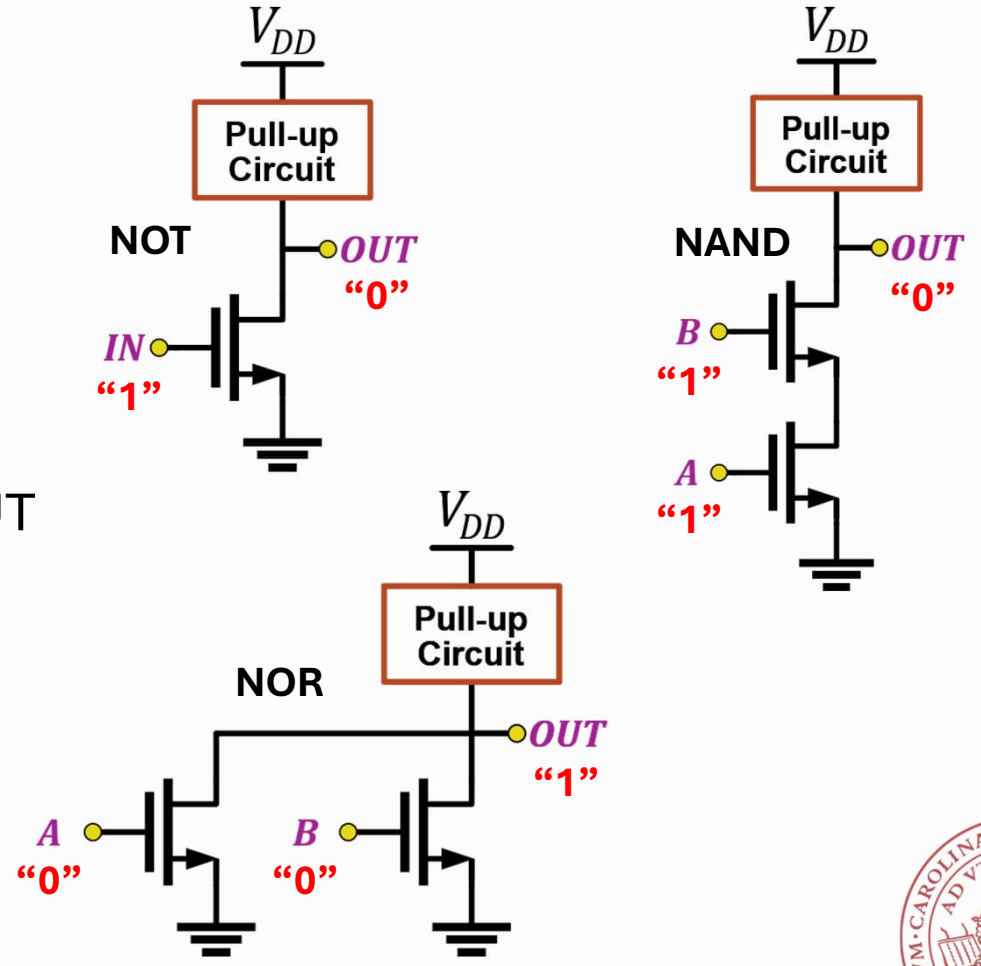
CMOS Logic Gates

- A gate decides to connect the output node to either GND or V_{DD} according to its digital input state (“0” or “1”) and the truth table.
- Lower-half (Pull-down) circuit connects to GND
- Upper-half (Pull-up) circuit connects to VDD
- CMOS construction:
  - **Pull-down:** NMOS
  - **Pull-up:** PMOS



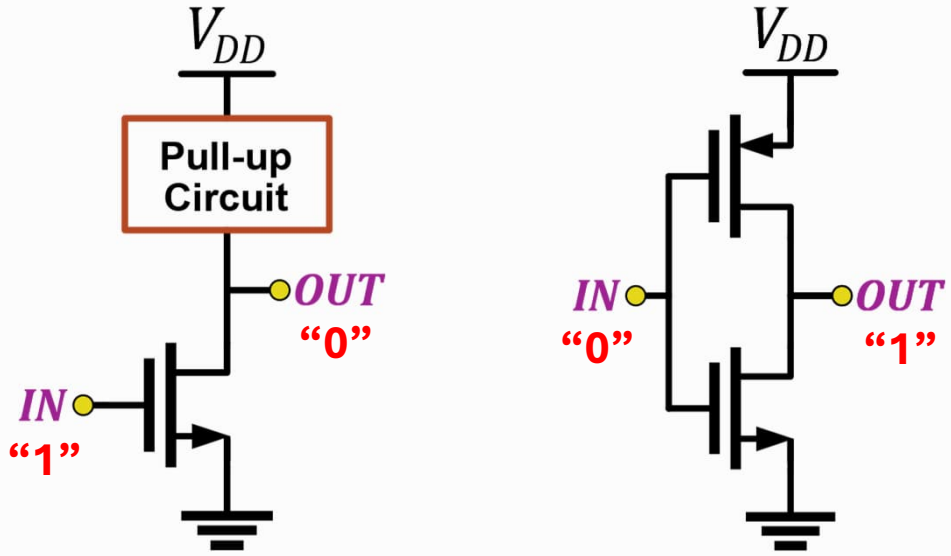
CMOS Logic Gates, Pull-Down

- Start from the lower half
- NMOS switch conducts when its input is “1”
- However, when an NMOS between GND and OUT is ON, the output becomes “0”; therefore:
- **Inverting:** NMOS switch between GND and OUT
- **NAND-ing:** Series NMOS switches
- **NOR-ing:** Parallel NMOS switches

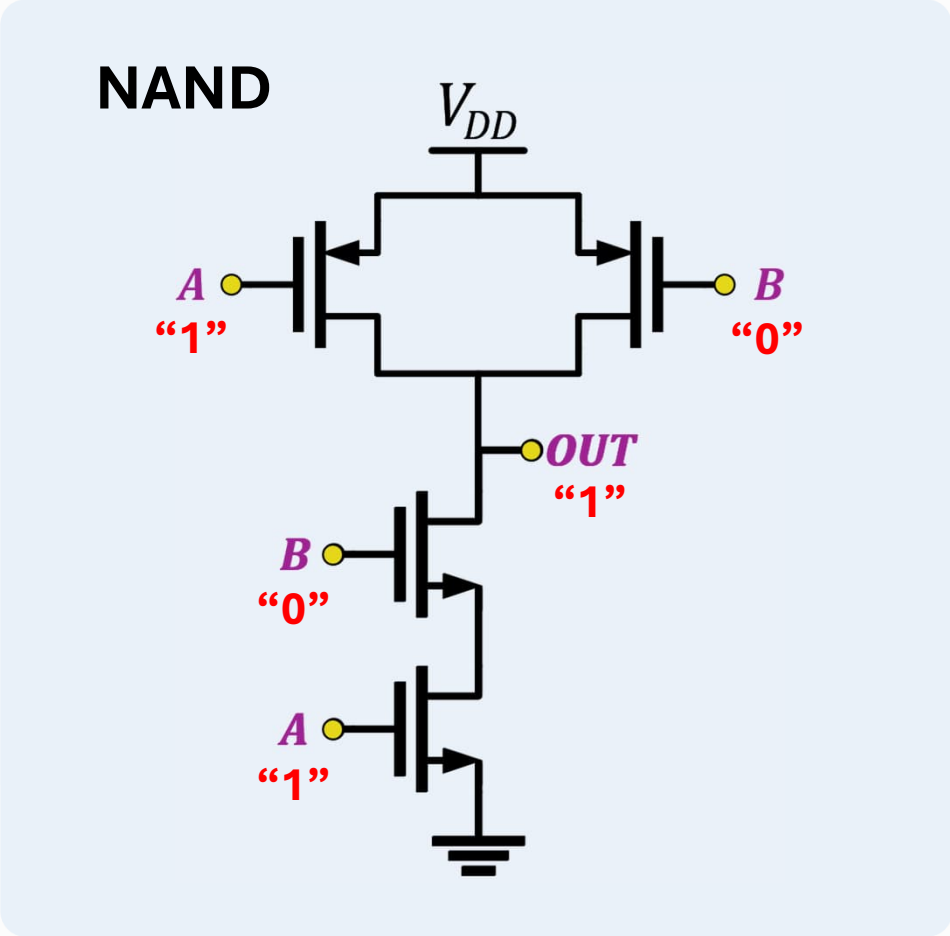


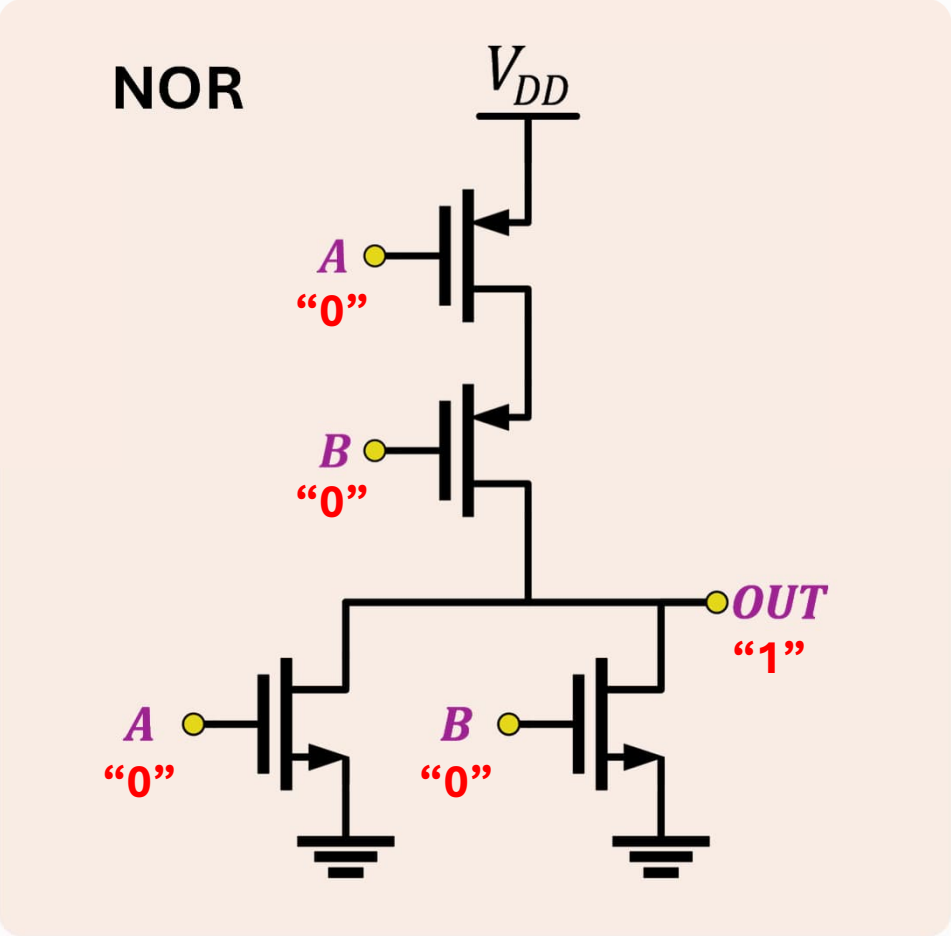
CMOS Logic Gates, Pull-Up

- The upper half complements the lower half.
- **Reminder:** PMOS conducts when it receives a “0” digital input
- **Duality:**
  - **Series NMOS ≡ Parallel PMOS**
  - **Parallel NMOS ≡ Series PMOS**

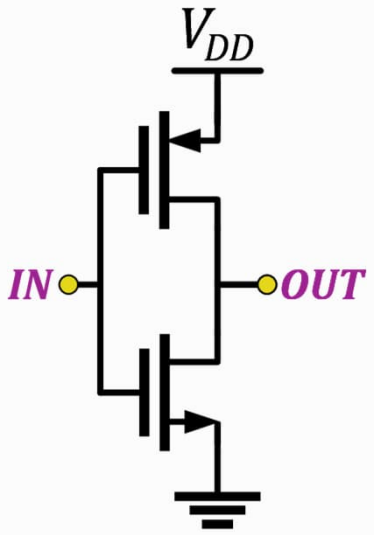


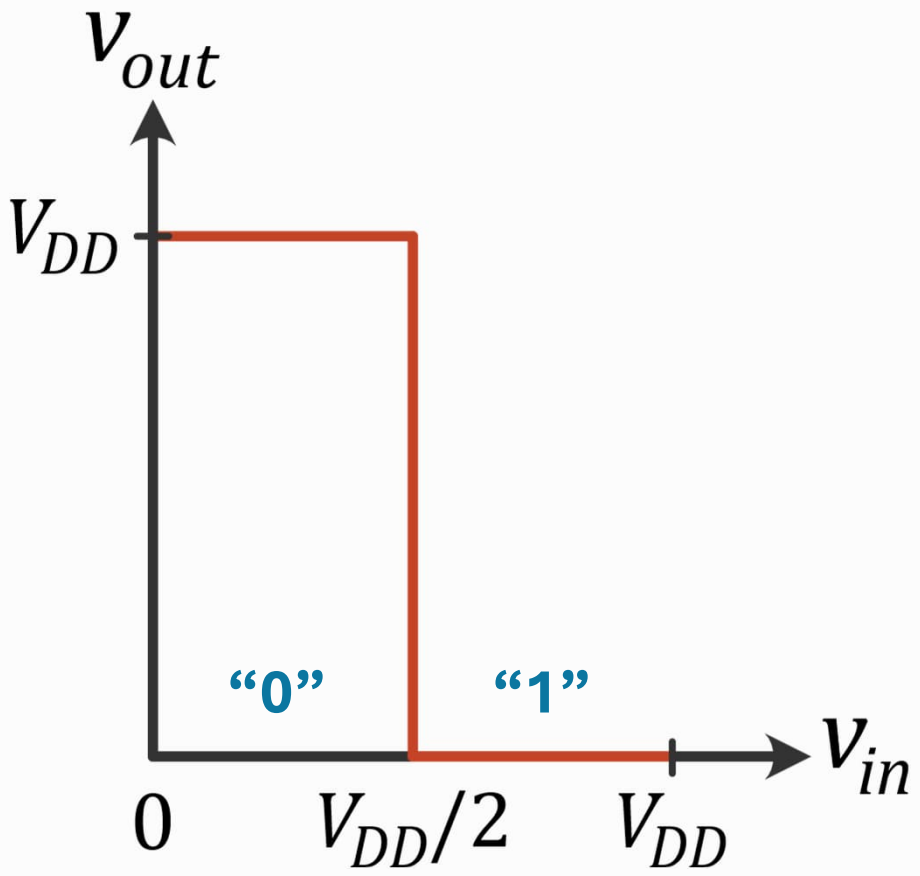
CMOS NAND and NOR





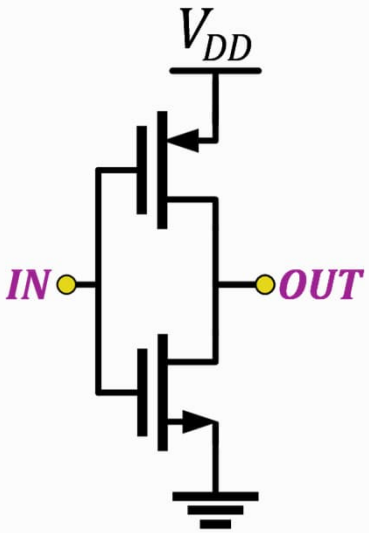
Voltage Transfer Characteristics



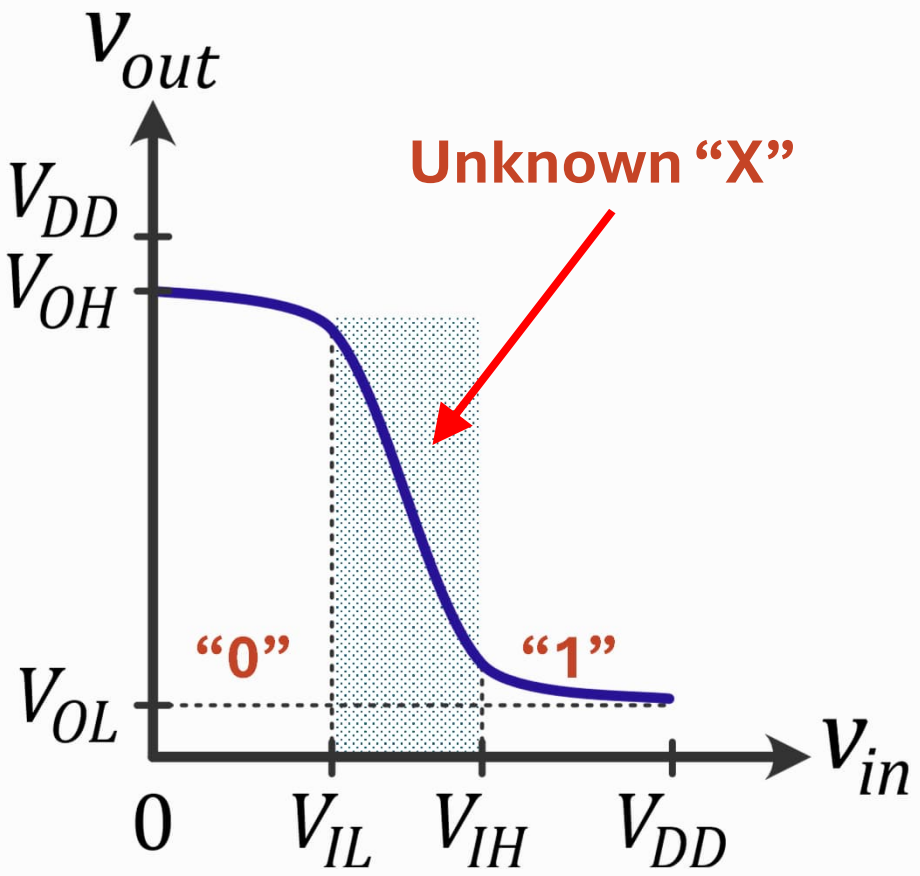


- Ideal input-output characteristics
- Low State: "0" $\equiv [0, V_{DD}/2)$
- High State: "1" $\equiv (V_{DD}/2\,, V_{DD}]$

Voltage Transfer Characteristics

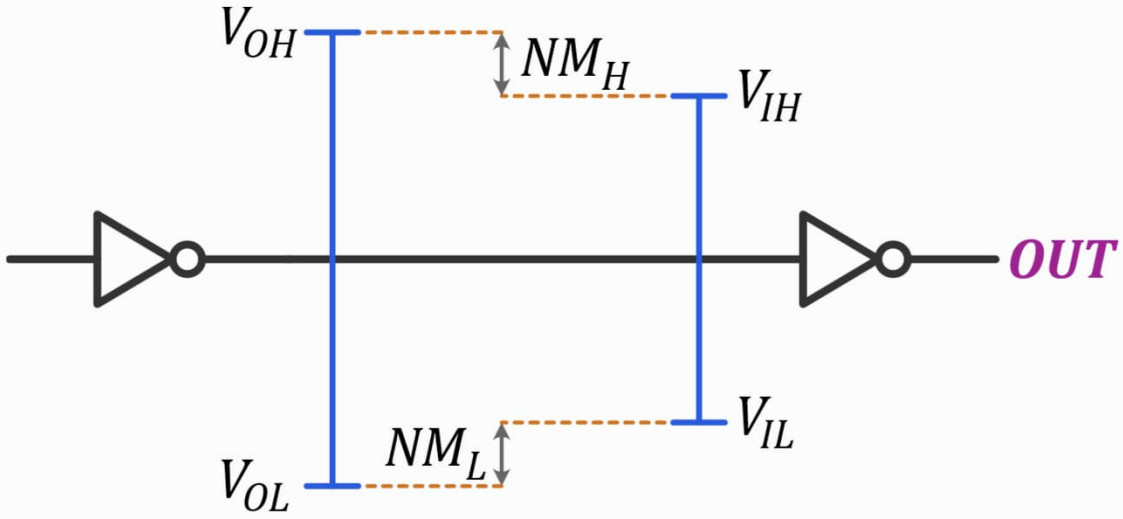


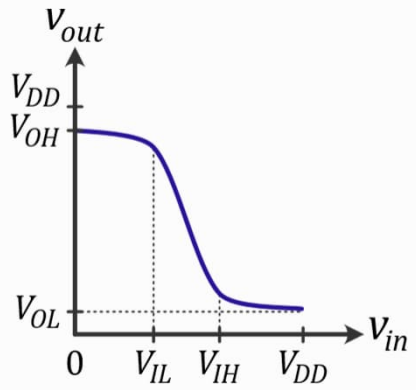
- Realistic input-output characteristics
- Low State: “0” $\equiv [0, V_{IL})$
- High State: “1” $\equiv (V_{IH}, V_{DD}]$



Noise Margin

- **Noise Margin:** Maximum tolerable noise for reliable function
- Sources of Noise:
  - Variations in manufacturing process, temperature and supply voltage (PVT)
  - Radiation waves and magnetic fields
  - Nearby (both on-chip and off-chip) switching circuits



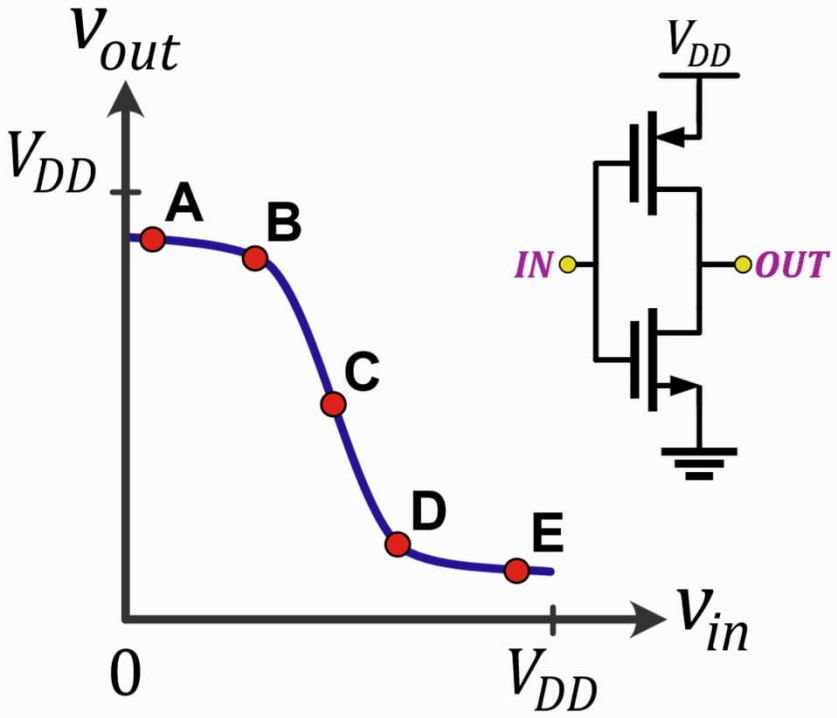


$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$

Pause and Ponder 2

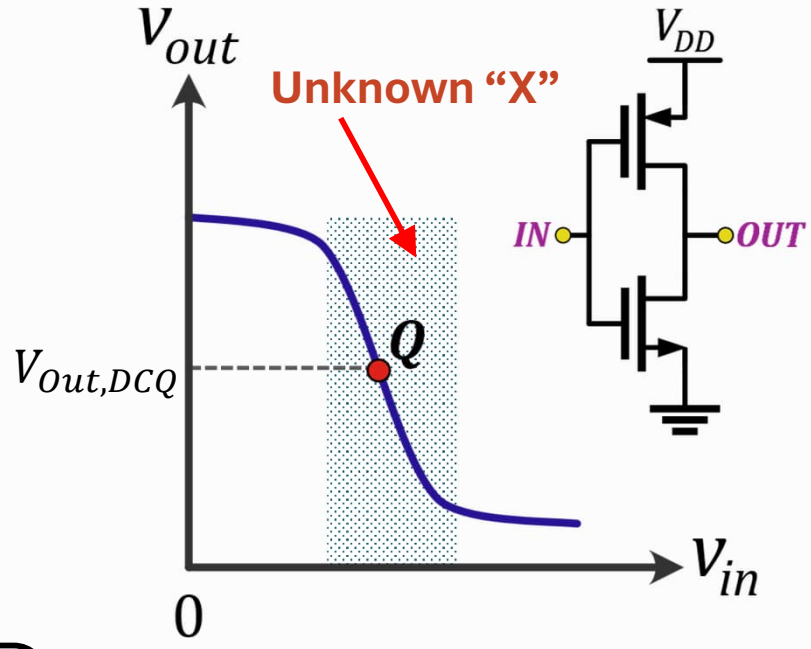
- Could you specify the operating region (cut-off, linear, saturation) for NMOS and PMOS transistors at each point?



Operating Point	NMOS	PMOS
A	Cut-off	Linear
B	Saturation	Linear
C	Saturation	Saturation
D	Linear	Saturation
E	Linear	Cut-off

Unknown (“X”) does NOT equate to useless!

- When both transistors operate in saturation, the inverter amplifies the input signal.
- **DC Operating Point (Q):** Identified by DC operating current (i_D) and voltages (V_{DS} and V_{GS}) of each transistor.
- **Gain (A_v):** the ratio of signal amplitudes

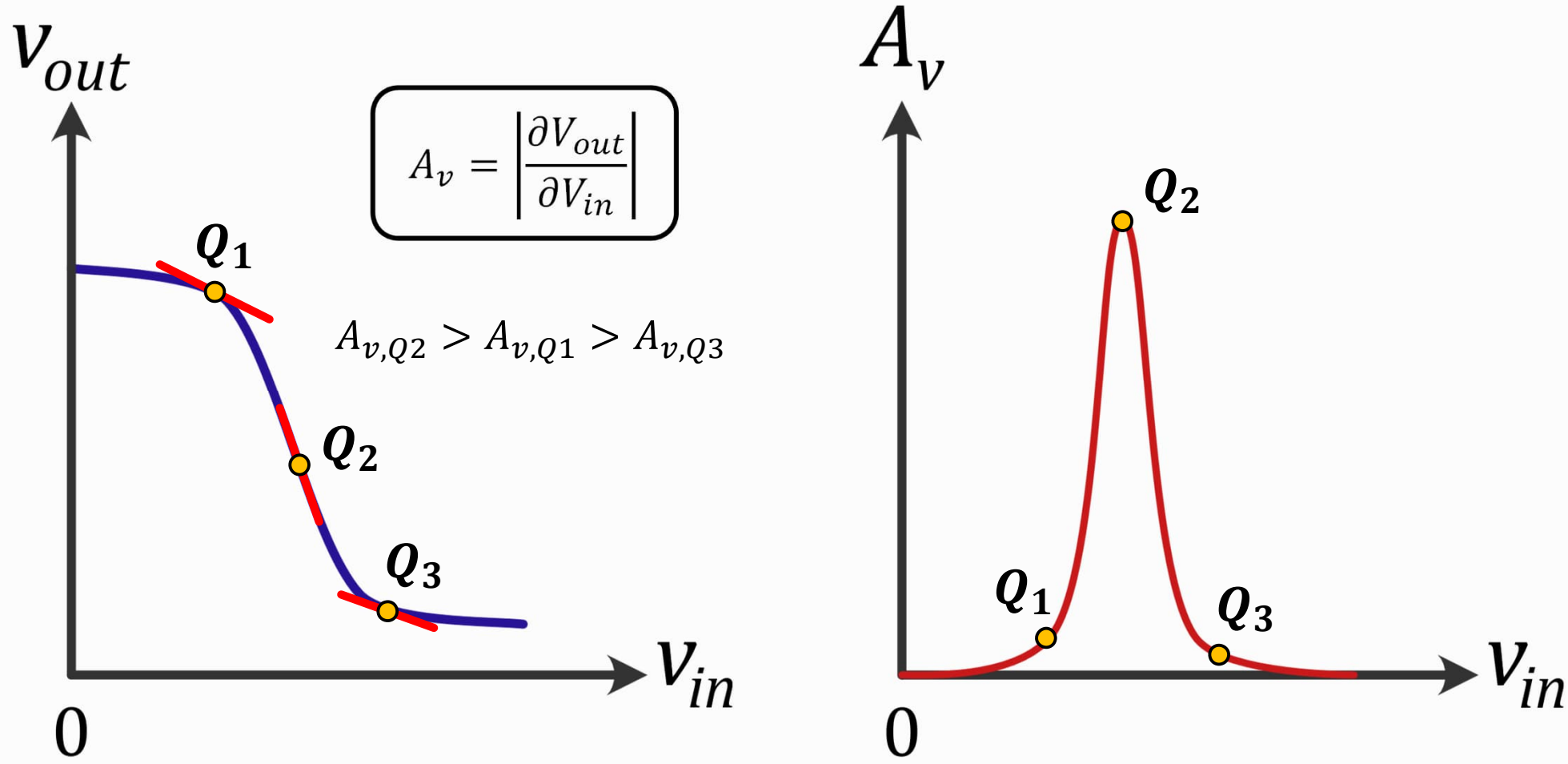


$$A_v = \left|\frac{v_{out,sig}}{v_{in,sig}}\right|$$

$$v_{out,Q} = v_{Out,DCQ} + A_v v_{in,sig}$$

$$\Rightarrow \quad A_v = \left|\frac{\partial v_{out}}{\partial v_{in}}\right|$$

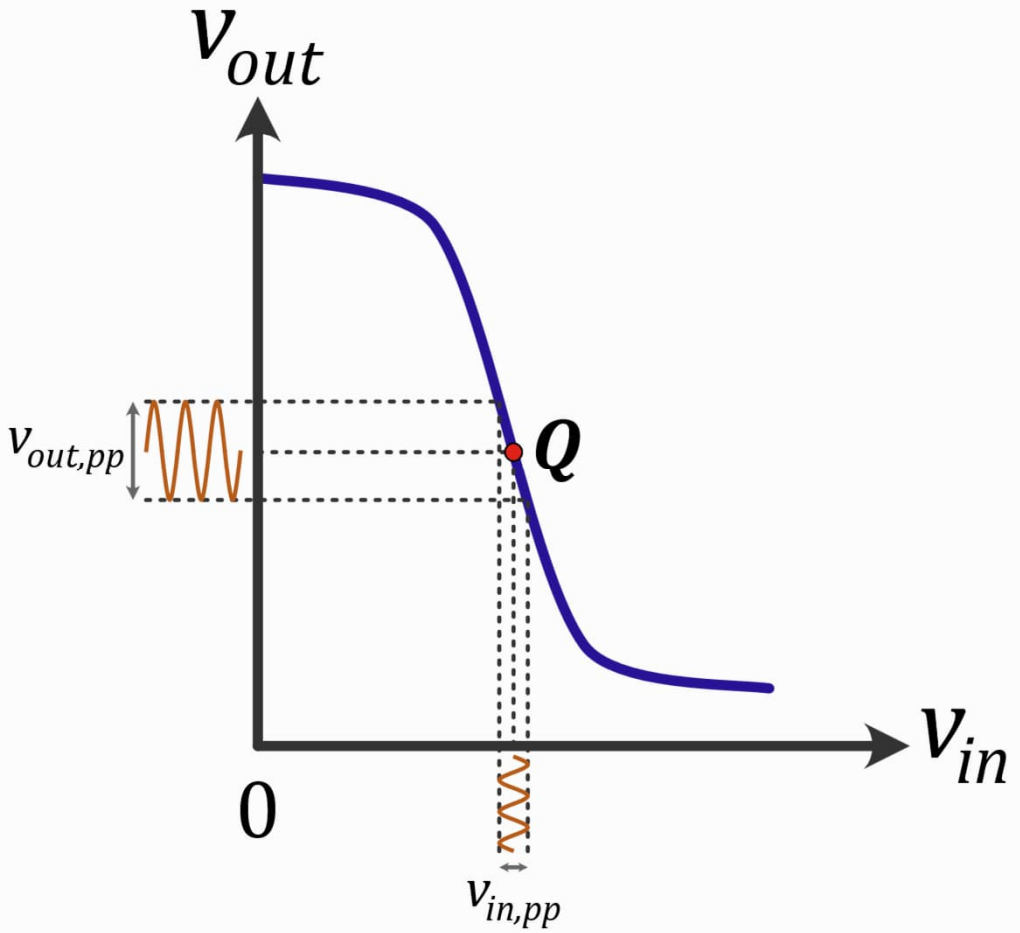
Voltage Gain



Voltage Gain (signal illustration)

- **pp:** peak-to-peak value

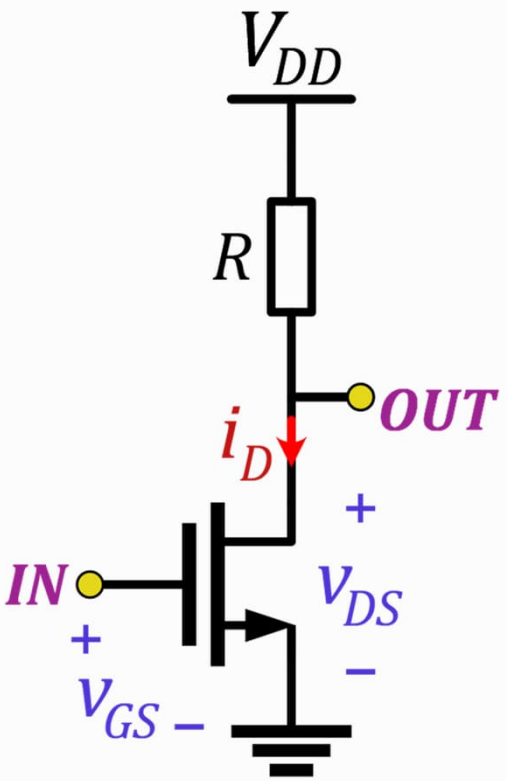
$$A_v = \left| \frac{v_{out,pp}}{v_{in,pp}} \right|$$



Circuit Analysis: Graphical Method

- **Step 1:** Write a linear equation for $i - v$ relationship of nonlinear device (transistor, diode, etc.)

KVL: $V_{DD} = Ri_D + v_{DS} \Rightarrow$ $\boxed{i_D = \frac{V_{DD}}{R} - \frac{v_{DS}}{R}}$



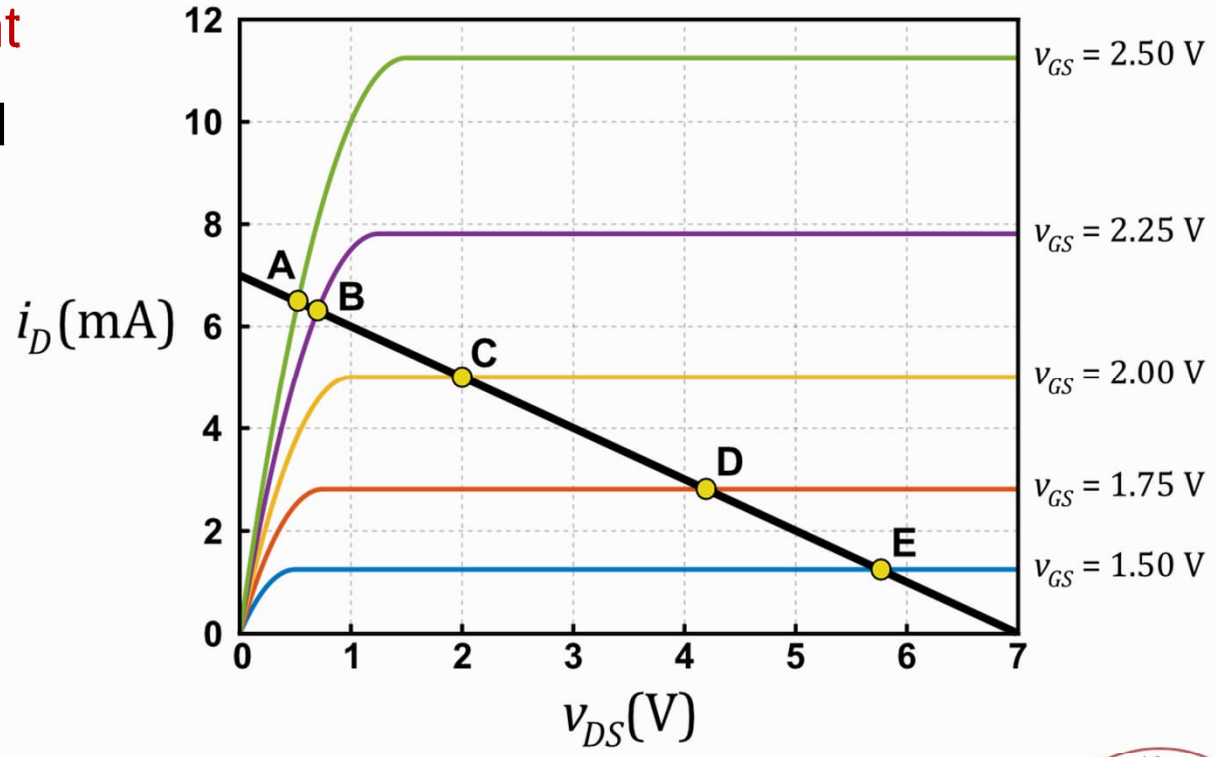
- Example: $V_{DD} = 7\ V, R = 1\ \text{k}\Omega$

$$\boxed{i_D = 7\ \text{mA} - \frac{v_{DS}}{1000}}$$

Circuit Analysis: Graphical Method

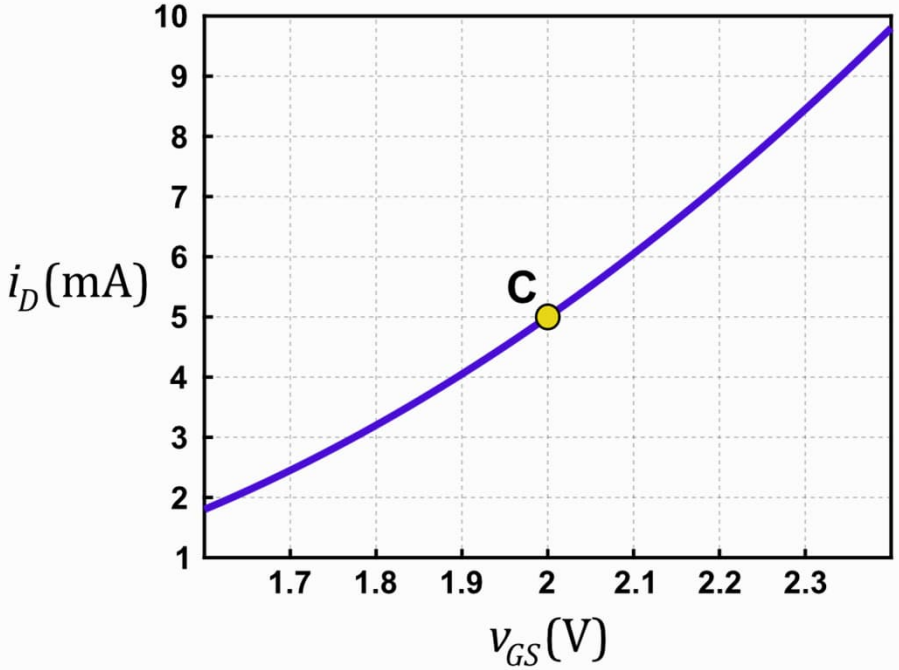
- **Step 2:** Determine the operating point by intersecting the linear function and nonlinear characteristic curves of device.
- A and B: linear region → no gain ☹
- C, D, and E: saturation → ☺
- Let's pick C!

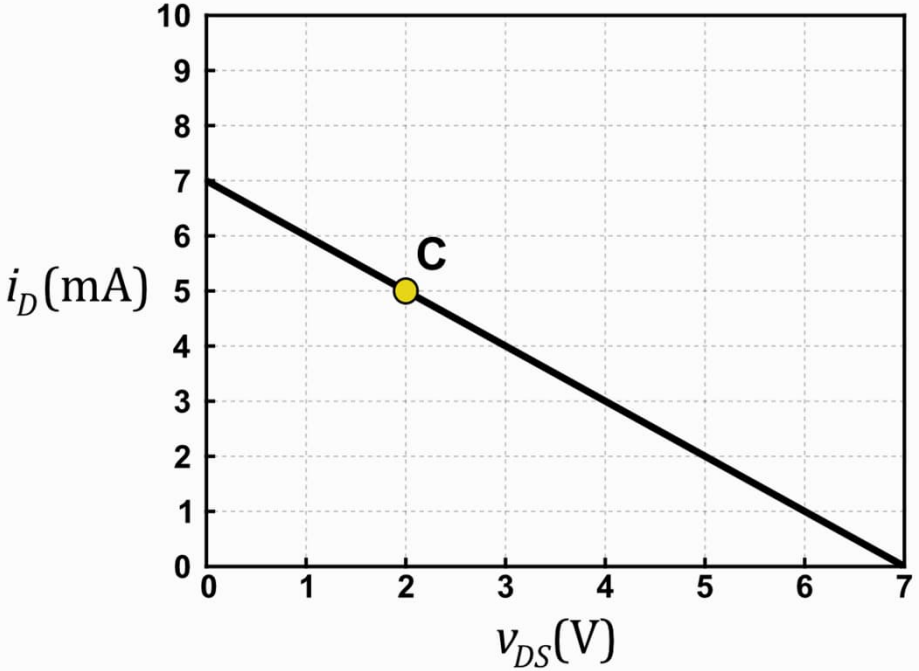
→ $V_{GS,C} = 2\ \text{V}, V_{DS,C} = 2\ \text{V}, I_{D,C} = 5\ \text{mA}$

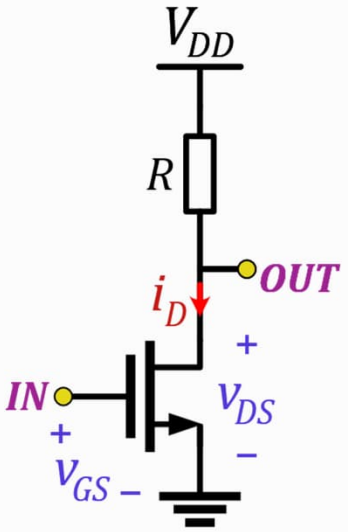


Circuit Analysis: Graphical Method

- **Step 3:** Find voltage gain from $v_{in} - v_{out}$ curve.







$v_{in} = v_{GS}$

$v_{out} = v_{DS}$

Circuit Analysis: Graphical Method