Elektronik

ADDA Circuits

EITA10

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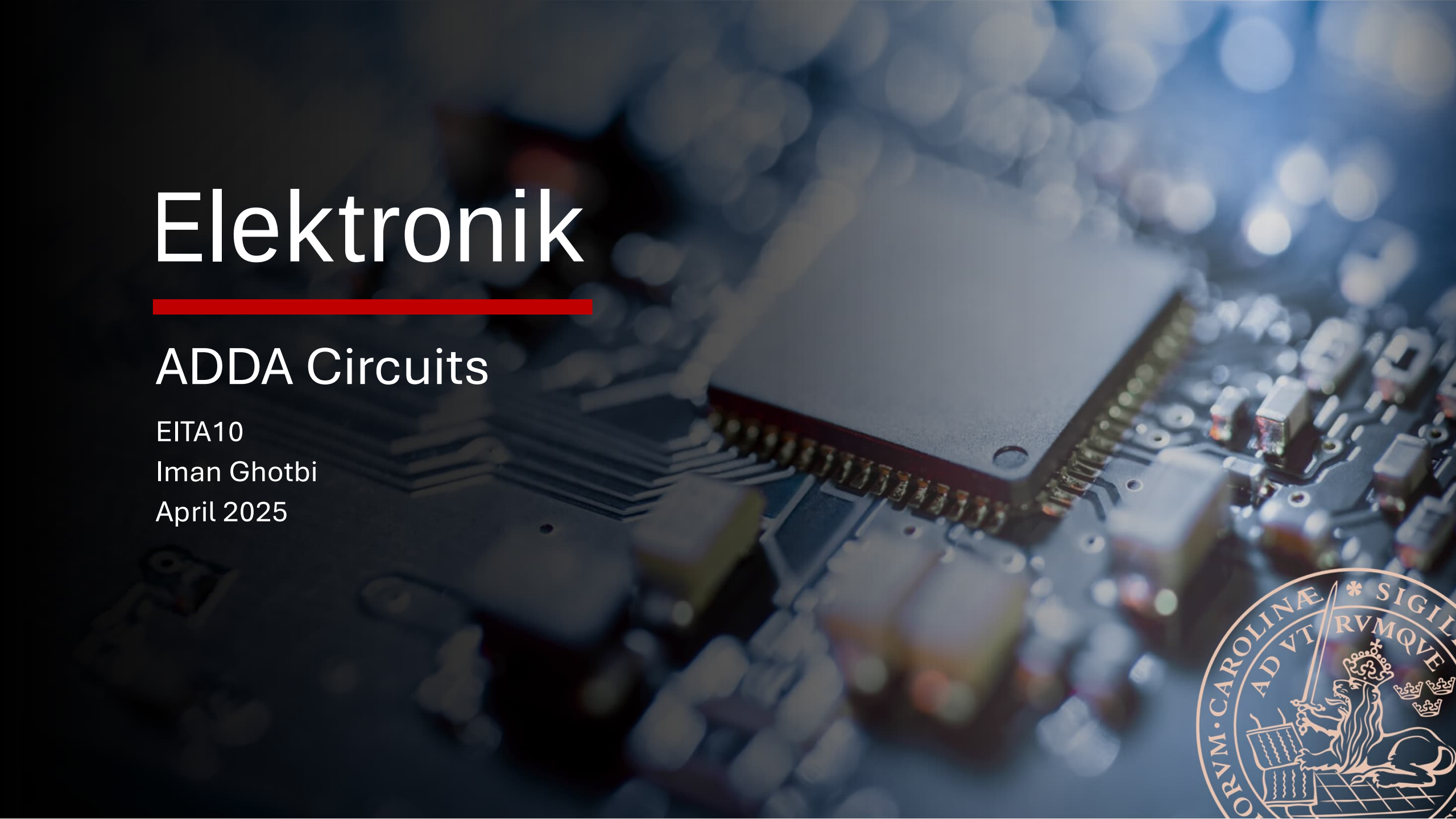
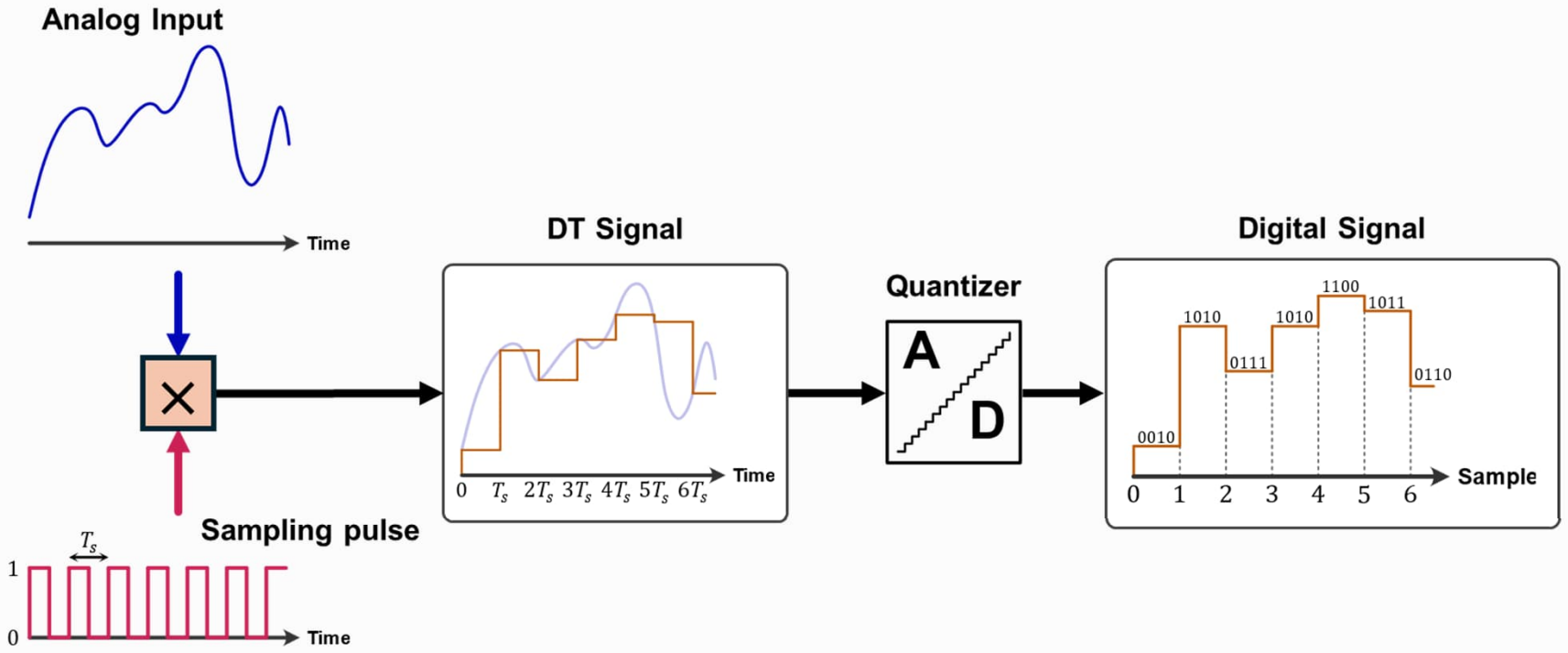


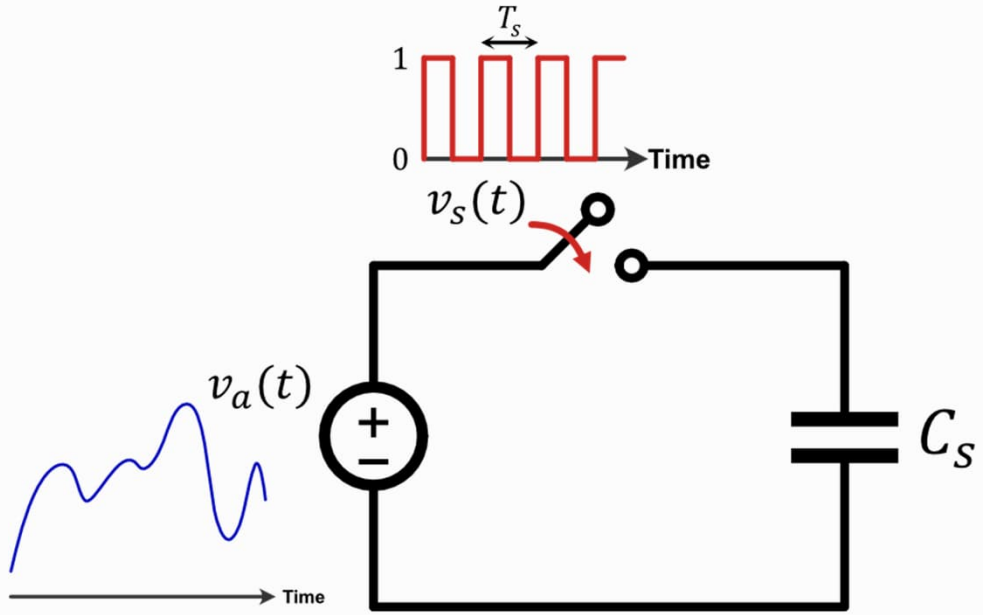
Data Converter Circuits

- Sample-and-Hold (SAH)
- Discrete-time Quantizers



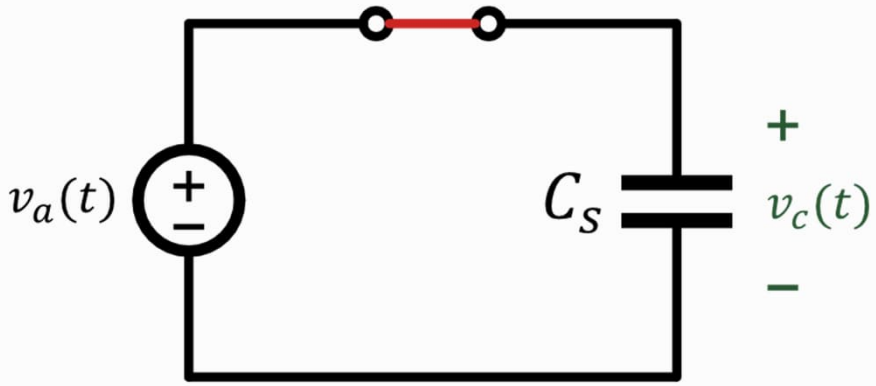
Sample-and-Hold Circuit

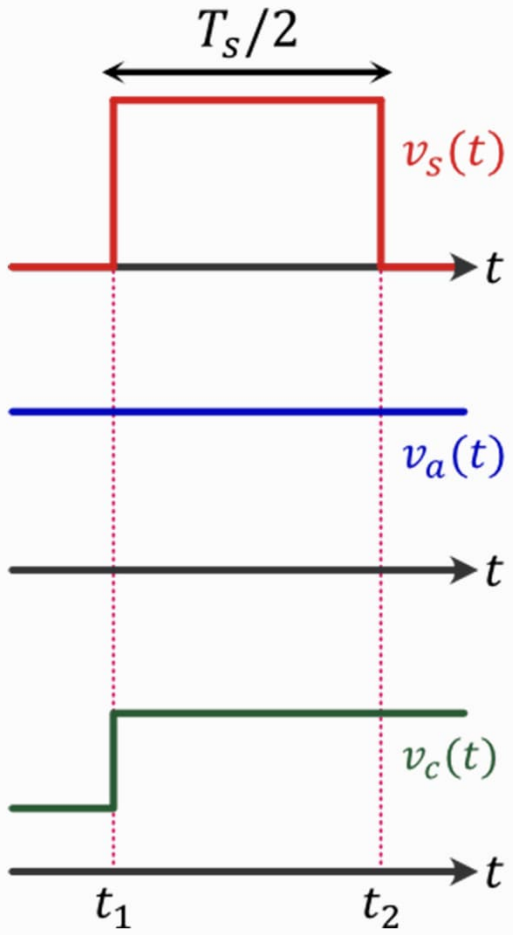
- A pulse train for sampling
  - Could be a smoother waveform in practice
- A sampling capacitor (C_s)
- A switch (SW)
- Two-phase operation:
  - Sampling: SW = ON
  - Holding SW = OFF



Sample-and-Hold Circuit

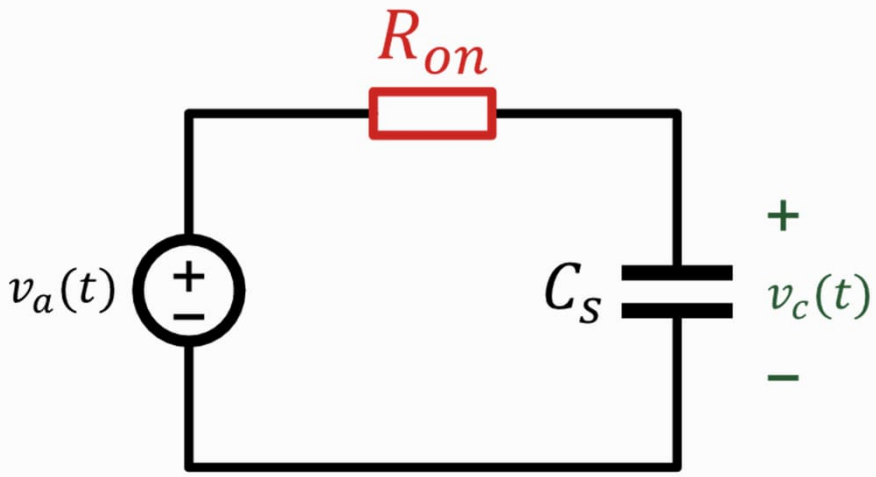
- **Sampling Phase (SW:ON)**
  - Slow-moving (**low-frequency**) input signal

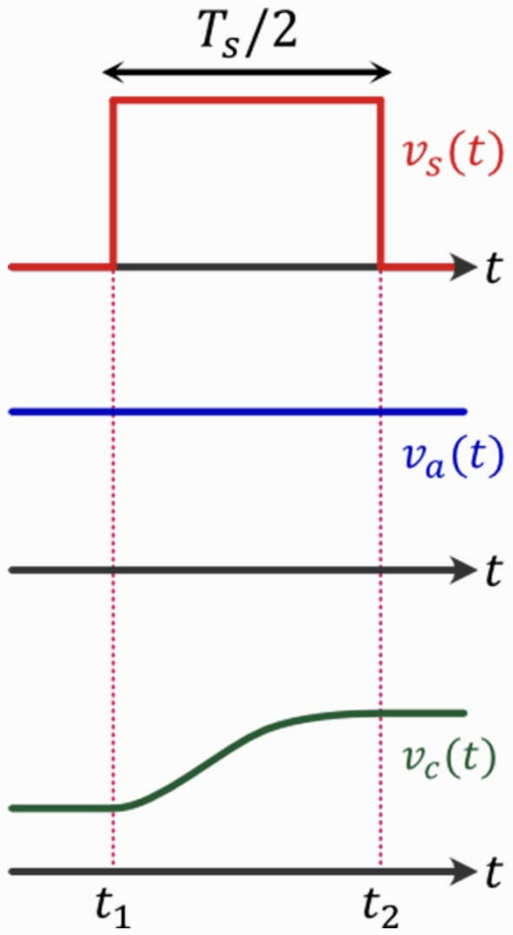




Sample-and-Hold Circuit

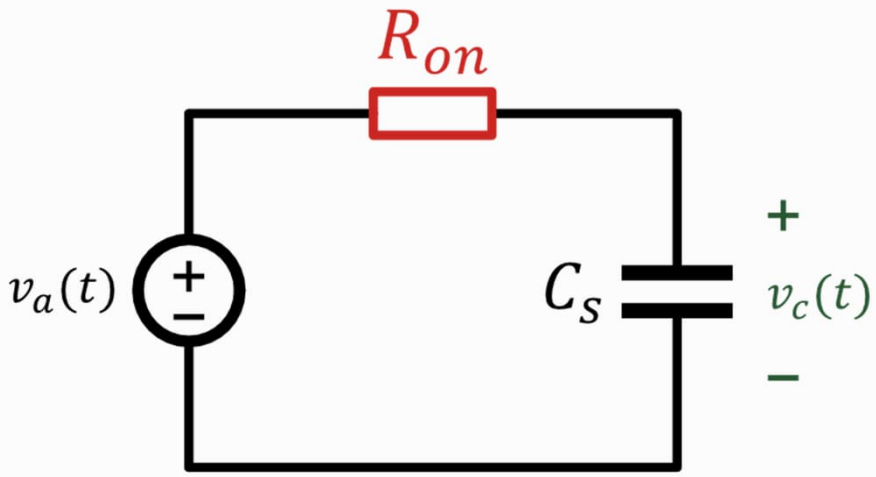
- **Sampling Phase (SW:ON)**
  - Slow-moving (low-frequency) input signal
  - Switch ON-resistance
  - Delay in sampling: $\tau = R_{on}C_s$



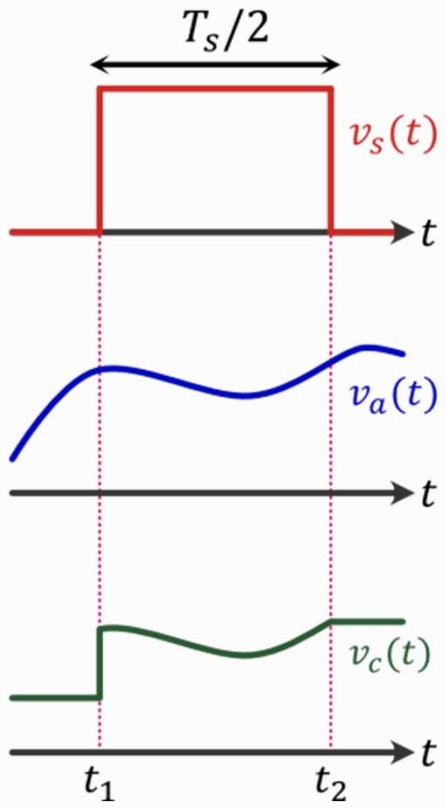


Sample-and-Hold Circuit

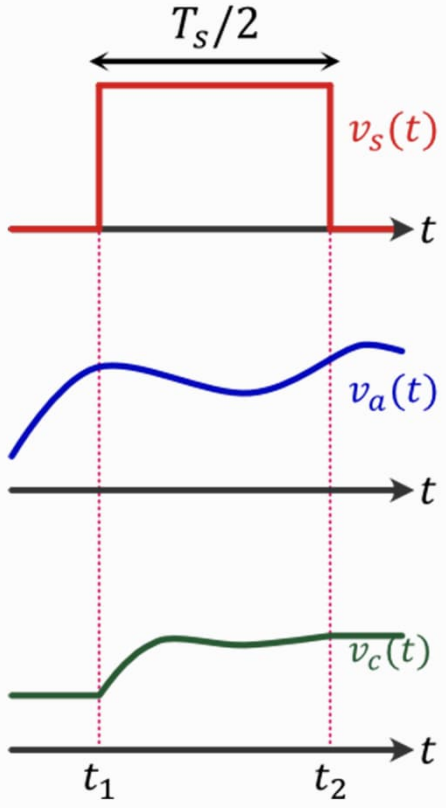
- **Sampling Phase (SW:ON)**
  - fast-moving (**high-frequency**) input signal



Ideal switch ($R_{on} = 0$)

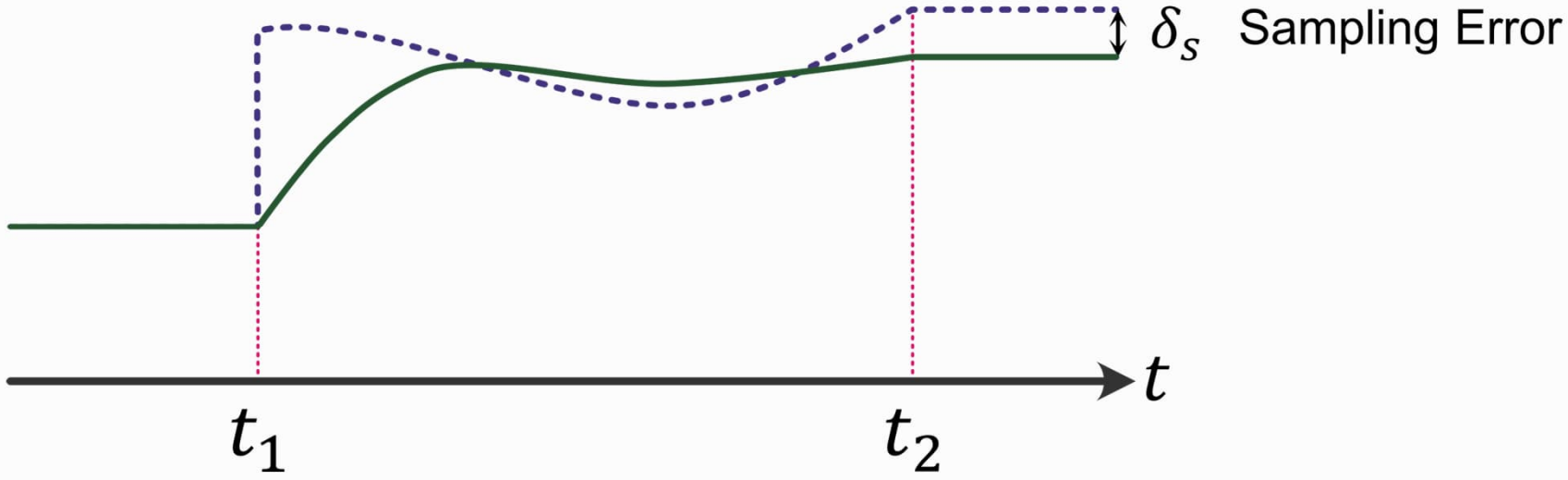


Practical switch ($R_{on} \neq 0$)



Sample-and-Hold Circuit

- **Sampling Phase (SW:ON)**
  - fast-moving (high-frequency) input signal
  - Sampling error
  - Limitation on the maximum input frequency (**sampling bandwidth**)



Pause and Ponder 1

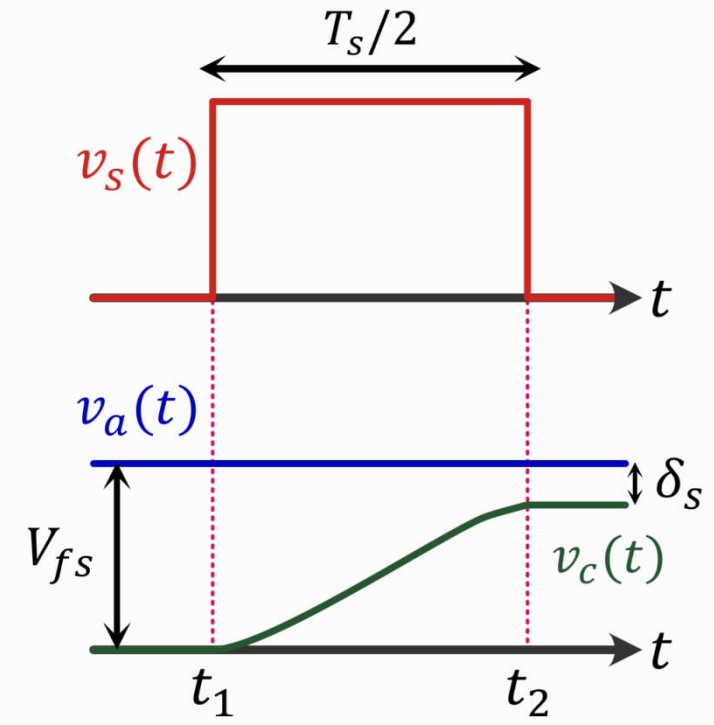
- What is the highest acceptable input frequency for keeping the sampling error below V_{LSB} in an N-bit ADC?

$$f_{s,max} = f_{Nyquist} = 2f_{in,max}$$

$$v_c(t) = V_{fs}\left(1 - e^{-(t-t_1)/\tau}\right)u(t-t_1)$$

$$\delta_s = V_{fs} - v_c(t_2) = V_{fs}e^{-(t_2-t_1)/\tau} = V_{fs}e^{-T_s/2\tau}$$

$$\delta_s \leq V_{LSB} \approx \frac{V_{fs}}{2^N} \quad \Rightarrow \quad T_{s,min} = 2N(\ln 2)\tau$$



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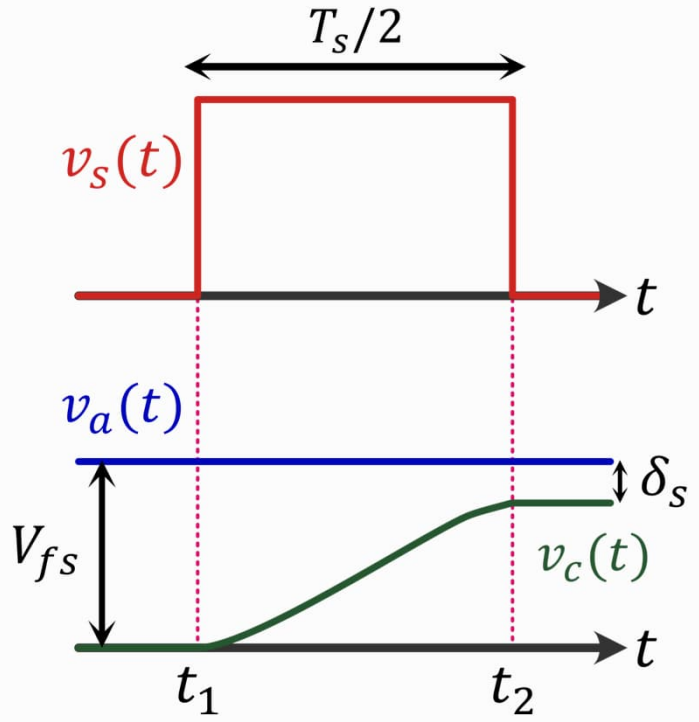


$$f_{s,max} = f_{Nyquist} = 2f_{in,max}$$

$$T_{s,min} = 2N(\ln 2)\tau \quad \Rightarrow \quad f_{s,max} = \frac{1}{2N(\ln 2)\tau}$$

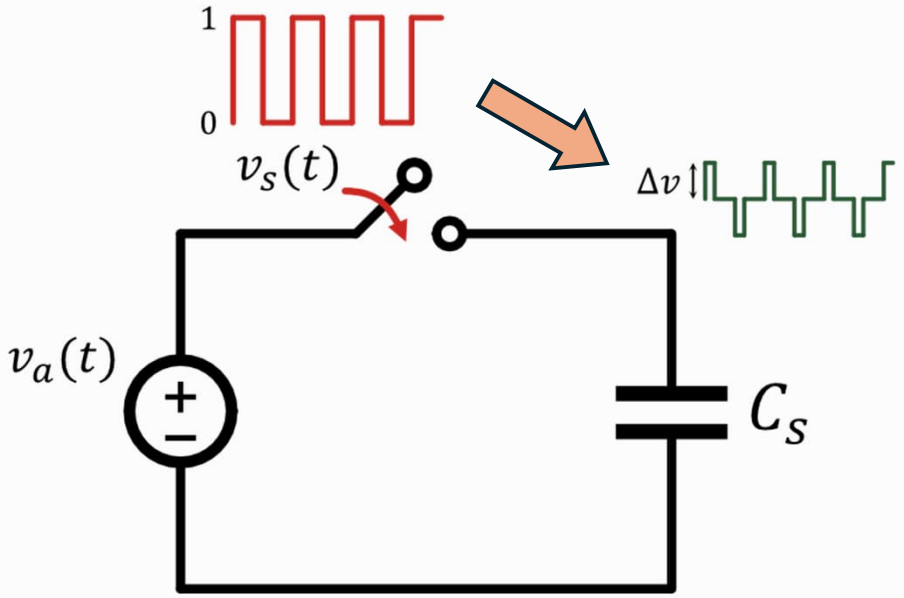
$$\Rightarrow \boxed{f_{in,max} = \frac{1}{4N(\ln 2)\tau}}$$

Example: $\tau = 20$ ps, $f_{in} = 2$ GHz
$\Rightarrow N_{max} = 9$

Sample-and-Hold Circuit

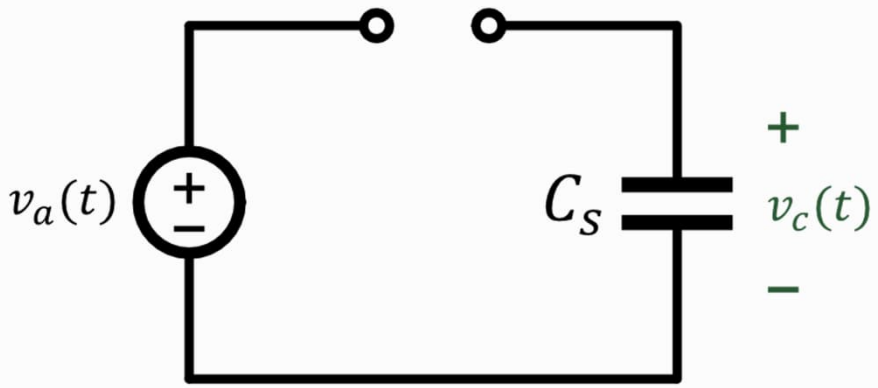
- Sampling Phase Nonidealities:
  - **Clock feedthrough**
    - Caused by parasitic capacitors
    - Clock harmonics
    - DR degradation, output glitches
  - **Nonlinearities**
    - Input-dependent delay

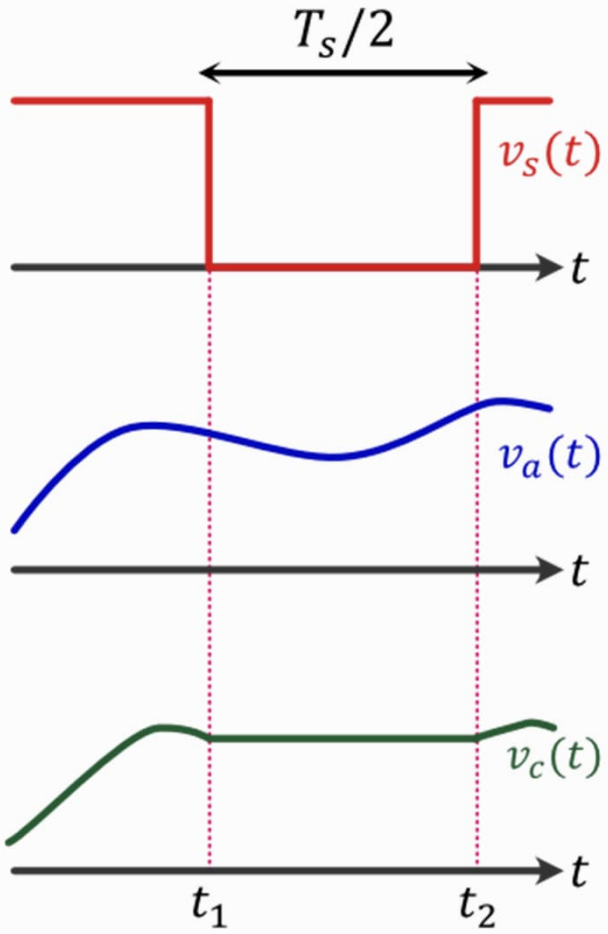
    → code-dependent sampling error
    - Input-dependent feedthrough



Sample-and-Hold Circuit

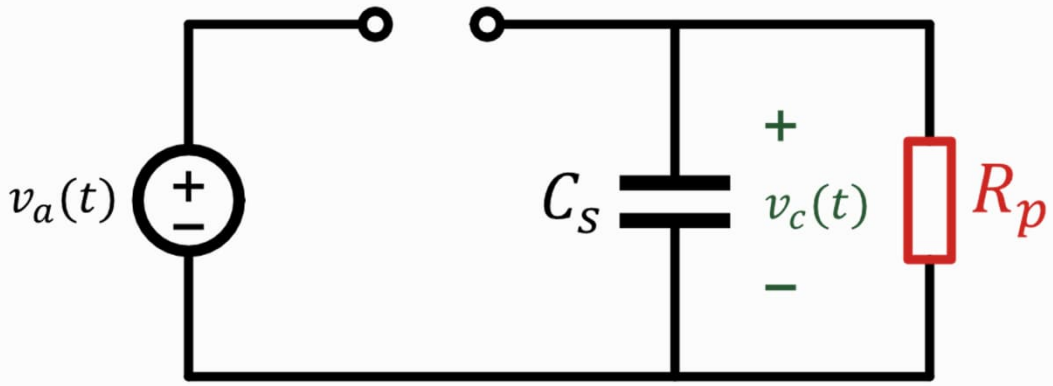
- **Holding Phase (SW:OFF)**
  - Ideal switch (open-circuit)
  - Sampling capacitor preserves its charge

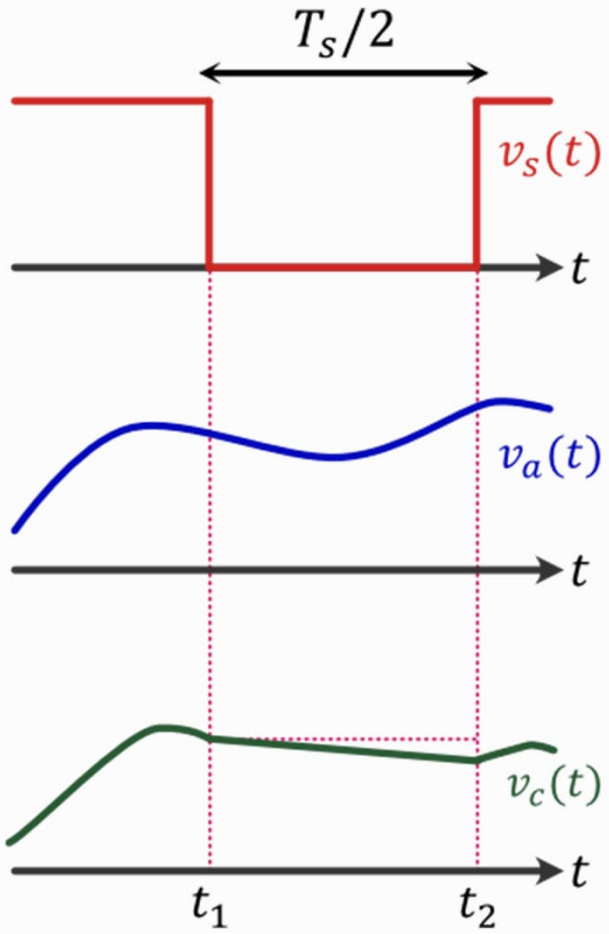




Sample-and-Hold Circuit

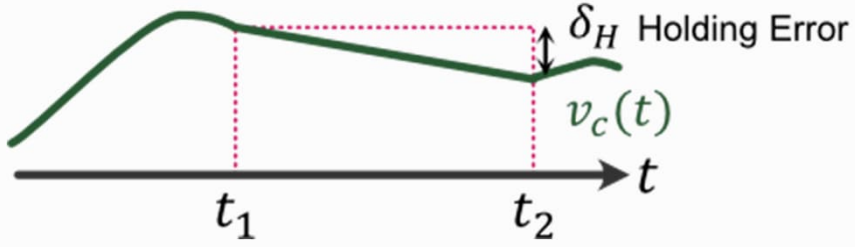
- **Holding Phase (SW:OFF)**
  - Parasitic resistance (leakage current)
  - R_p partially discharges C_S
  - $\tau = R_p C_S$





Pause and Ponder 2

- We are oversampling the signal $v_a = 2\cos(2\pi \times 10^7 t)$ with a 100 MHz pulse. How many digital codes are lost because of a leaky S/H circuit with C_S = 1 pF and R_p = 20 kΩ if we use a 10-bit quantizer?



$$v_c(t) = V_{fs}e^{-(t-t_1)/\tau}u(t-t_1) \qquad \tau = R_pC_S = 20\text{ ns} \qquad V_{LSB} = \frac{V_{fs}}{2^N - 1} = 1.96\text{ mV}$$

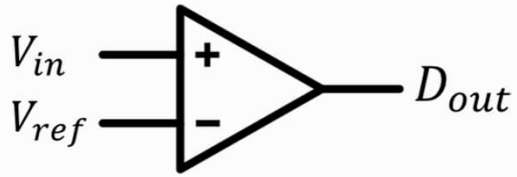
$$\delta_H = V_{fs} - v_c(t_2) = V_{fs}\left(1 - e^{-(t_2-t_1)/\tau}\right) = V_{fs}\left(1 - e^{-T_s/2\tau}\right) = 0.442\text{ V}$$

$$2^{N_{eff}} = \frac{V_{fs} - \delta_H}{V_{LSB}} \approx 795 \Rightarrow \begin{cases} D_{lost} = 1023 - 795 \approx 228 \\ N_{eff} = 9.63 \end{cases}$$

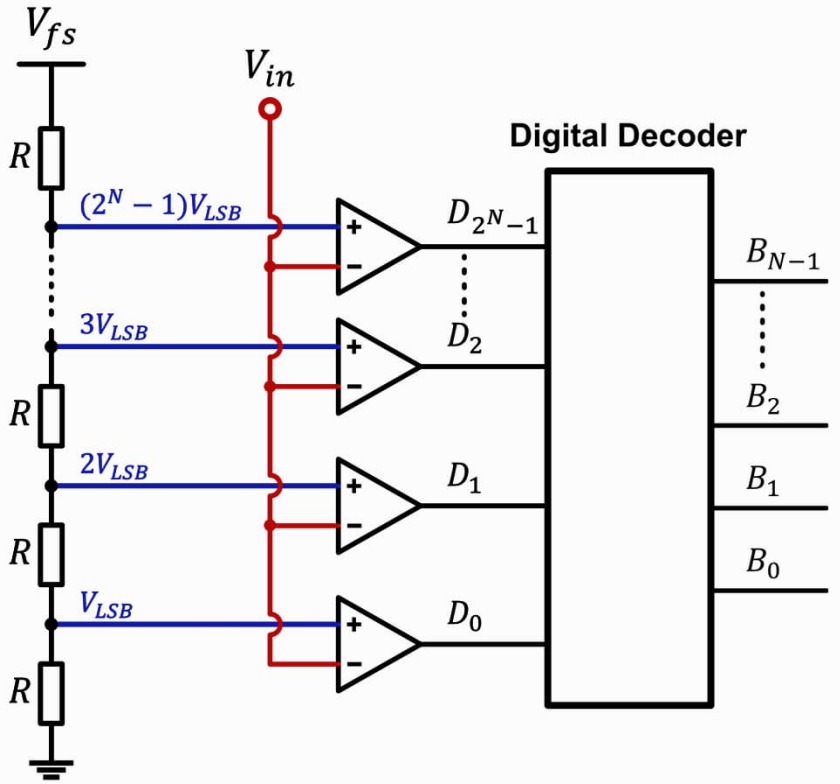
Flash ADC

- Analog comparator

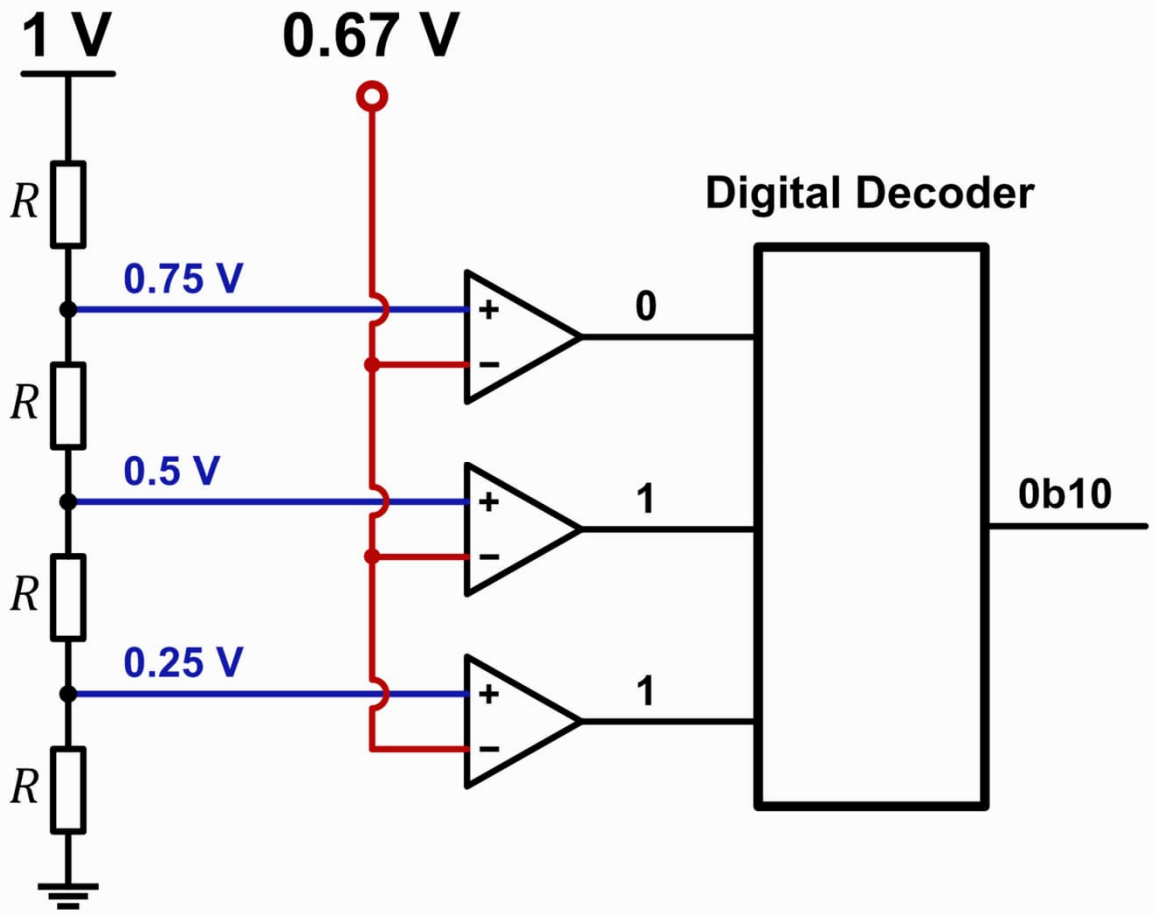
$$D_{out} = \begin{cases} 1 & ; V_{in} \geq V_{ref} \\ 0 & ; V_{in} < V_{ref} \end{cases}$$



- Reference voltage generation
  - Resistor ladder
- Fast conversion
  - All bits ready in just a single clock cycle
- Power inefficient and bulky
  - 2^N resistors and 2^N-1 comparators

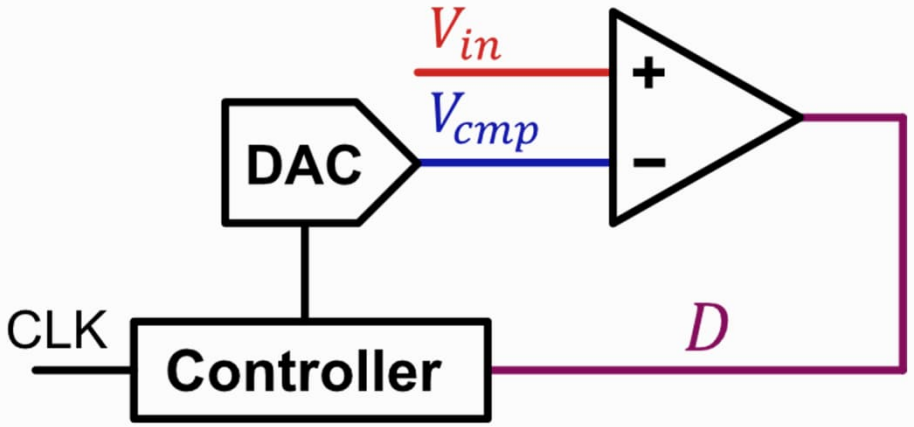


Flash ADC – Example



Successive Approximation ADC

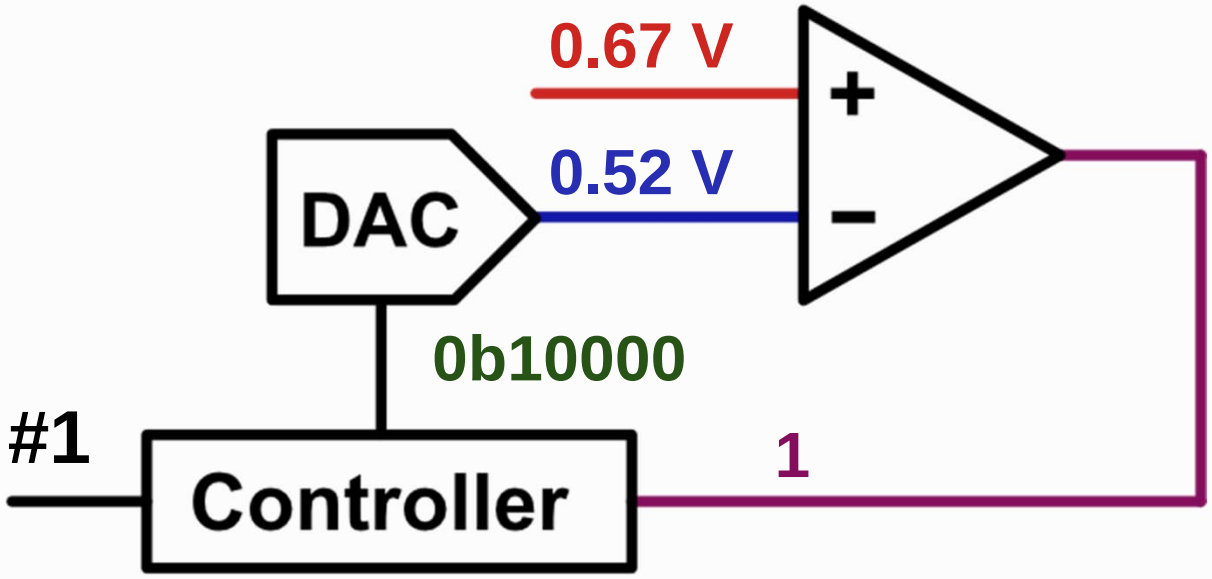
- An example of a multiple-cycle ADCs
  - Complete conversion takes *N* clock cycles
- Bit-by-bit approximation
- Power efficient and easy to scale for higher resolution
- SAR ADC in the literature

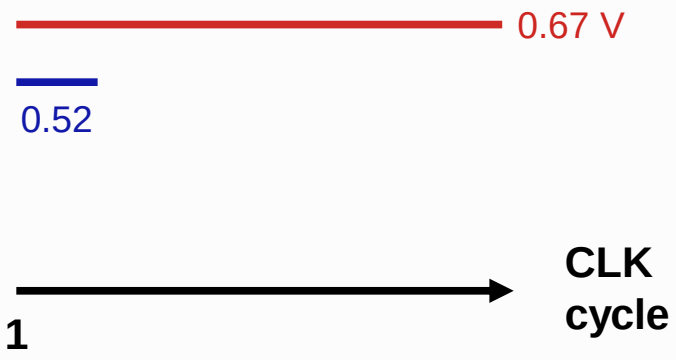


$$\begin{cases} \text{drop the bit} & ; D = 0 \\ \text{keep the bit} & ; D = 1 \end{cases}$$

Successive Approximation ADC – Example

- $N = 5, V_{fs} = 1\ V$





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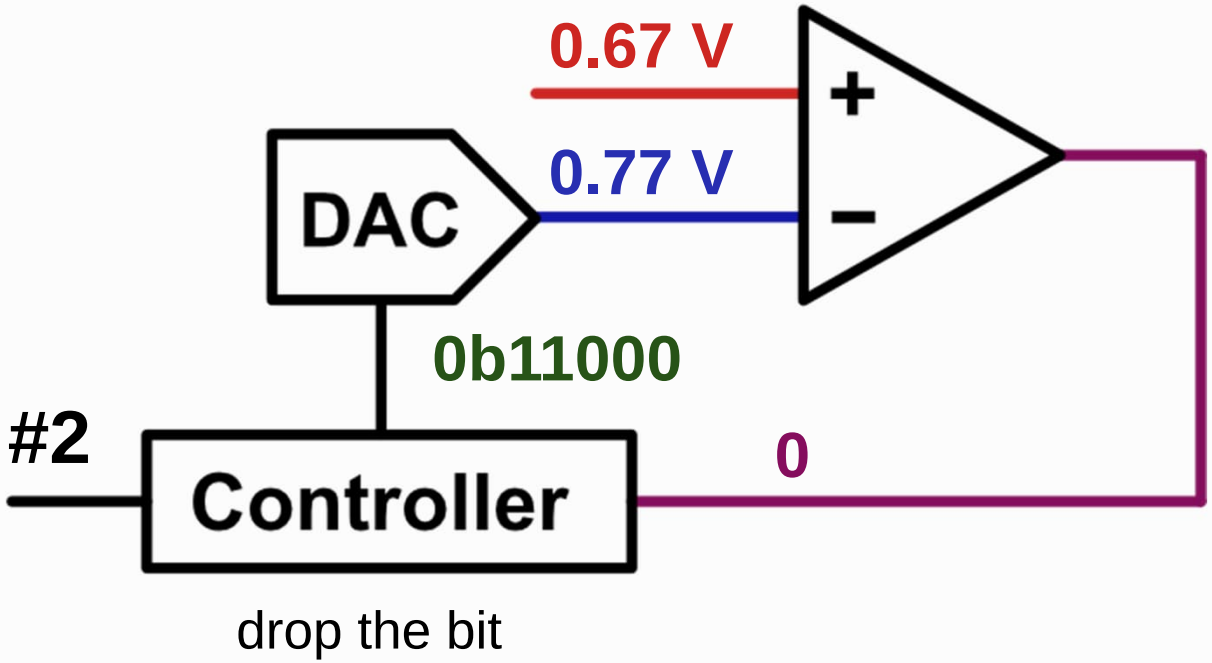

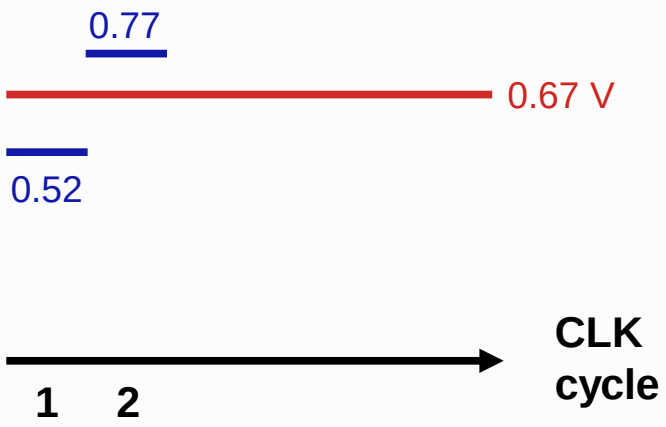

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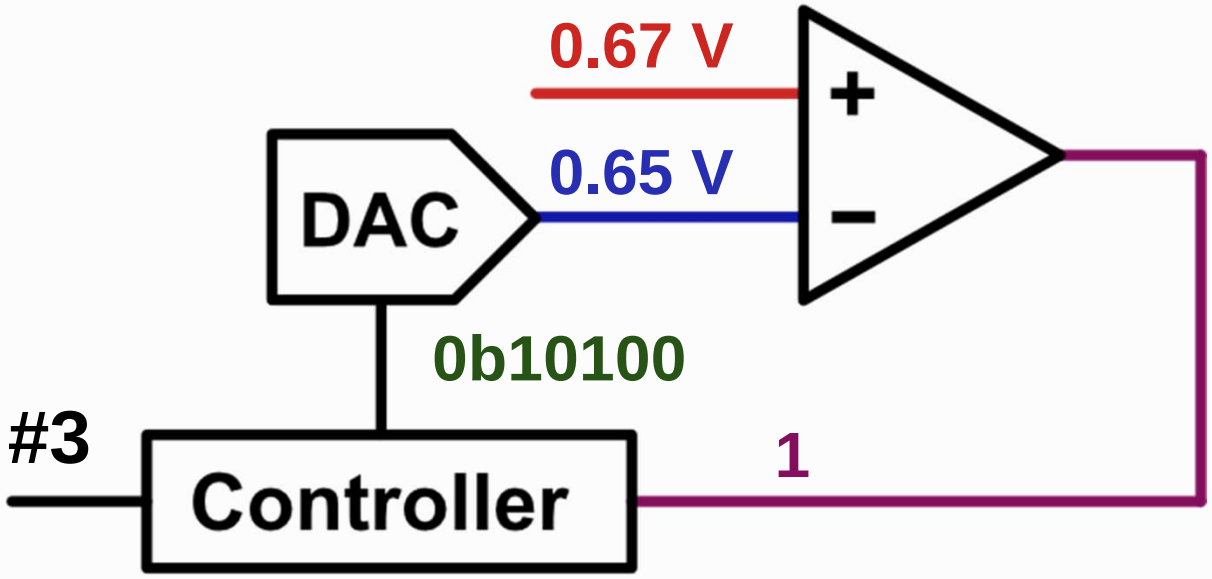

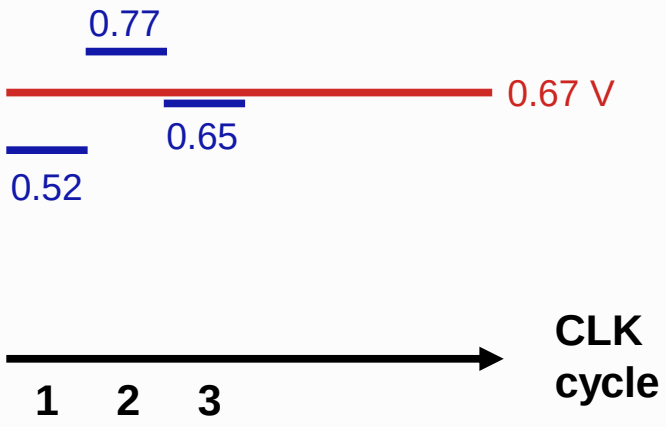

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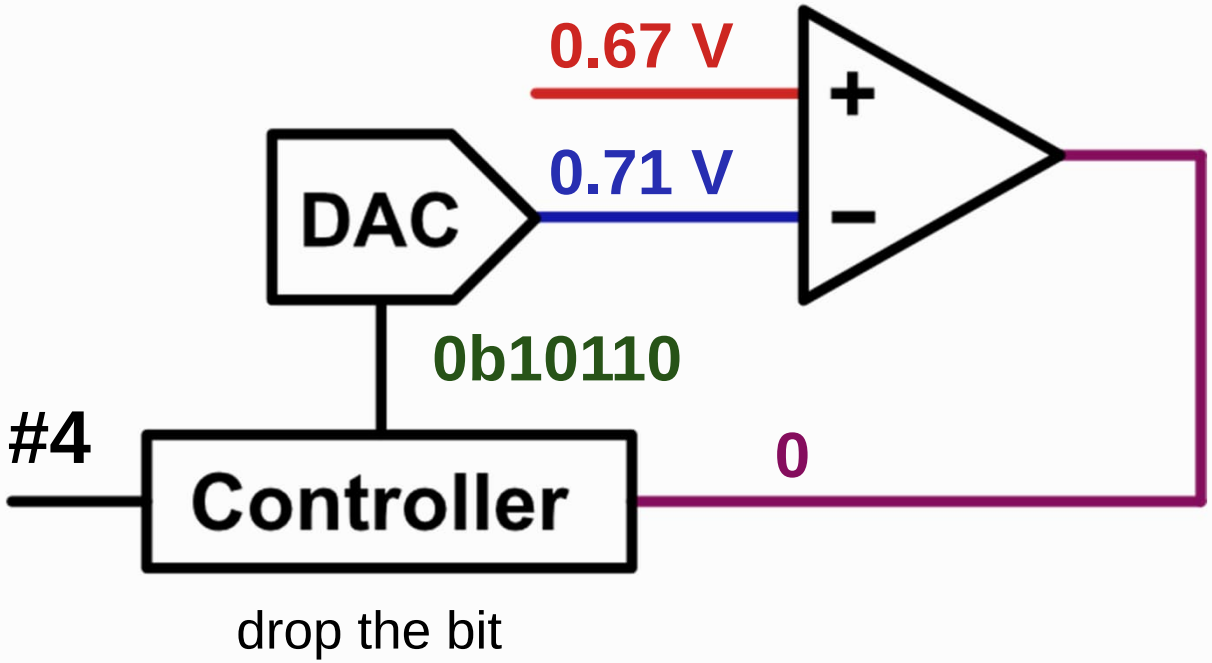

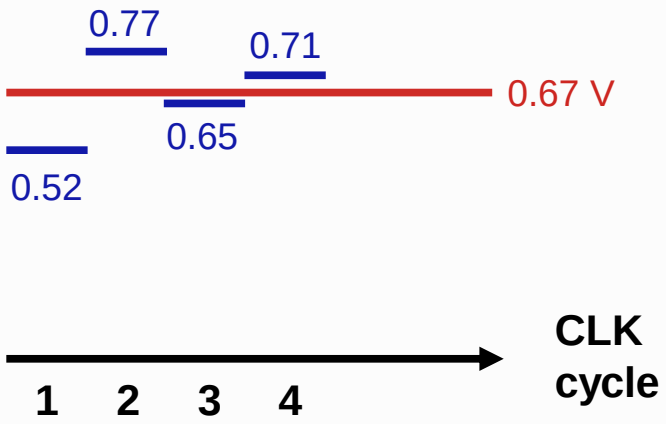

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