

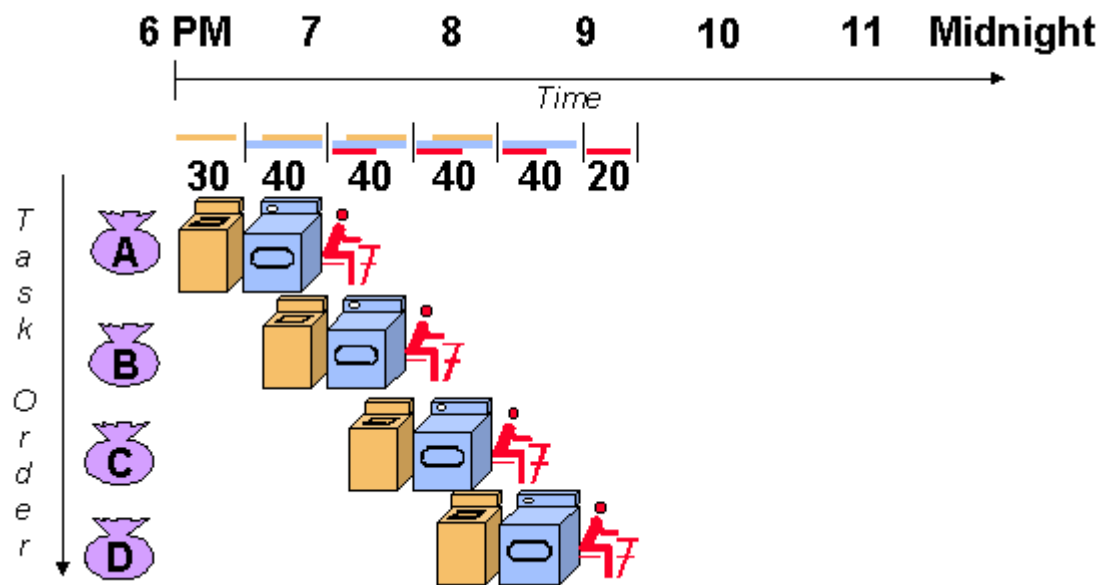
Design Activity 2

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COE17B010

Introduction:

Pipelining is a performance improvement technique by which we arrange the hardware such that more than one operation can be performed at the same time.

We do this by splitting the overall hardware into a series of submodules and attaching flip flops in between those stages. So, with each clock cycle inputs get processed by the stage and get stored in their respective stage flip flops. Thus, we can feed inputs as a series and outputs come out in 1 clock cycle itself.



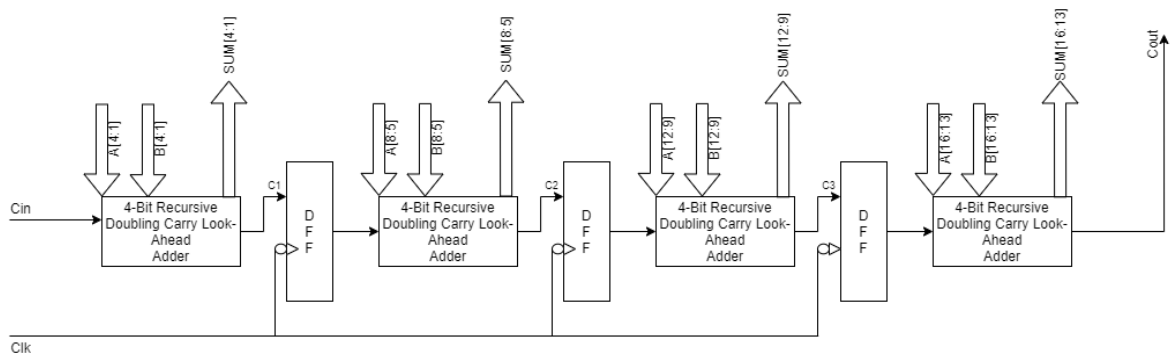
Primitive Gate Delay Values:

Logic gates	Delay considered (In Gate Delay Units)
NOT	1
AND	1

OR	1
NAND	2
NOR	2
XOR	2
MUX	1

16-bit Adder

Design:



Analysis:

1. Number of pipeline stages: 4

Stage 1	First 4 Bits Addition [4:1]
Stage 2	Second 4 Bits Addition [8:5]
Stage 3	Third 4 Bits Addition [12:9]
Stage 4	Last 4 Bits Addition [16:13]

2. Logic components:

Stages	Logic components involved (Number)	Total Delay (delay)
Stage 1	AND (14), XOR (4), NOT (6), NAND (4), NOR (8)	NOR (2) + AND (1) + NOR (2) + XOR (2) = 7
Stage 2	AND (14), XOR (4), NOT (6), NAND (4), NOR (8)	NOR (2) + AND (1) + NOR (2) + XOR (2) = 7
Stage 3	AND (14), XOR (4), NOT (6), NAND (4), NOR (8)	NOR (2) + AND (1) + NOR (2) + XOR (2) = 7
Stage 4	AND (14), XOR (4), NOT (6), NAND (4), NOR (8)	NOR (2) + AND (1) + NOR (2) + XOR (2) = 7

3. Calculations:

Exe Time Pipeline = (No. of Stages + No. of operations - 1) * Delay of 1 clock cycle

Here, Delay of 1 clock cycle = Max. (limiting) Stage Delay = 7 Gate Delay Units

No. of Stages = 4

Consider No. of operations = 100,

ET-Pipeline = $(4 + 100 - 1) * 7 = 721$ Gate Delay Units

Exe Time Non-Pipeline = (No. of operations) * Delay of Longest Path

= $100 * (7 * 4) = 2800$ Gate Delay Units

Efficiency = Given Speedup / Max Speedup

In ideal case, Max. Speedup = No. of Stages

Efficiency-Pipeline = $((\text{No of operations} * \text{No of Stages}) / (\text{No of Stages} + \text{No of operations} - 1)) / \text{No of Stages}$

$$= ((100 \times 4) / (100 + 4 - 1)) / 4 = 100 / 103 = \mathbf{0.97}$$

Throughput = No of operations / Execution Time

Throughput-Pipeline = $100 / 721 = \mathbf{0.139}$ operations per gate delay

Throughput-Non-Pipeline = $100 / 2800 = \mathbf{0.036}$ operations per gate delay

4. Comparison:

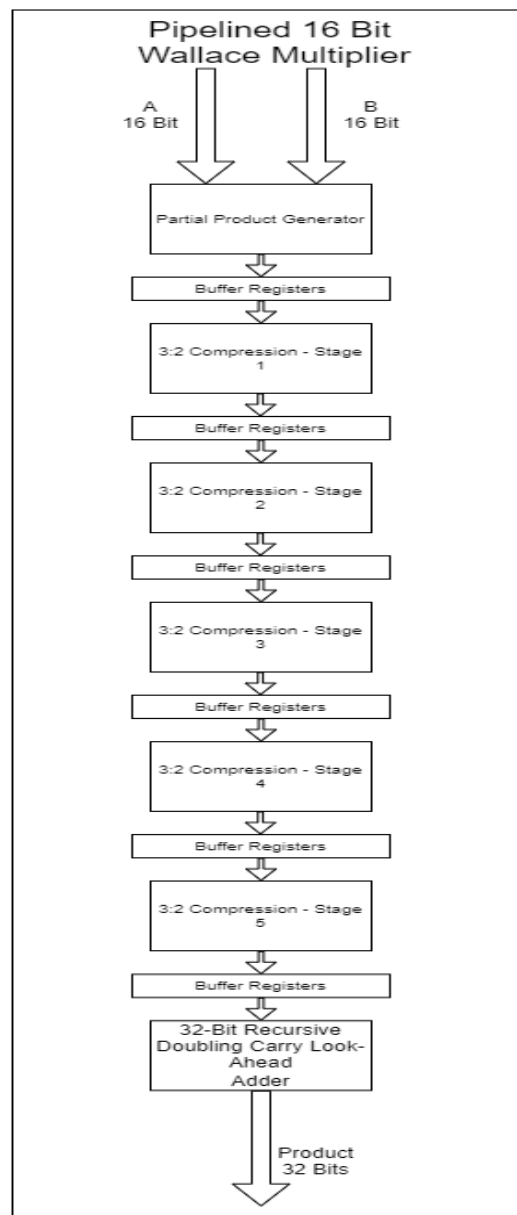
Factors	Non-Pipelined	Pipelined
Extra hardware	No	Extra DFFs, clock wiring, clock generation hardware
Cost	Less	More cost due to extra hardware
Area on chip	Less	More area due to extra components
Execution time (For 100 operations in Gate Delay Units)	2800	721
Power required	Less	High due to extra DFFs
Complexity	Less	More due to more connections and logical circuits
Efficiency	-	0.97
Throughput	0.036	0.139

5. Speedup:

$$\text{Speedup from pipelining} = \frac{\text{Average execution time unpipelined}}{\text{Average execution time pipelined}}$$
$$= 2800 / 721 = \mathbf{3.88}$$

16-bit Wallace Multiplier

Design:



Analysis:

1. Number of pipeline stages: 7

Stage 1	Partial Product Generation
Stage 2	3:2 Compression
Stage 3	3:2 Compression
Stage 4	3:2 Compression
Stage 5	3:2 Compression
Stage 6	3:2 Compression
Stage 7	32-Bit Addition

2. Logic components:

Half adder: XOR (1), AND (1)

Delay = XOR (2) = 2

Full adder: XOR (2), AND (2), OR (1)

Delay = XOR (2) + AND (1) + OR (1) = 4

Stages	Logic components involved (Number)	Total Delay (delay)
Stage 1	AND (256)	AND (1)

Stage 2	Half Adder (2), Full Adder (14)	Full Adder (4)
Stage 3	Half Adder (2), Full Adder (14)	Full Adder (4)
Stage 4	Half Adder (2), Full Adder (14)	Full Adder (4)
Stage 5	Half Adder (2), Full Adder (14)	Full Adder (4)
Stage 6	Half Adder (2), Full Adder (14)	Full Adder (4)
Stage 7	32-bit RD CLA	$7 \times 8 = 56$

3. Calculations:

Exe Time Pipeline = (No. of Stages + No. of operations - 1) * Delay of 1 clock cycle

Here, Delay of 1 clock cycle = Max. (limiting) Stage Delay = **56** Gate Delay Units

No. of Stages = 7

Consider No. of operations = 100,

ET-Pipeline = $(7 + 100 - 1) \times 56 = 5936$ Gate Delay Units

Exe Time Non-Pipeline = (No. of operations) * Delay of Longest Path

= $100 \times (1 + 4 + 4 + 4 + 4 + 4 + 56) = 7700$ Gate Delay Units

Efficiency = Given Speedup / Max Speedup

In ideal case, Max. Speedup = No. of Stages

Efficiency-Pipeline = $((\text{No of operations} \times \text{No of Stages}) / (\text{No of Stages} + \text{No of operations} - 1)) / \text{No of Stages}$

= $((100 \times 7) / (100 + 7 - 1)) / 7 = 100/106 = 0.94$

Throughput = No of operations / Execution Time

Throughput-Pipeline = $100 / 5936 = 0.017$ operations per gate delay

Throughput-Non-Pipeline = $100 / 7700 = 0.013$ operations per gate delay

4. Comparison:

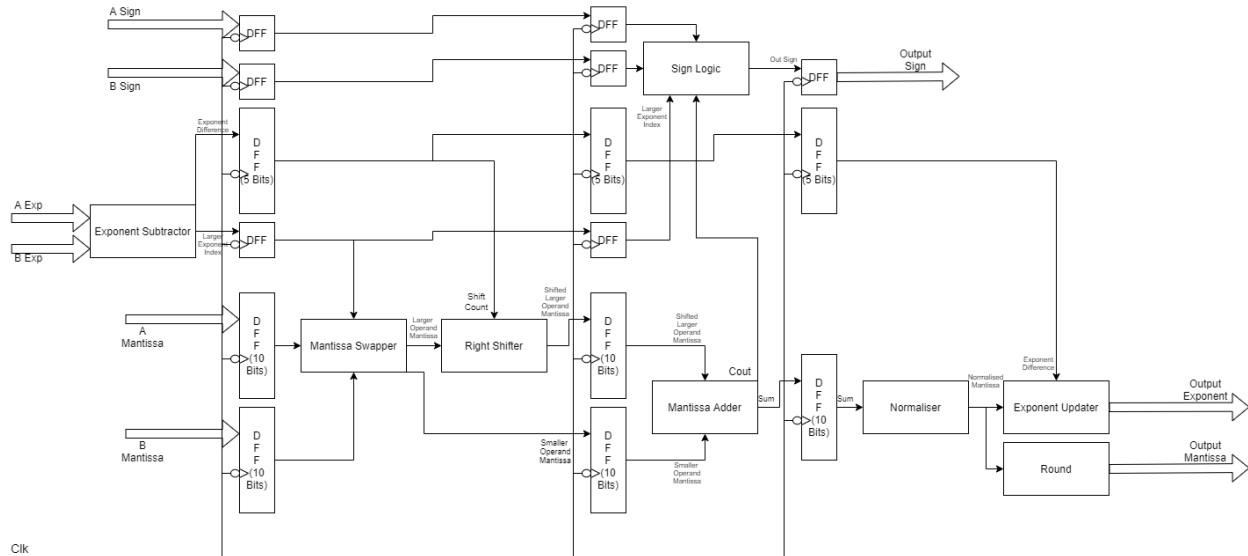
Factors	Non-Pipelined	Pipelined (Design 2)
Extra hardware	No	Extra DFFs, clock wiring, clock generation hardware
Cost	Less	More cost due to extra hardware
Area on chip	Less	More area due to extra components
Execution time (For 100 operations in Gate Delay Units)	7700	5936
Power required	Less	High due to extra DFFs
Complexity	Less	More due to more connections and logical circuits
Efficiency	-	0.94
Throughput	0.013	0.017

5. Speedup:

$$\begin{aligned}\text{Speedup from pipelining} &= \frac{\text{Average execution time unpipelined}}{\text{Average execution time pipelined}} \\ &= 7700 / 5936 = \mathbf{1.29}\end{aligned}$$

Half Precision Floating Point Adder

Design:



Analysis:

1. Number of pipeline stages: 4

Stage 1	Exponent Subtraction - Detect Larger Exponent
Stage 2	Swap Mantissa & Right Shift larger value
Stage 3	Sign Logic & Add Mantissas
Stage 4	Renormalize & Round Output Mantissa and Update Output Exponent

2. Logic components:

Stages	Logic components involved (Number)	Total Delay (delay)
Stage 1	NOT (5), 8-Bit CLA (1)	NOT (1) + Adder (14) = 15
Stage 2	2:1 MUX (1), 10-Bit Barrel Shifter (1)	MUX (1) + Shifter (1) = 2
Stage 3	16-Bit CLA (1), Sign Logic (1)	Adder (28) + Sign Logic (1) = 29
Stage 4	16-Bit Priority Encoder (1), 10-Bit Barrel Shifter, 8-Bit CLA (1)	Priority Encoder (5) + Shifter (1) + Adder (14) = 20

3. Calculations:

Exe Time Pipeline = (No. of Stages + No. of operations - 1) * Delay of 1 clock cycle

Here, Delay of 1 clock cycle = Max. (limiting) Stage Delay = **29** Gate Delay Units

No. of Stages = 4

Consider No. of operations = 100,

ET-Pipeline = $(4 + 100 - 1) * 29 = \mathbf{2987}$ Gate Delay Units

Exe Time Non-Pipeline = (No. of operations) * Delay of Longest Path

= $100 * (15 + 2 + 29 + 20) = \mathbf{6600}$ Gate Delay Units

Efficiency = Given Speedup / Max Speedup

In ideal case, Max. Speedup = No. of Stages

Efficiency-Pipeline = $((\text{No of operations} * \text{No of Stages}) / (\text{No of Stages} + \text{No of operations} - 1)) / \text{No of Stages}$

= $((100*4) / (100+4-1)) / 4 = 100/103 = 0.97$

Throughput = No of operations / Execution Time

Throughput-Pipeline = $100 / 2987 = 0.033$ operations per gate delay

Throughput-Non-Pipeline = $100 / 6600 = 0.015$ operations per gate delay

4. Comparison:

Factors	Non-Pipelined	Pipelined
Extra hardware	No	Extra DFFs, clock wiring, clock generation hardware
Cost	Less	More cost due to extra hardware
Area on chip	Less	More area due to extra components
Execution time (For 100 operations in Gate Delay Units)	6600	2987
Power required	Less	High due to extra DFFs
Complexity	Less	More due to more connections and logical circuits
Efficiency	-	0.97
Throughput	0.015	0.033

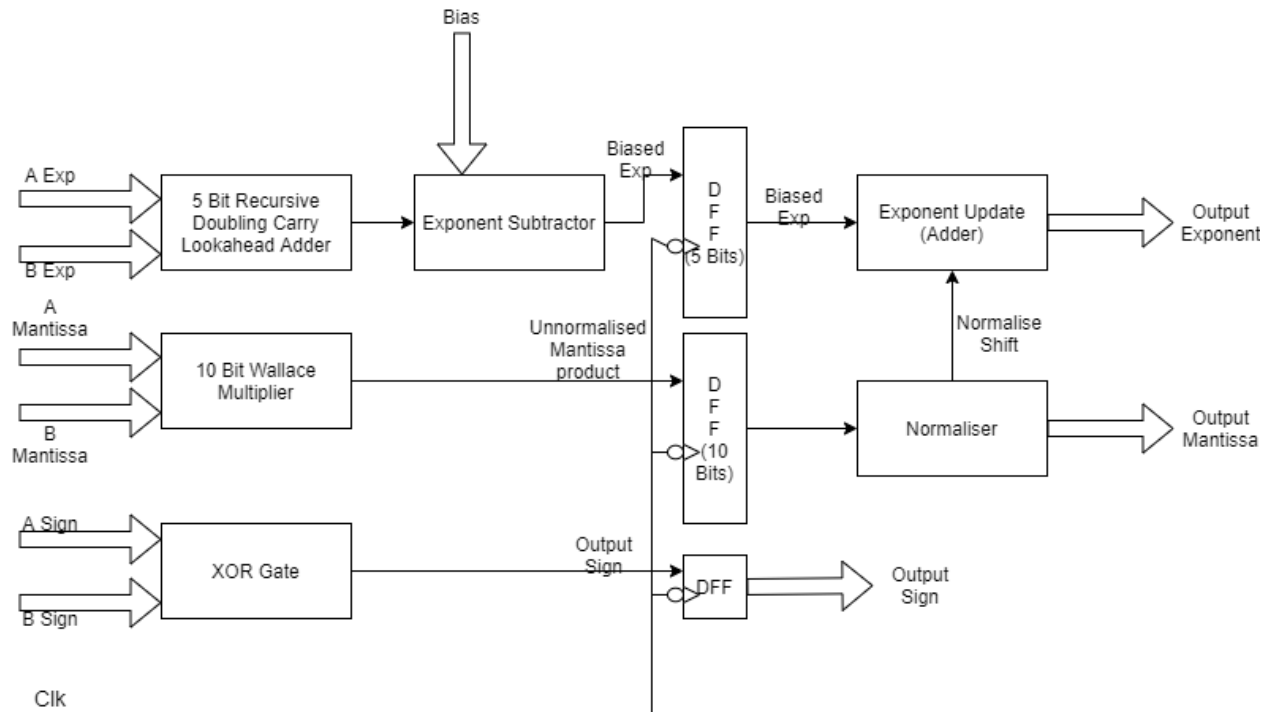
5. Speedup:

Speedup from pipelining = $\frac{\text{Average execution time unpipelined}}{\text{Average execution time pipelined}}$

= $6600 / 2987 = 2.21$

Half Precision Floating Point Multiplier

Design:



Analysis:

1. Number of pipeline stages: 2

Stage 1	Exponent Addition & Mantissa Multiplication & Sign Logic
Stage 2	Normalization and Exponent Updation

2. Logic components:

Stages	Logic components involved (Number)	Total Delay (delay)
Stage 1	8-Bit CLA (2), 16-Bit Wallace Multiplier (1), XOR (1)	Multiplier (77)
Stage 2	16-Bit Priority Encoder (1), 10-Bit Barrel Shifter, 8-Bit CLA (1)	Priority Encoder (5) + Shifter (1) + Adder (14) = 20

3. Calculations:

Exe Time Pipeline = (No. of Stages + No. of operations - 1) * Delay of 1 clock cycle

Here, Delay of 1 clock cycle = Max. (limiting) Stage Delay = **77** Gate Delay Units

No. of Stages = 2

Consider No. of operations = 100,

ET-Pipeline = $(2 + 100 - 1) * 77 = 7777$ Gate Delay Units

Exe Time Non-Pipeline = (No. of operations) * Delay of Longest Path

= $100 * (77 + 20) = 9700$ Gate Delay Units

Efficiency = Given Speedup / Max Speedup

In ideal case, Max. Speedup = No. of Stages

Efficiency-Pipeline = $((\text{No of operations} * \text{No of Stages}) / (\text{No of Stages} + \text{No of operations} - 1)) / \text{No of Stages}$

= $((100*2) / (100+2-1)) / 2 = 100/101 = 0.99$

Throughput = No of operations / Execution Time

Throughput-Pipeline = $100 / 7777 = 0.013$ operations per gate delay

Throughput-Non-Pipeline = $100 / 9700 = 0.010$ operations per gate delay

4. Comparison:

Factors	Non-Pipelined	Pipelined
Extra hardware	No	Extra DFFs, clock wiring, clock generation hardware
Cost	Less	More cost due to extra hardware
Area on chip	Less	More area due to extra components
Execution time (For 100 operations in Gate Delay Units)	9700	7777
Power required	Less	High due to extra DFFs
Complexity	Less	More due to more connections and logical circuits
Efficiency	-	0.99
Throughput	0.010	0.013

5. Speedup:

$$\begin{aligned}\text{Speedup from pipelining} &= \frac{\text{Average execution time unpipelined}}{\text{Average execution time pipelined}} \\ &= 9700 / 7777 = \mathbf{1.25}\end{aligned}$$